IFPA300, IFPA301

Monolithic JFET Preamplifier

Description & Features

The IFPA300 series is an inverting transimpedance amplifier featuring extremely low noise and a wide gain-bandwidth suitable as a charge-sensitive pre-amplifier for a broad range of applications.

The monolithic IFPA300 series contain 8 n-channel epitaxial-channel diffused-gate JFETs to achieve optimally low 1/f noise performance over a wide temperature range (120K-300K).

DC open loop gain	85 dB
GBW	200 MHz
$\bar{e}_N$ @ 10 Hz	3.0 nV/√Hz

General Specifications

Power Dissipation at VDD = 12 V	<100 mW
Input Leakage Current (T = 300 K)	10 pA
Input-Referred Noise Voltage (f = 10 kHz)	0.6 nV/√Hz
Input-Referred Noise Voltage (f = 10 Hz)	3.0 nV/√Hz
Output Range at VDD = 12 V	4.0 V (5.0 V Max)

Designed to drive 50Ω load.

Charge Sensitive Preamplifier Specifications

The IFPA300 Series is actually tailored to detector capacitance in the 100 – 1000 pF range.

Input Open-Loop Capacitance	60 pF
Rise Time (CD = 500 pF, Cf = 33 pF)	20 ns

Equivalent Noise Charge

(Measured with semigaussian shaping, peaking time = t_p)

4200 e– rms at CD @ 500 pF, t_p = 0.2 µm

3200 e– rms at CD @ 500 pF, t_p = 1.0 µm

4200 e– rms at CD @ 500 pF, t_p = 4.0 µm

Absolute maximum ratings at TA = 25°C

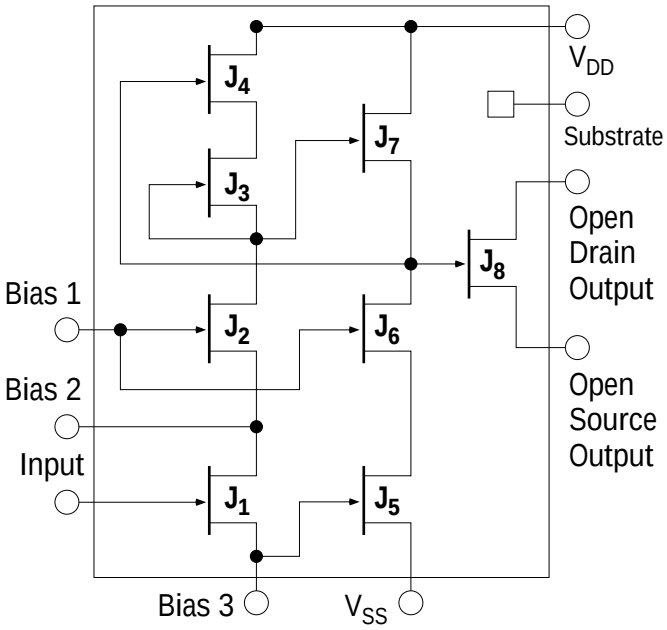
All pins (except Input) referenced to Bias 3	85 dB
Input to Bias 3	Ø V
Power Dissipation	225 mW
Derating Factor	1.8 mW/°C
Operating Temperature	150°C

At this time, there are two units in this family.

The 300/301 Series gives more flexibility with respect to output transistor drain.

The 310/311 Series ties the output transistor drain to the V_{DD} line.

Simplified Schematic Circuit



Packages & Test Circuit Overside

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1000 N. Shiloh Road, Garland, TX 75042
(972) 487-1287 FAX (972) 276-3375
www.interfet.com

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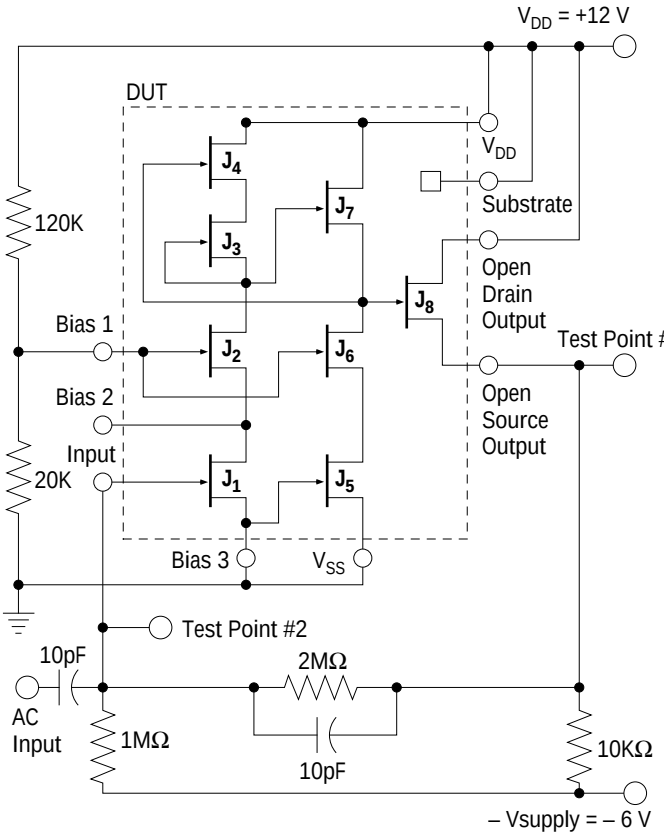
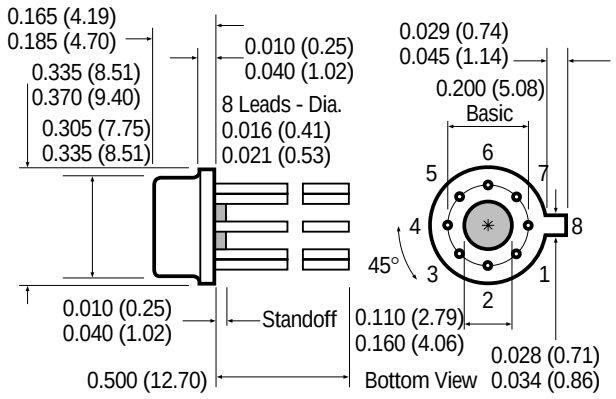
Input FET J1 selected to the following elecrical parameters.

Parameter	Conditions	Min	Max	Units
BV_{GSS}	Vds = 0, Ig = 1 µA	– 25		Volts
I_{GSS}	Vds = 0, Vgs = – 10 V		2	nA
I_{DSS}	Vds = 0, Vgs = 10 V	40	500	mA
$V_{GS(OFF)}$	Vds = 0, Id = 1 µA	1	2	Volts
G_M	Vgs = 0, Vds = 10 V	50		mM
V_{GSF}	Id = 1 µA	0.35	0.65	Volts

Test Circuit Reference

Parameter	Conditions	Min	Max	Units
VDCout	Vdd = 12 V, – VS = – 6 V Test pt #1	6	10	V
Vin	Vdd = 12 V, – VS = – 6 V Test pt #2	– 0.6	– 1.6	V
VACout	Vdd = 12 V, – VS = – 6 V t = O µsec	50		mV
VACout	Vdd = 12 V, – VS = – 6 V t = 100 µsec		20	mV



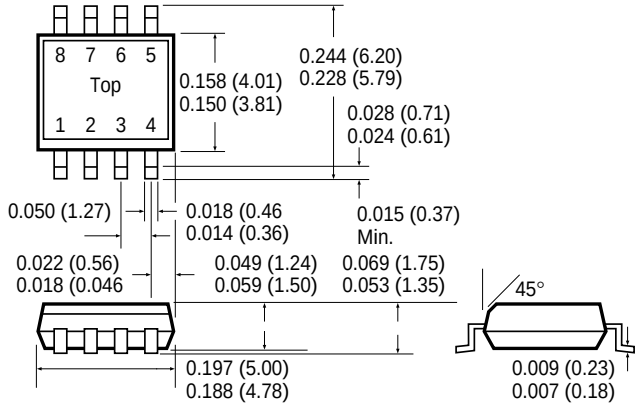


IFPA300 uses TO-99 Package

Dimensions in Inches (mm)

Pin Configuration

1 Bias 3, 2 VSS, 3 Bias 1, 4 VDD /Substrate
5 Open Drain Output, 6 Open Source Output, 7 Bias 2, 8 Input



IFPA301 uses SOIC-8 Package

Dimensions in Inches (mm)

Pin Configuration

1 Bias 2, 2 Input, 3 Bias 3, 4 VSS, 5 Bias 1, 6 VDD/Substrate
7 Open Drain Output, 8 Open Source Output

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