ADVANCED SMARTRECTIFIER™ CONTROL IC

Features

- Secondary side high speed SR controller
- Flyback, Forward and Half-bridge topologies
- CCM operation with SYNC function
- 200 V proprietary IC technology
- Max 500 KHz switching frequency
- Anti-bounce logic and UVLO protection
- 4 A peak turn off drive current
- Micropower start-up & low quiescent current
- 10.7 V gate drive clamp
- 50 ns turn-off propagation delay
- Vcc range from 11 V to 20 V
- Enable function synchronized with MOSFET VDS transition
- Cycle by Cycle MOT Check Circuit prevents multiple false trigger GATE pulses
- Lead-free
- Compatible with 0.3 W Standby, Energy Star, CECP, etc.

Typical Applications

- Telecom SMPS, ATX SMPS, Server SMPS, AC-DC adapters

Product Summary

Topology	Flyback, Forward, Half-Bridge
VD	200 V
V_{OUT}	10.7 V
I_{o+} & I_{o-} (typ.)	+1 A & -4 A
Turn on Propagation Delay (typ.)	70 ns
Turn off Propagation Delay (typ.)	50 ns

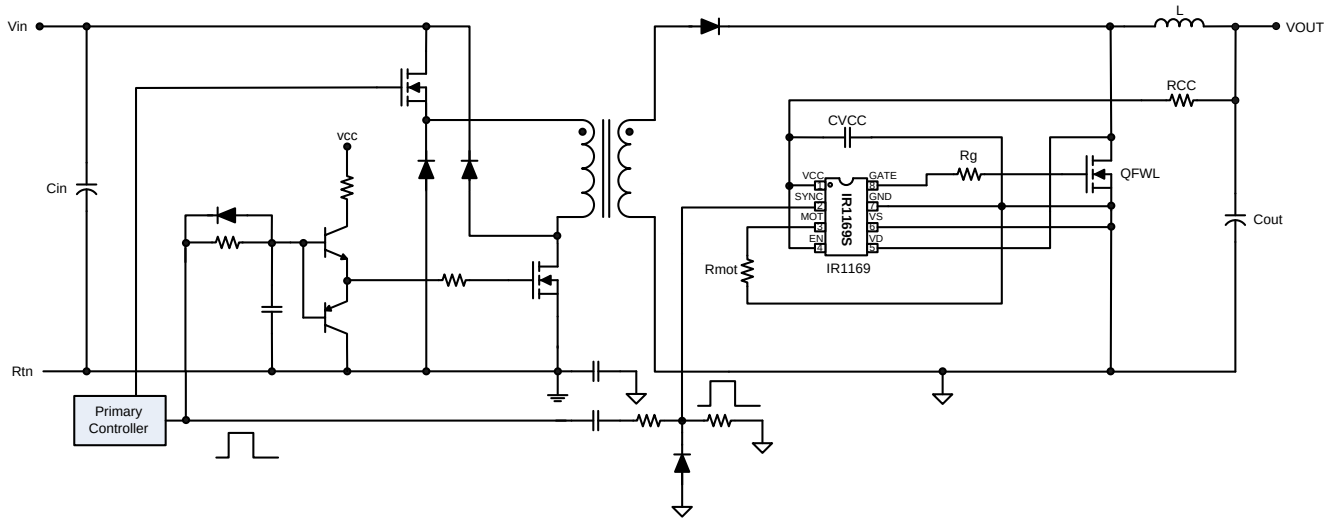
Package Options

8-Lead SOIC

Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
IR1169S	SOIC8N	Tube/Bulk	95	IR1169SPBF
		Tape and Reel	2500	IR1169STRPBF

Typical Connection Diagram



Description

IR1169 is a smart secondary-side driver IC designed to drive N-Channel power MOSFETs used as synchronous rectifiers in isolated Flyback, Forward or Half-bridge converters. The IC can control one or more paralleled N-MOSFETs to emulate the behavior of Schottky diode rectifiers. IR1169 works in both DCM and CCM operation modes. The SYNC pin should be used in CCM mode to directly turn-off the MOSFET by a signal from secondary or primary controller. The IC is designed to use simple capacitor coupling interface to communicate with primary controller. In addition to the SYNC control, the drain to source voltage is sensed differentially to determine the polarity of the current and turn the power switch on and off in proximity of the zero current transition. Ruggedness and noise immunity are accomplished using an advanced blanking scheme and double-pulse suppression which allow reliable operation in all operating modes.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Parameters	Symbol	Min.	Max.	Units	Remarks
Supply Voltage	V_{CC}	-0.3	20	V	
Enable Voltage	V_{EN}	-0.3	20		
Cont. SYNC Voltage	V_{SYNC}	-0.3	20		
Pulse SYNC Voltage	V_{SYNC}	-0.7 †	20		
SYNC Current	I_{SYNC}	-10	10	mA	
Cont. Drain Sense Voltage	V_D	-1	200	V	
Pulse Drain Sense Voltage	V_D	-5	200		
Source Sense Voltage	V_S	-3	20		
Gate Voltage	V_{GATE}	-0.3	20		V_{CC}=20V, Gate off
Operating Junction Temperature	T_J	-40	150	°C	
Storage Temperature	T_S	-55	150		
Thermal Resistance	$R_{\theta JA}$		128	°C/W	SOIC-8
Package Power Dissipation	P_D		970	mW	SOIC-8, T_{AMB}=25°C
Switching Frequency	fsw		500	kHz	

† An input resistor of 2kΩ or above is required to SYNC pin for negative pulse

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions.

Symbol	Definition	Min.	Max.	Units
V_{CC}	Supply Voltage	11	19	V
V_D	Drain Sense Voltage	-3 ††	200	
T_J	Junction Temperature	-25	125	°C
Fsw	Switching Frequency	---	500	kHz

†† V_D -3V negative spike width ≤100ns

Recommended Component Values

Symbol	Component	Min.	Max.	Units
R_{MOT}	MOT pin resistor value	5	75	kΩ

Electrical Characteristics

V_{CC}=15V and T_A = 25°C unless otherwise specified. The output voltage and current (V_O and I_O) parameters are referenced to GND (pin7).

Supply Section

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
V_{CC} Turn On Threshold	$V_{CC\ ON}$	9.4	10.4	11.0	V	
V_{CC} Turn Off Threshold (Under Voltage Lock Out)	$V_{CC\ UVLO}$	8.6	9.3	10.0		
V_{CC} Turn On/Off Hysteresis	$V_{CC\ HYST}$		1.1			
Operating Current	I_{CC}		8.5	10	mA	C_{LOAD}=1nF,f_{SW}=400kHz
			45	55		C_{LOAD}=10nF,f_{SW}=400kHz
Quiescent Current	I_{QCC}		1.8	2.3		SYNC=low
Start-up Current	$I_{CC\ START}$		100	200	µA	V_{CC}=$V_{CC\ ON}$ - 0.1V
Sleep Current	I_{SLEEP}		150	200		V_{EN}=0V, V_{CC} =15V
Enable Voltage High	V_{ENHI}	2.25	2.8	3.3	V	
Enable Voltage Low	V_{ENLO}	1.2	1.6	2.0		
Enable Pull-up Resistance	R_{EN}		1.5		MΩ	GBD

Comparator Section

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Turn-off Threshold	V_{TH1}	-7	-3.5	0	mV	
Turn-on Threshold	V_{TH2}	-263	-230	-197		
Hysteresis	V_{HYST}		230			
Input Bias Current	I_{IBIAS1}		1	7.5	µA	V_D = -50mV
	I_{IBIAS2}		10	100		V_D = 200V
Input CM Voltage Range	V_{CM}	0		2	V	

One-Shot Section

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Blanking pulse duration	t_{BLANK}	9	17	25	µs	
Reset Threshold	V_{TH3}		2.5		V	V_{CC}=10V – GBD
			5.4		V	V_{CC}=20V – GBD
Hysteresis	V_{HYST3}		40		mV	V_{CC}=10V – GBD

Minimum On Time Section

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Minimum on time	T_{Onmin}	180	240	300	ns	R_{MOT} =5kΩ, V_{CC}=12V
		2.4	3	3.6	µs	R_{MOT} =75kΩ, V_{CC}=12V

Electrical Characteristics

V_{CC}=15V and T_A = 25°C unless otherwise specified. The output voltage and current (V_O and I_O) parameters are referenced to GND (pin7).

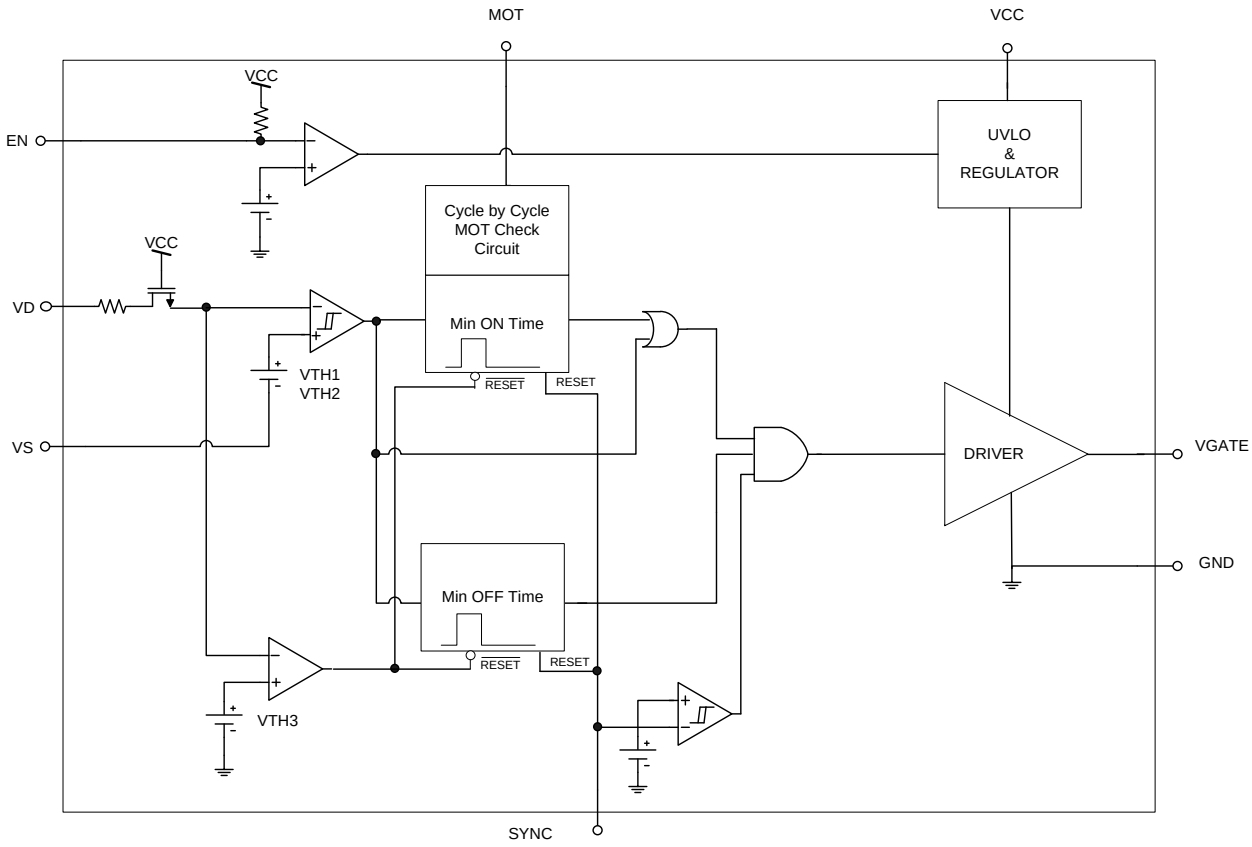
SYNC Section

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
SYNC Voltage High (disable)	V_{SYHI}	2.0	2.5	3.0	V	
SYNC Voltage Low (enable)	V_{SYLO}	0.6	0.8	1.0		
SYNC Turn-on Prop. Delay	T_{Syon}		65	100	ns	SYNC =high to low
SYNC Turn-off Prop. Delay	T_{Syoff}		55	90		SYNC=low to high
Minimum SYNC pulse width	T_{SYPW}	50				GBD

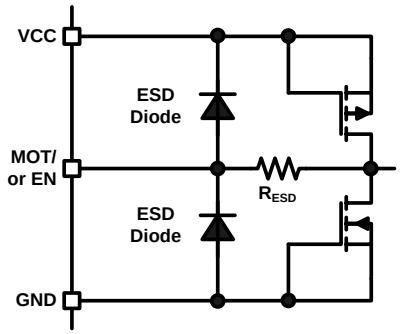
Gate Driver Section

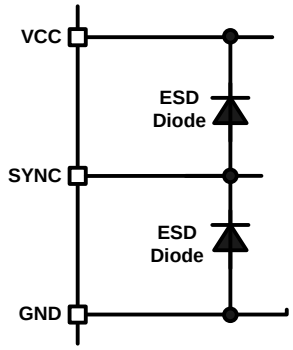
Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Gate Low Voltage	V_{GLO}		0.24	0.5	V	I_{GATE} = 200mA
Gate High Voltage	V_{GTH}	9.0	10.7	14		V_{CC}=12V-18V (internally clamped)
Rise Time	t_{r1}		20		ns	C_{LOAD} = 1nF, V_{CC}=12V
	t_{r2}		180			C_{LOAD} = 10nF, V_{CC}=12V
Fall Time	t_{f1}		10			C_{LOAD} = 1nF, V_{CC}=12V
	t_{f2}		44			C_{LOAD} =10nF, V_{CC}=12V
Turn on Propagation Delay	t_{Don}		70	95		V_{DS} to V_{GATE} –V_{DS} goes down from 6V to -1V
Turn off Propagation Delay	t_{Doff}		50	75		V_{DS} to V_{GATE} –V_{DS} goes up from -1V to 6V
Pull up Resistance	r_{up}		5		Ω	I_{GATE} = 200mA – GBD
Pull down Resistance	r_{down}		1.2			I_{GATE} = -200mA
Output Peak Current (source)	$I_{O\ source}$		1		A	C_{LOAD} = 10nF – GBD
Output Peak Current (sink)	$I_{O\ sink}$		4			

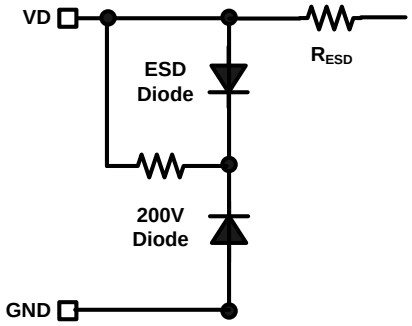
Functional Block Diagram

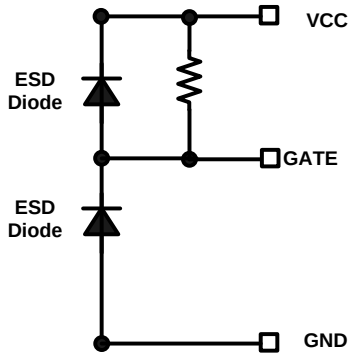


I/O Pin Equivalent Circuit Diagram





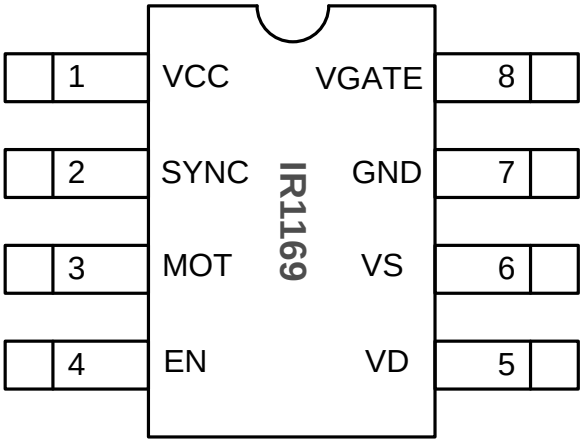




Lead Definitions

PIN#	Symbol	Description
1	VCC	Supply Voltage
2	SYNC	SYNC Input for direct turn off
3	MOT	Minimum On Time
4	EN	Enable
5	VD	FET Drain Sensing
6	VS	FET Source Sensing
7	GND	Ground
8	VGATE	Gate Drive Output

Lead Assignments



Detailed Pin Description

VCC: Power Supply
This is the supply voltage pin of the IC and it is monitored by the under voltage lockout circuit. It is possible to turn off the IC by pulling this pin below the minimum turn off threshold voltage, without damage to the IC.
To prevent noise problems, a bypass ceramic capacitor connected to Vcc and COM should be placed as close as possible to the IR1169. This pin is internally clamped.

SYNC: Direct Turn-off and Reset
SYNC is used to directly turn-off the SR MOSFET by an external signal. The gate output of IR1169 is low when SYNC voltage is higher than V_{SYHI} threshold. The propagation delay from SYNC goes high to gate turns off is 55ns. The turn-off of SYNC is a direct control and it ignores the MOT time (override).

The SYNC pin will reset MOT and Blanking time when SYNC switches from low to high. It will reset MOT timer and Blanking timer only at the rising edge of signal. This function is useful for very low output voltage condition (such as overload or short circuit) where the VD voltage is too low to reach Vth3 threshold to reset the timers.

SYNC pin also can be used to control the turn-on time of SR MOSFET (adding additional delay time at turn-on for noise immunity).

If not used, SYNC pin should be connected to GND.

MOT: Minimum On Time
The MOT programming pin controls the amount of minimum on time. When V_{SYNC} is low and V_{TH2} is crossed, the gate signal will become active and turn on the power FET. Spurious ringings and oscillations can trigger the input comparator off. The MOT blanks the input comparator keeping the FET on for a minimum time.
The MOT is programmed between 200ns and 3us (typ.) by using a resistor referenced to COM.

EN: Enable
This pin is used to activate the IC “sleep” mode by pulling the voltage level below 1.6V (typ). In sleep mode the IC will consume a minimum amount of current. All switching functions will be disabled and the gate will be inactive. The EN pin voltage cannot linger between the Enable low and Enable high thresholds. The pin is intended to operate as a switch with the pin voltage either above or below the threshold range. The Enable control pin (EN) is not intended to operate at high frequency. For proper operation, EN positive pulse width needs to be longer than 20µs, EN negative pulse width needs to be longer than 10µs. Please refer to Figure 15B for the definition of EN pulse width.

VD: Drain Voltage Sense
VD is the voltage sense pin for the power MOSFET Drain. This is a high voltage pin and particular care must be taken in properly routing the connection to the power MOSFET drain.

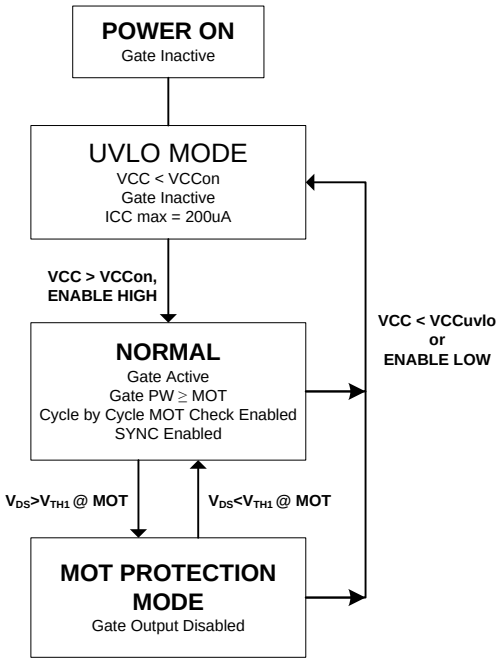
VS: Source Voltage Sense
VS is the differential sense pin for the power MOSFET Source. This pin should be connected directly to the power ground pin (7) but must be used to create a kelvin contact as close as possible to the power MOSFET source pin.

GND: Ground
This is ground potential pin of the integrated control circuit. The internal devices and gate driver are referenced to this point.

VGATE: Gate Drive Output
This is the gate drive output of the IC. Drive voltage is internally limited and provides 1A peak source and 4A peak sink capability. Although this pin can be directly connected to the power MOSFET gate, the use of minimal gate resistor is recommended, especially when putting multiple FETs in parallel.
Care must be taken in order to keep the gate loop as short and as small as possible in order to achieve optimal switching performance.

Application Information and Additional Details

State Diagram



UVLO/Sleep Mode

The IC remains in the UVLO condition until the voltage on the VCC pin exceeds the VCC turn on threshold voltage, $V_{CC\ ON}$. During the time the IC remains in the UVLO state, the gate drive circuit is inactive and the IC draws a quiescent current of $I_{CC\ START}$. The UVLO mode is accessible from any other state of operation whenever the IC supply voltage condition of VCC < $V_{CC\ UVLO}$ occurs.
The sleep mode is initiated by pulling the EN pin below 1.6V (typ). In this mode the IC is essentially shut down and draws a very low quiescent supply current.

Normal Mode and Synchronized Enable Function

The IC enters in normal operating mode once the UVLO voltage has been exceeded and EN voltage is above V_{ENHI} threshold. When the IC enters Normal Mode from UVLO Mode, the GATE output is disabled (stays low) until V_{DS} exceeds V_{TH3} to activate the gate. This ensures that the GATE output is not enabled in the middle of a switching cycle. This logic prevents any reverse currents across the device due to minimum on time function in the IC. The gate will continuously drive the SR MOSFET after this one-time activation. The Cycle by Cycle MOT protection circuit is enabled in Normal Mode.

MOT Protection Mode

If the secondary current conduction time is shorter than the MOT (Minimum On Time) setting, the next driver output is disabled. This function can avoid reverse current that occurs when the system works at very low duty-cycles or at very light/no load conditions and reduce system standby power consumption by disabling GATE outputs. The Cycle by Cycle MOT Check circuit is always activated under Normal Mode and MOT Protection Mode, so that the IC can automatically resume normal operation once the load increases to a level and the secondary current conduction time is longer than MOT.

General Description

The IR1169 Smart Rectifier IC can emulate the operation of diode rectifier by properly driving a Synchronous Rectifier (SR) MOSFET. The direction of the rectified current is sensed by the input comparator using the power MOSFET R_{Dson} as a shunt resistance and the GATE pin of the MOSFET is driven accordingly. Internal blanking logic is used to prevent spurious transitions. The Synchronous pin (SYNC) can directly take the signal sent from primary controller to turn off the gate of SR MOSFET prior to the turn-on of primary MOSFET therefore prevent negative current in SR circuit under CCM condition.

IR1169 is suitable for Flyback, Forward and Resonant Half-Bridge topologies.

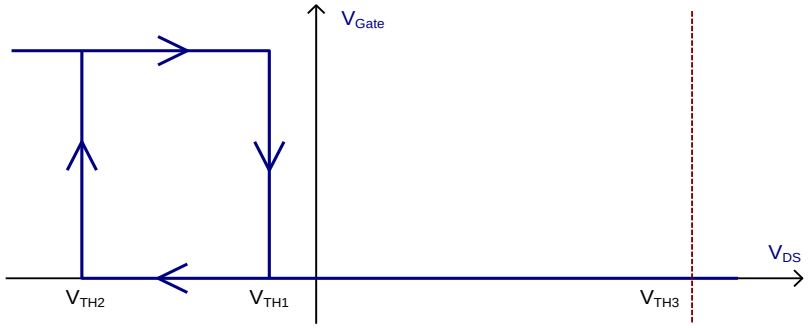


Figure 1: Input comparator thresholds

Flyback Application

The modes of operation for a Flyback circuit differ mainly for the turn-off phase of the SR switch, while the turn-on phase of the secondary switch (which corresponds to the turn off of the primary side switch) is identical.

Turn-on phase

When the conduction phase of the SR FET is initiated, current will start flowing through its body diode, generating a negative V_{DS} voltage across it. The body diode has generally a much higher voltage drop than the one caused by the MOSFET on resistance and therefore will trigger the turn-on threshold V_{TH2}.

At that point, if SYNC voltage is low IR1169 will drive the gate of MOSFET on, which will in turn cause the conduction voltage VDS to drop down. This drop is usually accompanied by some amount of ringing, that can trigger the input comparator to turn off; hence, a Minimum On Time (MOT) blanking period is used that will maintain the power MOSFET on for a minimum amount of time.

The programmed MOT will limit also the minimum duty cycle of the SR MOSFET and, as a consequence, the max duty cycle of the primary side switch.

DCM/CrCM Turn-off phase

Once the SR MOSFET has been turned on, it will remain on until the rectified current will decay to the level where V_{DS} will cross the turn-off threshold V_{TH1}. This will happen differently depending on the mode of operation.

In DCM the current will cross the threshold with a relatively low dI/dt. Once the threshold is crossed, IR1169 will turn off gate and the current will start flowing again thru the body diode, causing the V_{DS} voltage to jump negative. Depending on the amount of residual current, V_{DS} may trigger once again the turn on threshold: for this reason V_{TH2} is blanked for a certain amount of time (T_{BLANK}) after V_{TH1} has been triggered.

The blanking time is internally set. As soon as V_{DS} crosses the positive threshold V_{TH3} the blanking time is terminated and the IC is ready for next conduction cycle.

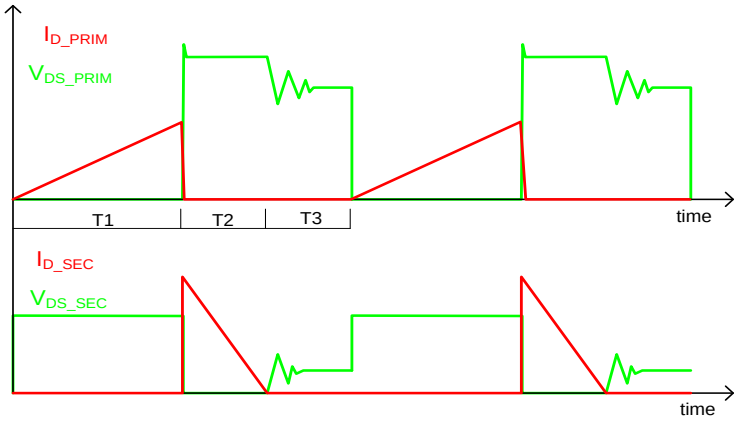


Figure 2: Flyback primary and secondary currents and voltages for DCM mode

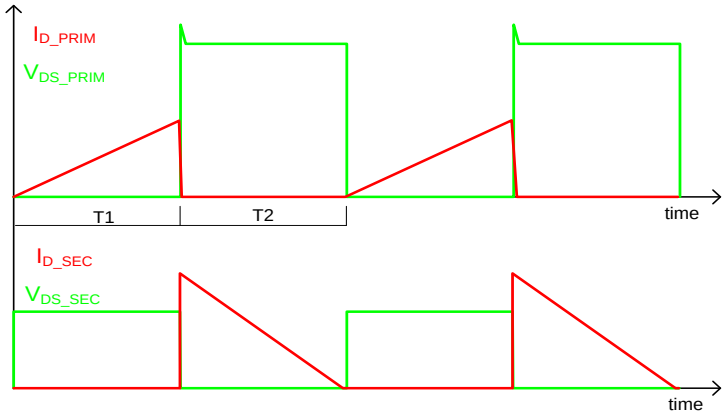


Figure 3: Flyback primary and secondary currents and voltages for CrCM mode

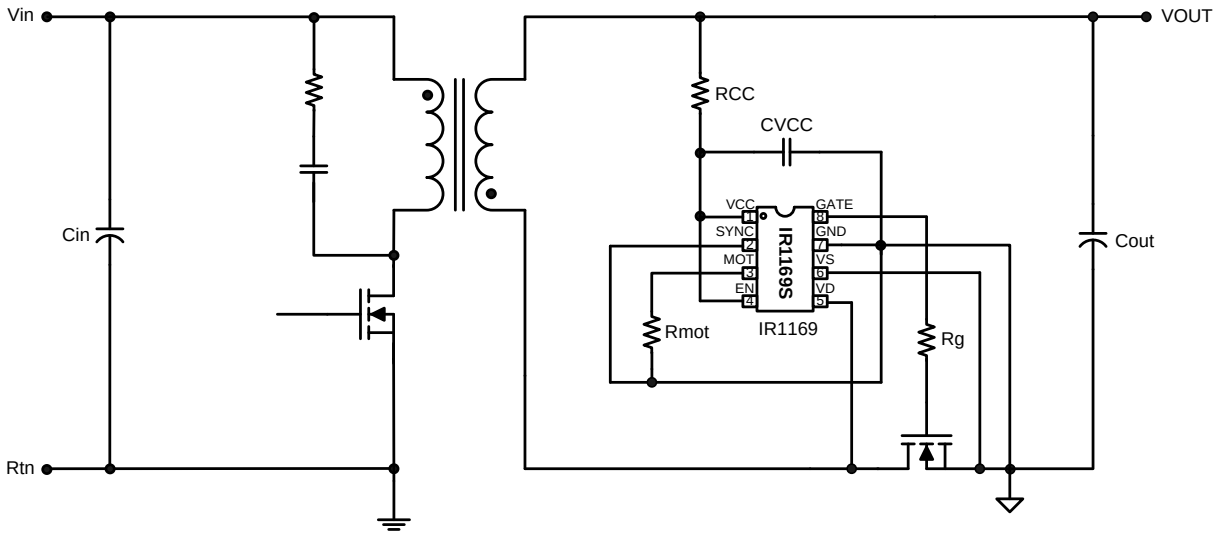


Figure 4: IR1169 schematic in DCM/CrCM mode Flyback

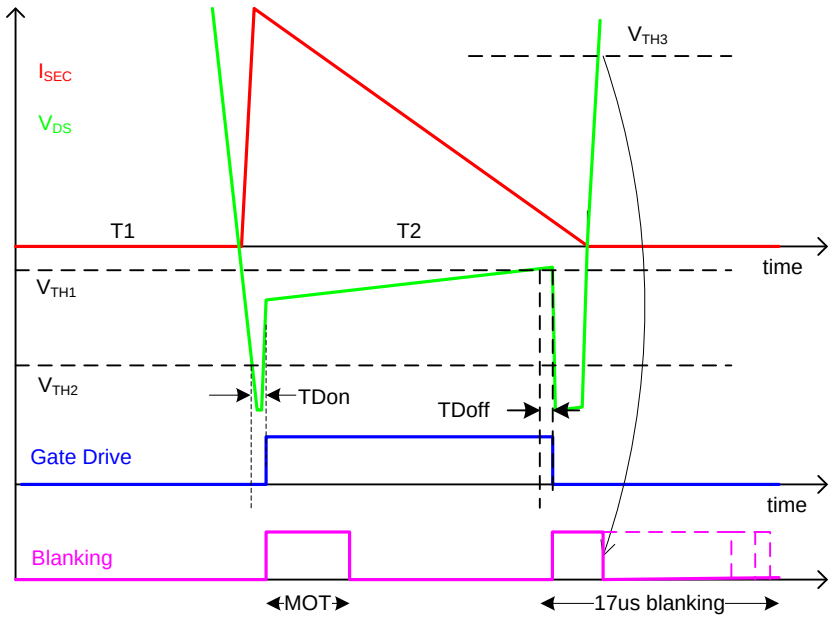


Figure 5: IR1169 DCM/CrCM Sync Rect operation (with SYNC connected to COM)

CCM Turn-off phase

In CCM mode the turn on phase is identical to DCM or CrCM and therefore won't be repeated here.

The turn off transition is much steeper and dI/dt involved is much higher (Figure 6). If the SR controller wait for the primary switch to turn back on and turn the gate off according to the FET current crossing V_{TH1}, it has high chance to get reverse current in the SR MOSFET. A predictable turn-off prior to the primary turn-on is necessary. A decoupling and isolation capacitor can be used to couple the primary gate signal to IR1169 SYNC pin and turn-off the SR MOSFET prior to the current slope goes to negative. Some turn-on delay to the primary MOSFET can guarantee no shoot through between the primary and secondary.

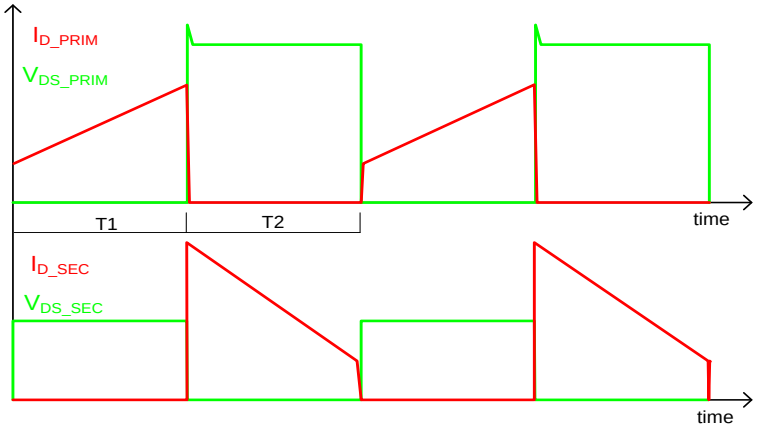


Figure 6: Primary and secondary currents and voltages for CCM mode

In CCM application the connection of IR1169 is recommended as shown in Figure 7.

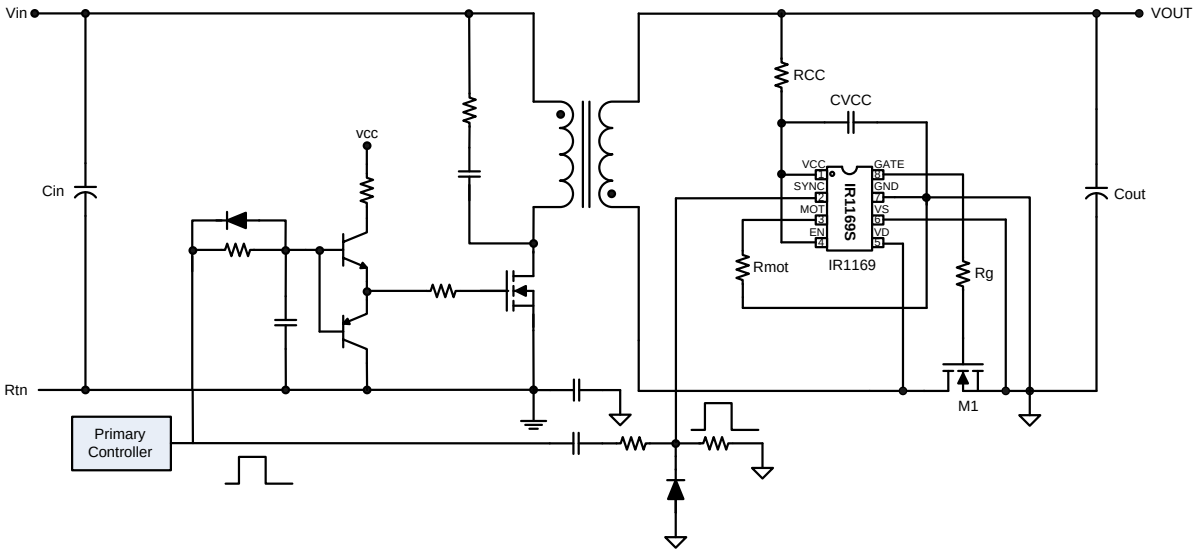


Figure 7: IR1169 schematic in CCM mode Flyback

IR1169 is designed to directly take the control information from primary side with capacitor coupling. A high voltage, low capacitance capacitor is used to send the primary gate driver signal to the SYNC pin. To have the circuit work properly, a Y cap is required between primary ground and secondary ground. No pulse transformer is required for the SYNC function, helps saving cost and PCB area.

The turn-off phase with SYNC control is shown in Figure 8.
In this case a blanking period is not applied; SYNC logic high will reset blanking time.

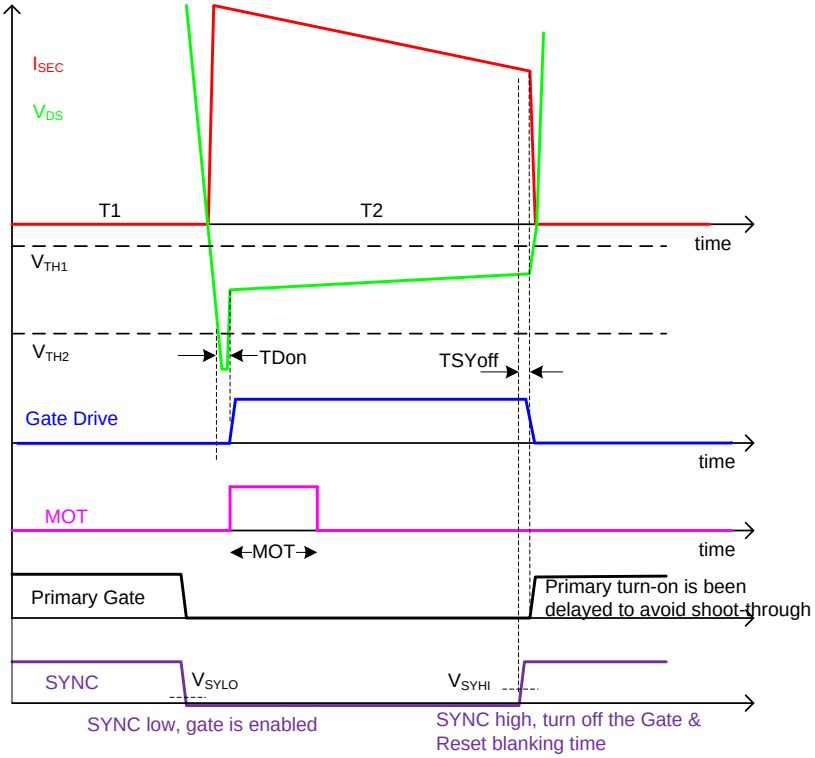


Figure 8: Secondary side CCM operation

Forward Application

The typical forward schematic with IR1169 is shown in Figure 9. The operation waveform of secondary Sync Rect circuit in Forward is similar to the CCM operation of Flyback.

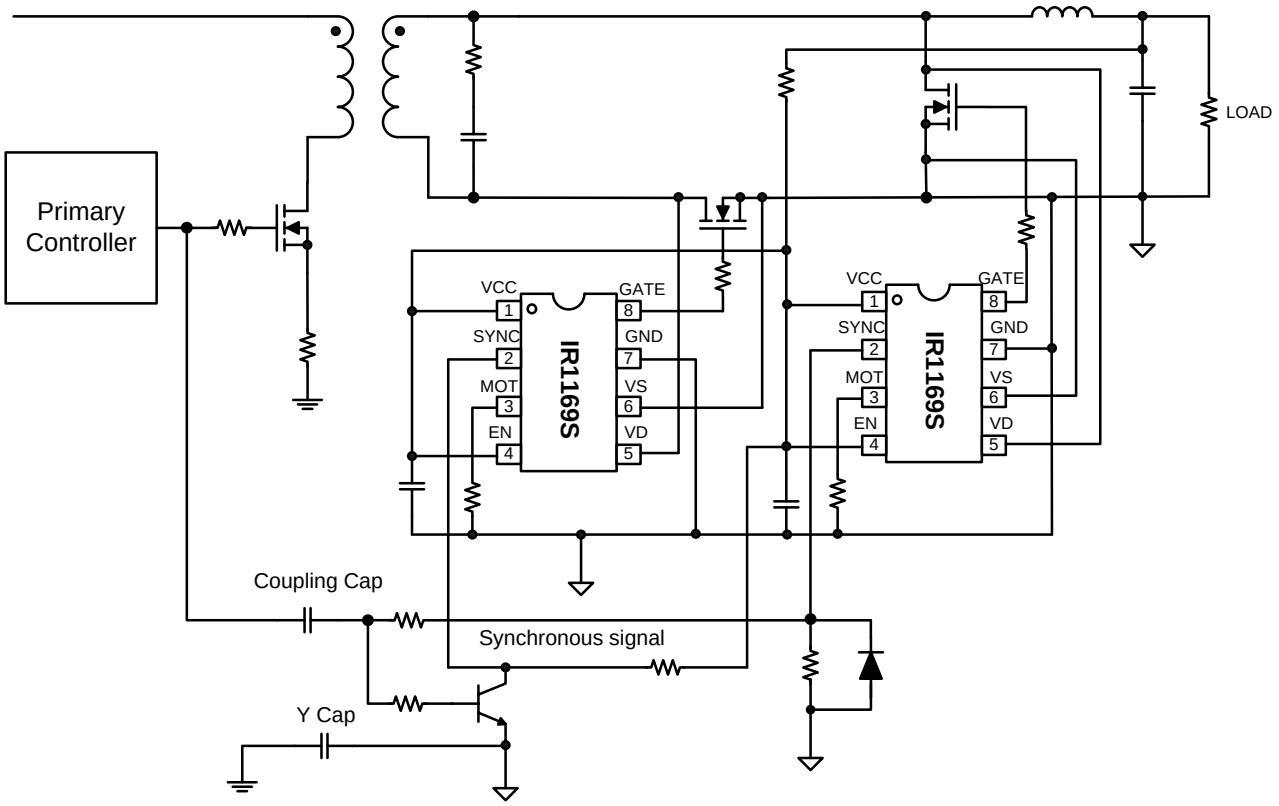


Figure 9: Forward application circuit

Resonant Half-Bridge Application

The typical application circuit of IR1169 in LLC half-bridge is shown in Figure 10.

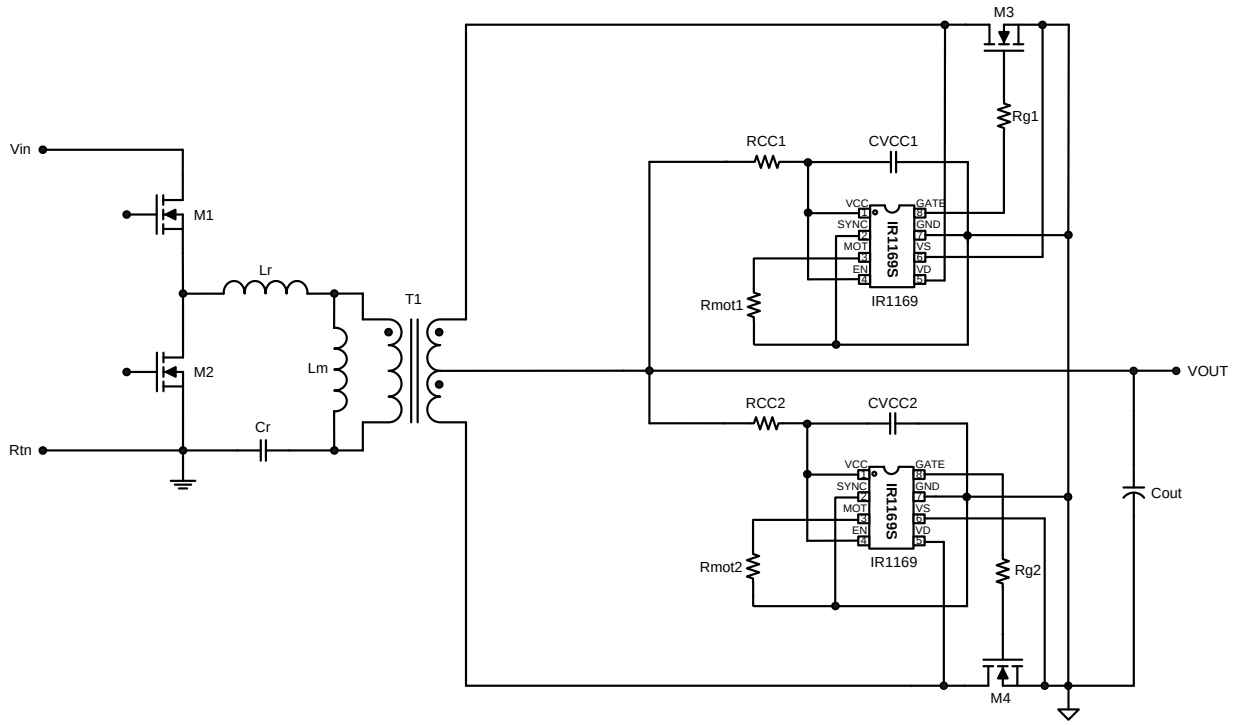


Figure 10: Resonant half-bridge application circuit

The SYNC pin can be tied to COM in LLC converter. The turn-on phase and turn-off phase is similar to Flyback converter except the current shape is sinusoid. The typical operation waveform can be found below.

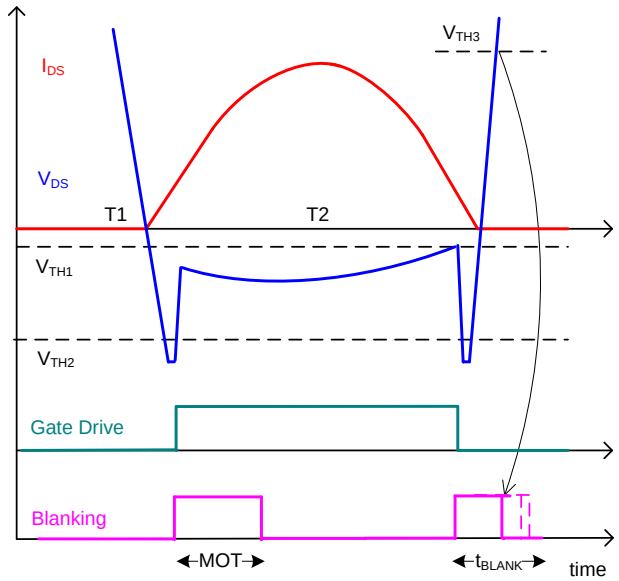


Figure 11: Resonant half-bridge operation waveform (with SYNC connected to GND)

The SYNC pin also can be connected to a control signal for special turn-on and/or turn-off control. Figure 12 is an example where the SYNC function is used to put some delay to the turn-on phase.

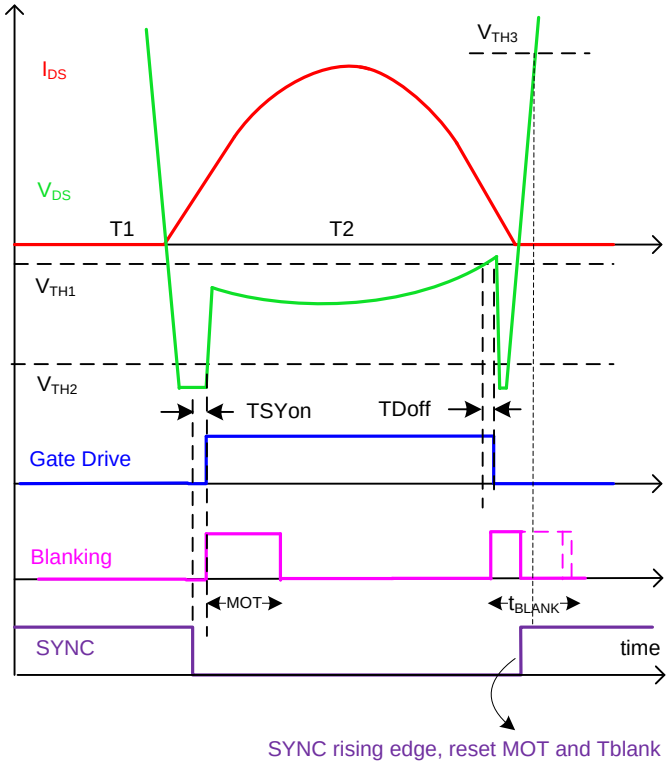


Figure 12: Resonant half-bridge with SYNC control

MOT Protection Mode

The MOT protection prevents reverse current in SR MOSFET. This function works in all three topologies. Figure 13 is an example in Flyback converter.

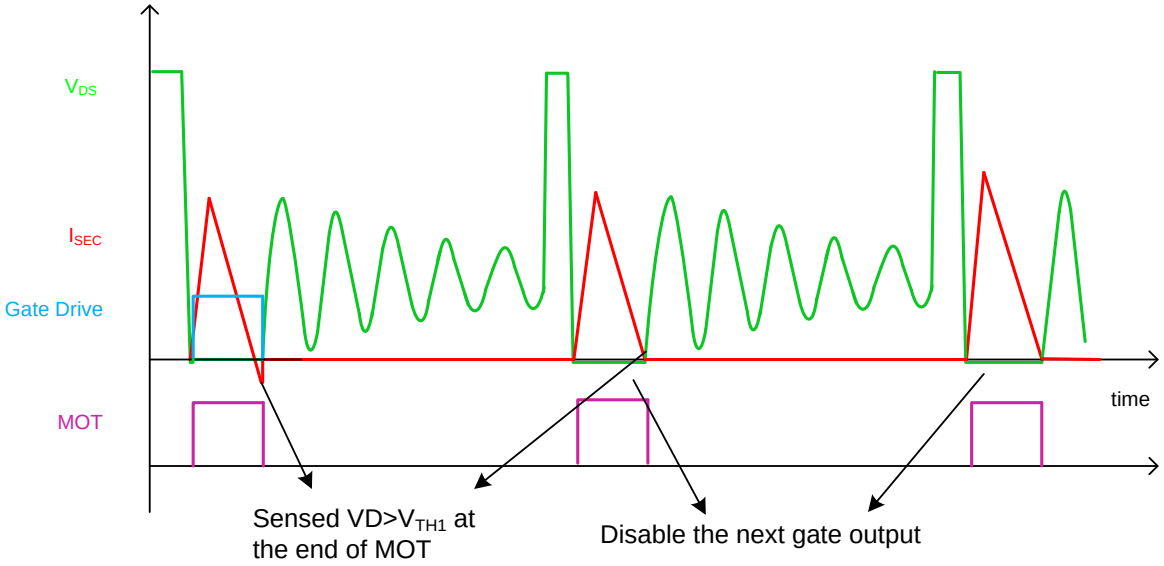


Figure 13: MOT Protection Mode

SYNC Reset Function

The SYNC pin resets MOT and Blanking time when SYNC switches from low to high. This function is useful for very low output voltage condition (such as overload or short circuit) where the VD voltage is too low to reach Vth3 threshold to reset the timers.

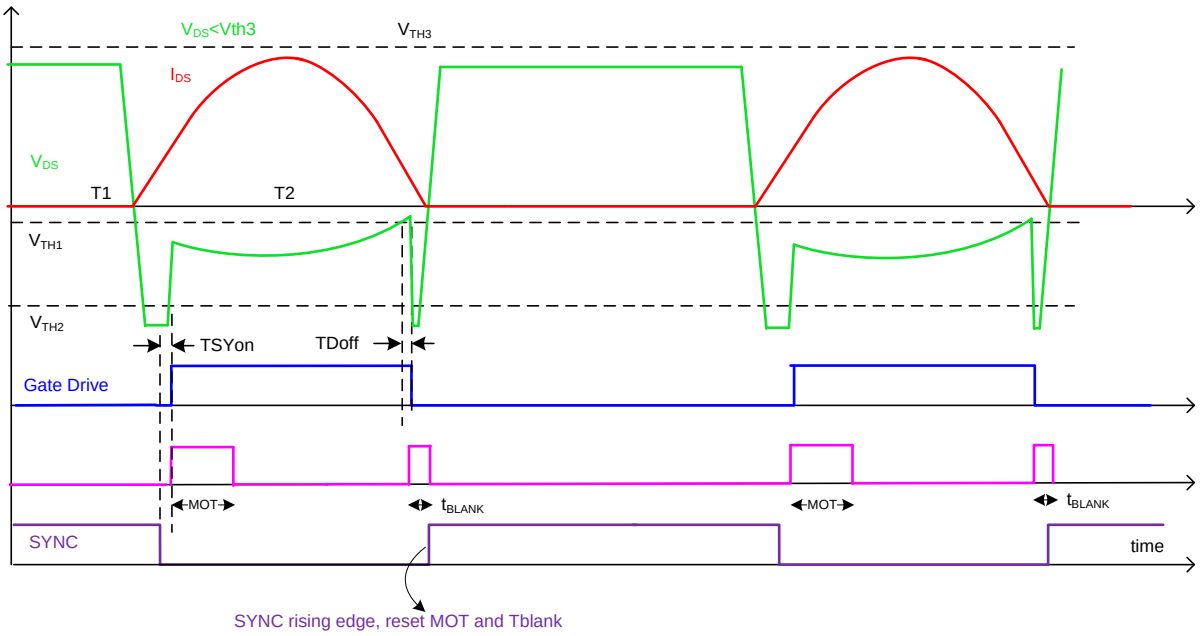


Figure 14: Reset by SYNC when VD<Vth3

General Timing Waveform

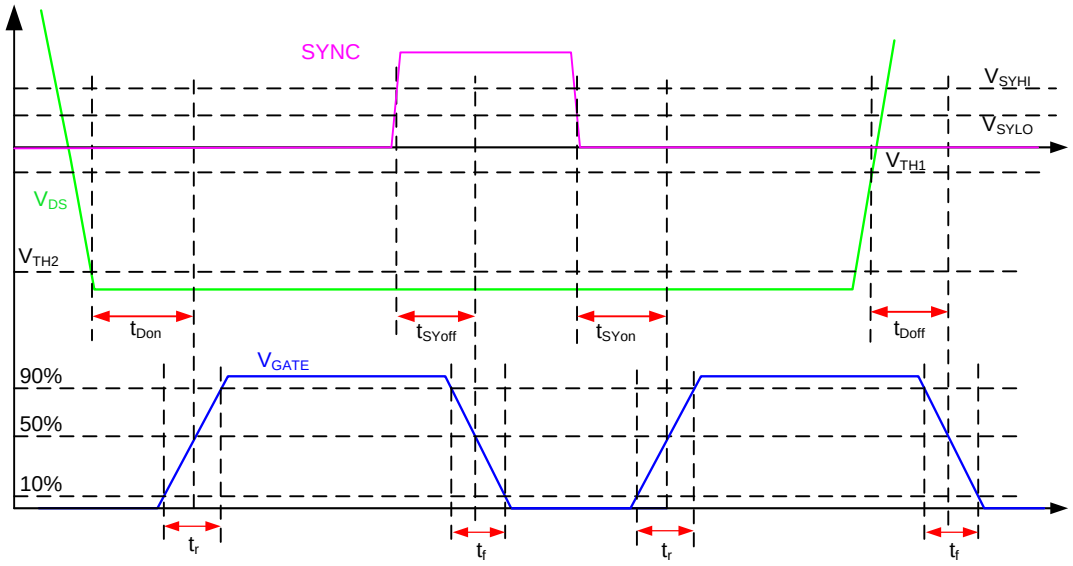


Figure 15A: Timing waveform

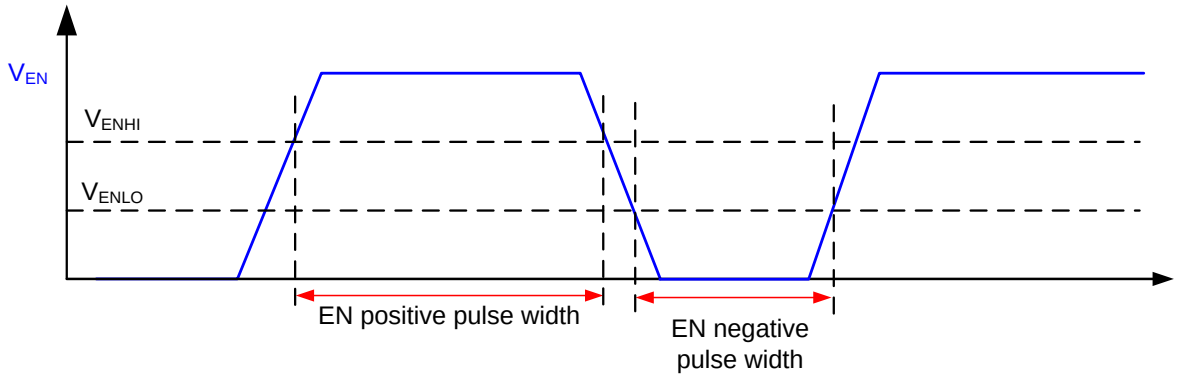


Figure 15B: Enable timing waveform

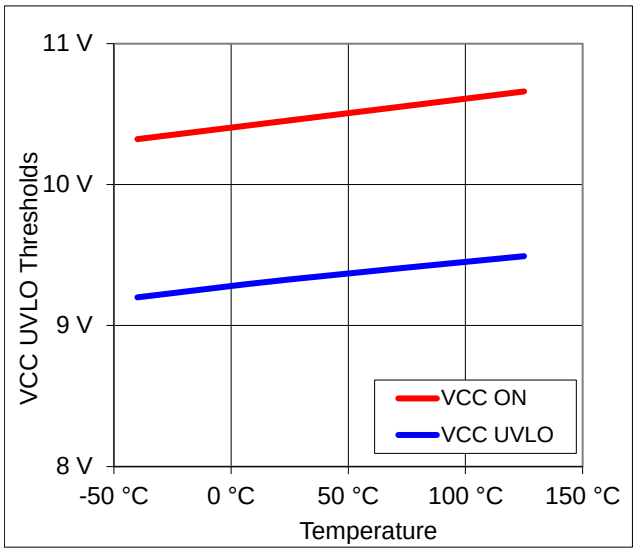


Figure 16: Undervoltage Lockout vs. Temperature

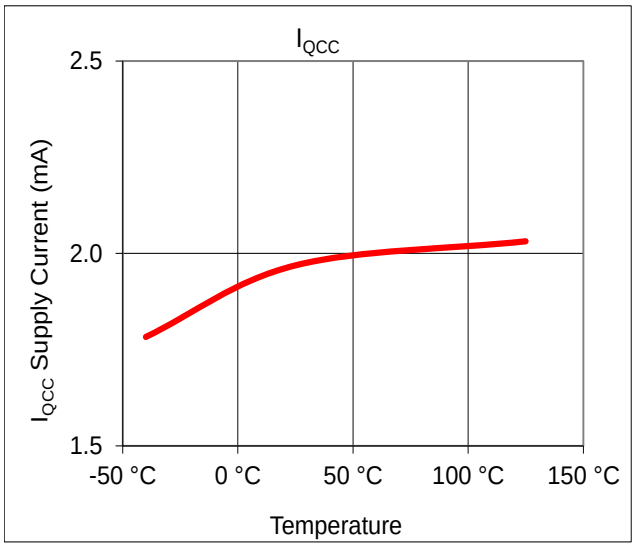


Figure 17: Icc Quiescent Current vs. Temperature

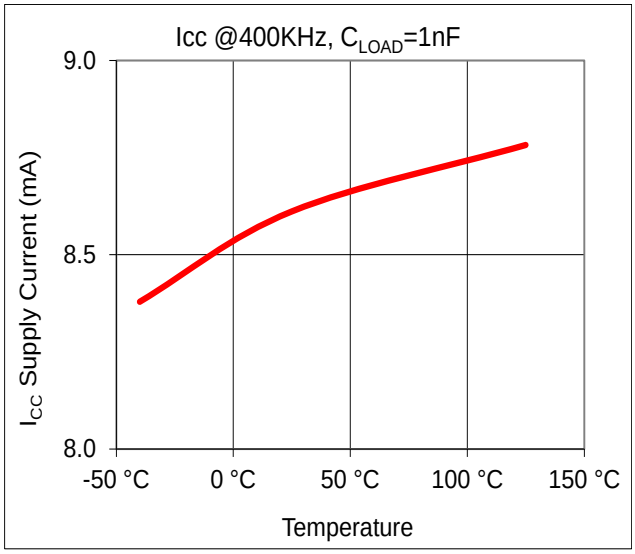


Figure 18: Icc Supply Currrent @1nF Load vs. Temperature

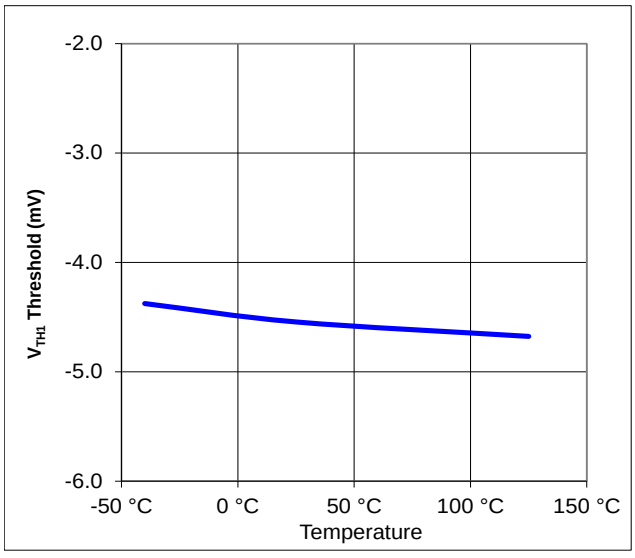


Figure 19: V_{TH1} vs. Temperature

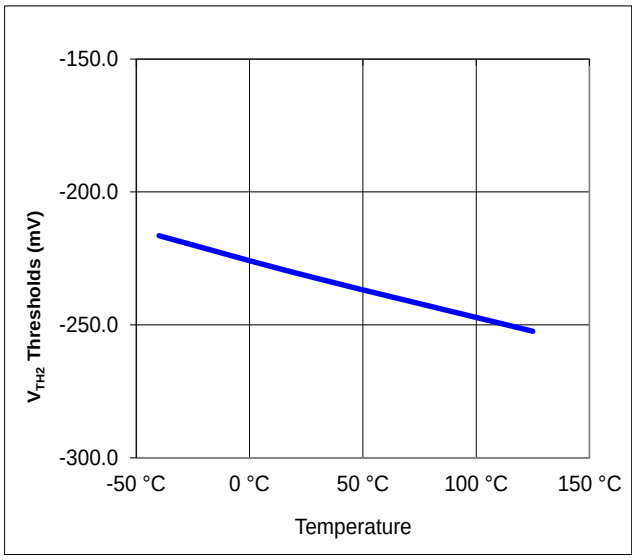


Figure 20: V_{TH2} vs. Temperature

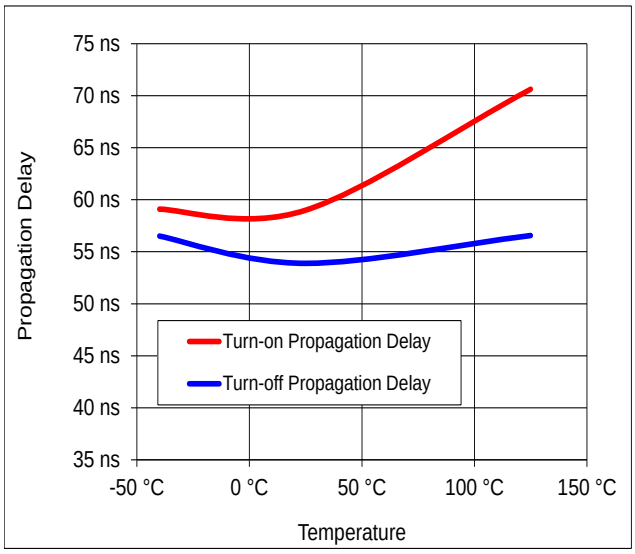


Figure 21: Turn-on and Turn-off Propagation Delay vs. Temperature

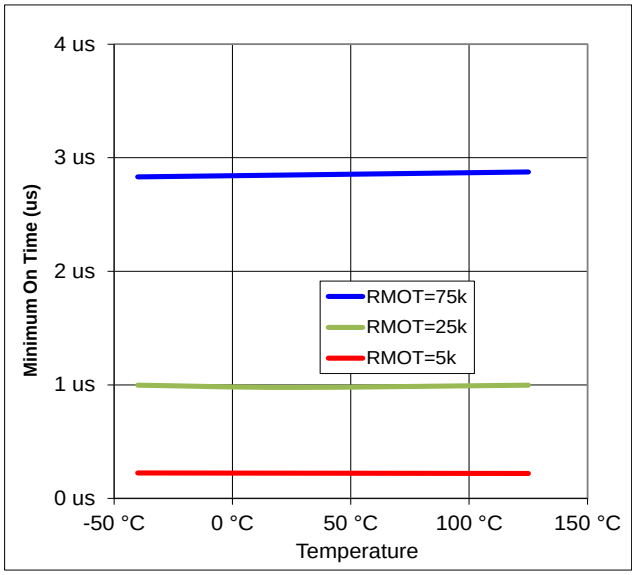


Figure 22: MOT vs Temperature

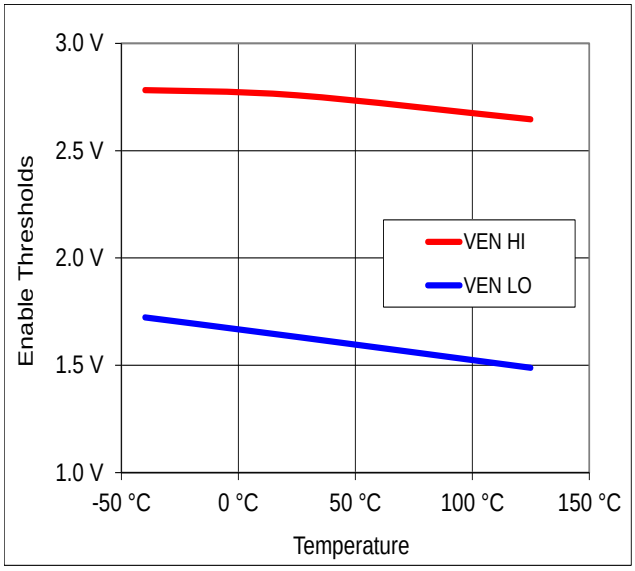


Figure 23: Enable Threshold vs. Temperature

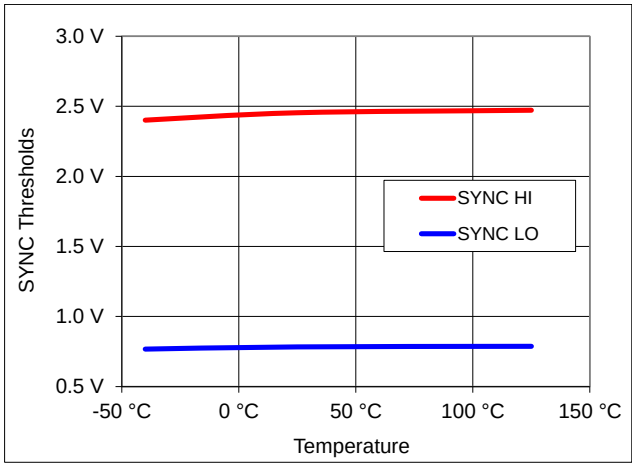


Figure 24: SYNC Thresholds vs. Temperature

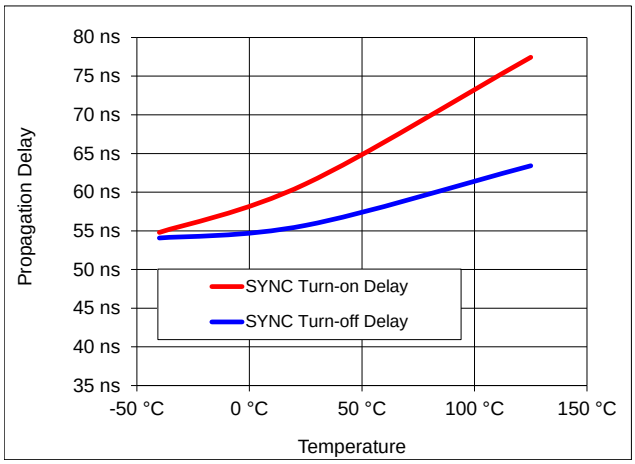


Figure 25: SYNC Turn-on and Turn-off Propagation Delay vs. Temperature

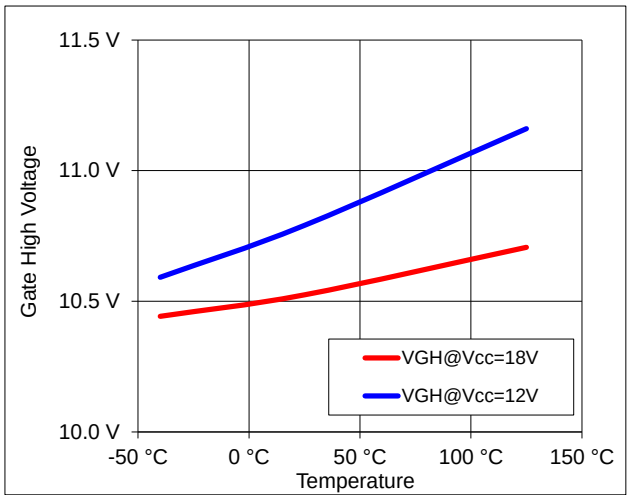


Figure 26: Gate Clamping Voltage vs. Temperature

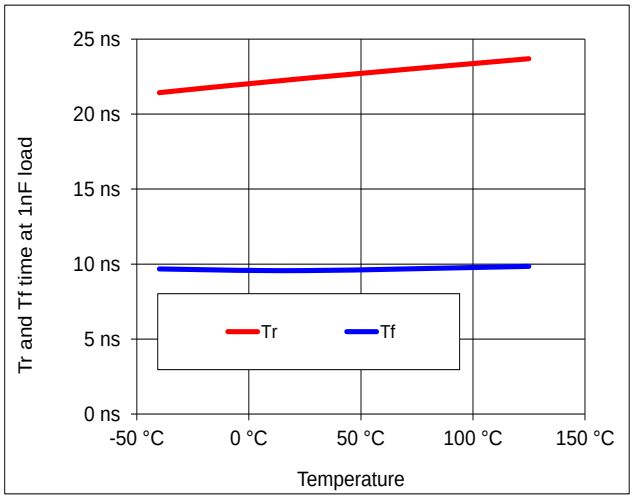
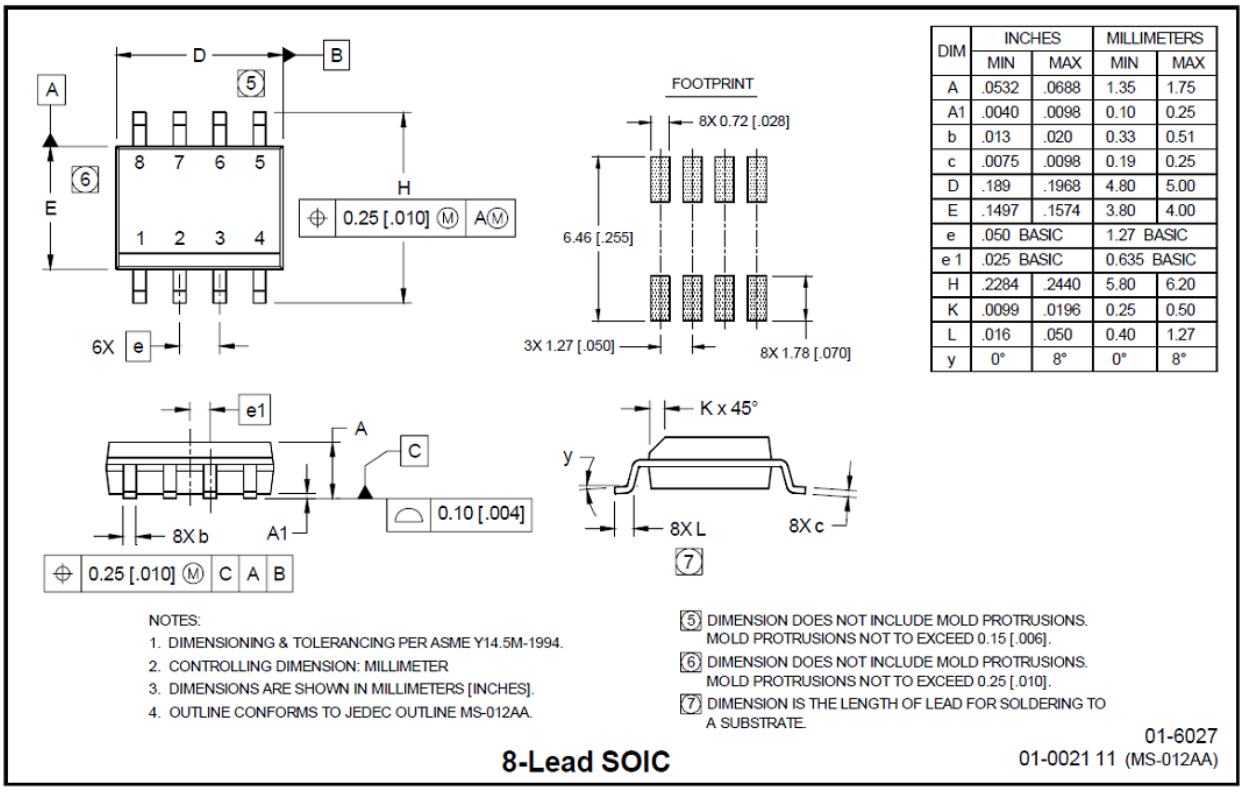


Figure 27: Rise and Fall time vs. Temperature

Package Details: SOIC8N



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

5 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].

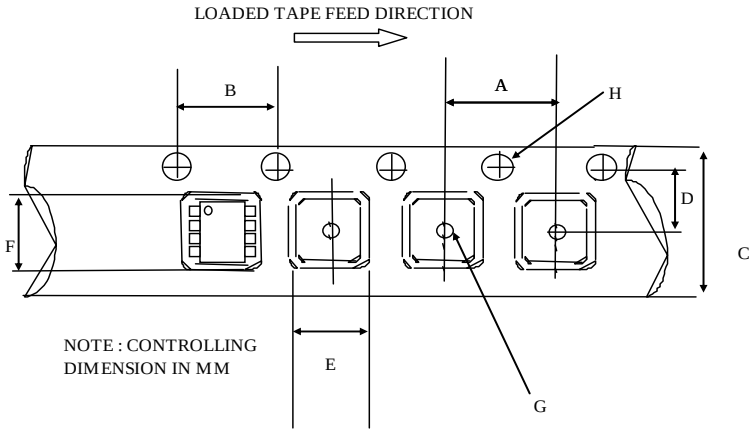
6 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].

7 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

01-6027
01-0021 11 (MS-012AA)

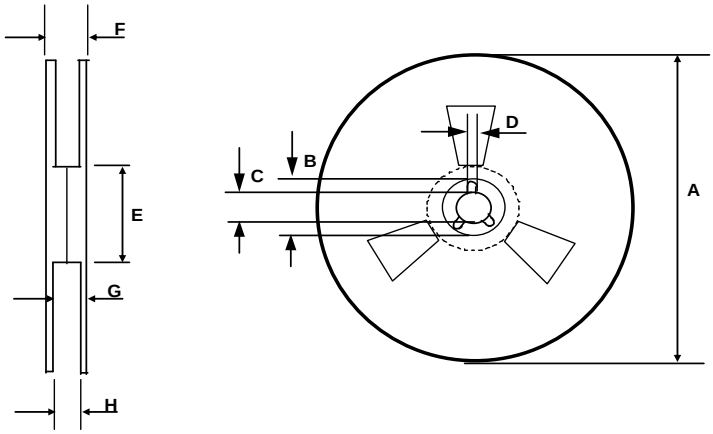
8-Lead SOIC

Tape and Reel Details: SOIC8N



CARRIER TAPE DIMENSION FOR 8SOICN

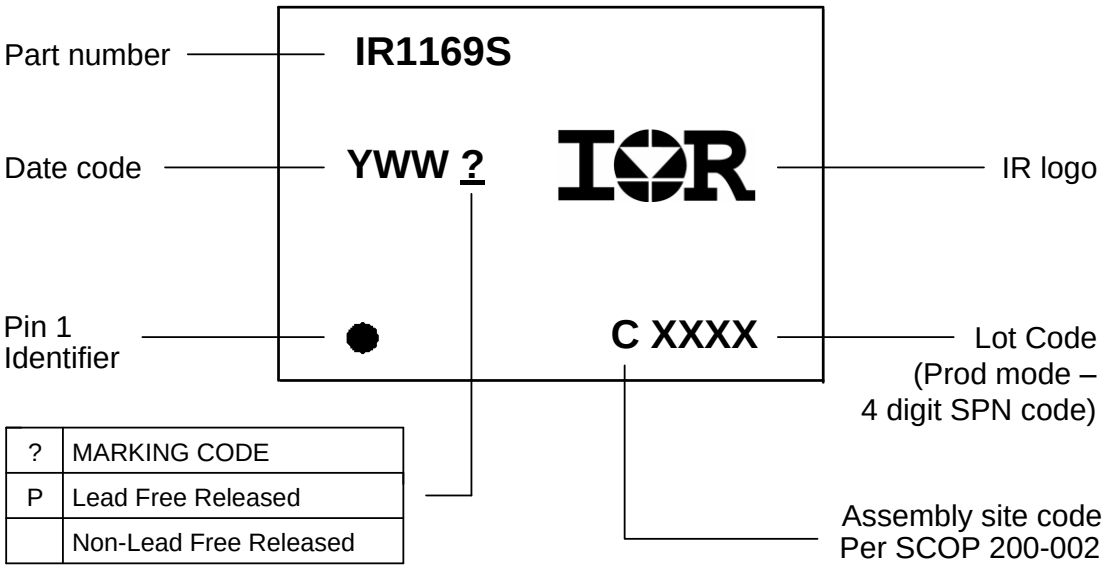
Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

Part Marking Information



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Released

Qualification Information†

Qualification Level		Industrial††	
		Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.	
Moisture Sensitivity Level		SOIC8N	MSL2††† 260°C (per IPC/JEDEC J-STD-020)
ESD	Machine Model	Class A (per JEDEC standard JESD22-A115)	
	Human Body Model	Class 1C (per EIA/JEDEC standard EIA/JESD22-A114)	
IC Latch-Up Test		Class I, Level A (per JESD78)	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

For technical support, please contact IR's Technical Assistance Center
http://www.irf.com/technical-info/

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