ispGDX2™ Family

High Performance Interfacing and Switching

Includes High-Performance, Low-Cost "E-Series"

September 2005 **Data Sheet**

Features

■ High Performance Bus Switching

- High bandwidth
  - Up to 12.8 Gbps (SERDES)
  - Up to 38 Gbps (without SERDES)
- Up to 16 (15x10) FIFOs for data buffering
- High speed performance
  - f_{MAX} = 360MHz
  - t_{PD} = 3.0ns
  - t_{CO} = 2.9ns
  - t_S = 2.0ns
- Built-in programmable control logic capability
- I/O intensive: 64 to 256 I/Os
- Expanded MUX capability up to 188:1 MUX

■ sysCLOCK™ PLL

- Frequency synthesis and skew management
- Clock multiply and divide capability
- Clock shifting up to +/-2.35ns in 335ps steps
- Up to four PLLs

■ sysIO™ Interfacing

- LVCMOS 1.8, 2.5, 3.3 and LVTTL support for standard board interfaces
- SSTL 2/3 Class I and II support
- HSTL Class I, III and IV support
- GTL+, PCI-X for bus interfaces
- LVPECL, LVDS and Bus LVDS differential support
- Hot socketing
- Programmable drive strength

■ Two Options Available

- High-performance sysHSI (standard part number)
- Low-cost, no sysHSI ("E-Series")

■ sysHSI Blocks Provide up to 16 High-speed Channels

- Serializer/de-serializer (SERDES) included
- Clock Data Recovery (CDR) built in
- 800 Mbps per channel
- LVDS differential support
- 10B/12B support
  - Encoding / decoding
  - Bit alignment
  - Symbol alignment
- 8B/10B support
  - Bit alignment
  - Symbol alignment
- Source Synchronous support

■ Flexible Programming and Testing

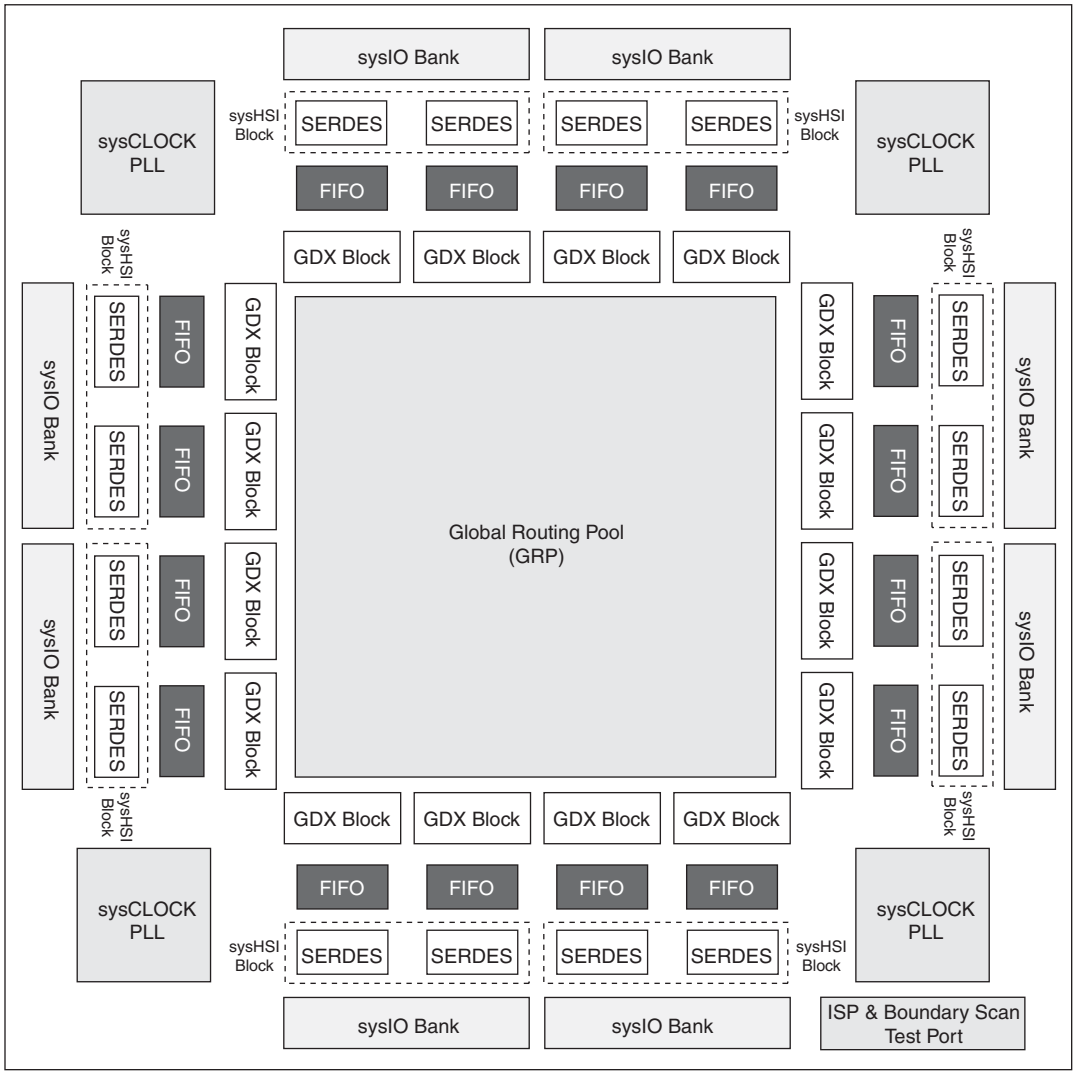
- IEEE 1532 compliant In-System Programmability (ISP™)
- Boundary scan test through IEEE 1149.1 interface
- 3.3V, 2.5V or 1.8V power supplies
- 5V tolerant I/O for LVCMOS 3.3 and LVTTL interfaces

Table 1. ispGDX2 Family Selection Guide

		ispGDX2-64/E	ispGDX2-128/E	ispGDX2-256/E
I/Os		64	128	256
GDX Blocks		4	8	16
t_{PD}		3.0ns	3.2ns	3.5ns
t_S		2.0ns	2.0ns	2.0ns
t_{CO}		2.9ns	3.1ns	3.2ns
f_{MAX} (Toggle)		360MHz	330MHz	300MHz
Max Bandwidth	SERDES[1, 2]	3.2Gbps	6.4Gbps	12.8Gbps
	Without SERDES[3]	11Gbps	21Gbps	38Gbps
sysHSI Channels[2]		4	8	16
LVDS/Bus LVDS (Pairs)		32	64	128
PLLs		2	2	4
Package		100-ball fpBGA	208-ball fpBGA	484-ball fpBGA

1. Max number of SERDES channels per device * 800Mbps
2. "E-Series" does not support sysHSI.
3. f_{MAX} (Toggle) * maximum I/Os divided by 2.

Figure 1. ispGDX2 Block Diagram (256-I/O Device)



Introduction

The ispGDX2™ family is Lattice's second generation in-system programmable generic digital crosspoint switch for high speed bus switching and interface applications.

The ispGDX2 family is available in two options. The standard device supports sysHSI capability for ultra fast serial communications while the lower-cost "E-series" supports the same high-performance FPGA fabric without the sysHSI Block.

This family of switches combines a flexible switching architecture with advanced sysIO interfaces including high performance sysHSI Blocks, and sysCLOCK PLLs to meet the needs of the today's high-speed systems. Through a muliplexer-intensive architecture, the ispGDX2 facilitates a variety of common switching functions.

The availability of on-chip control logic further enhances the power of these devices. A high-performance solution, the family supports bandwidth up to 38Gbps.

Every device in the family has a number of PLLs to provide the system designer with the ability to generate multiple clocks and manage clock skews in their systems.

The sysIO interfaces provide system-level performance and integration. These I/Os support various modes of LVCMOS/LVTTL and support popular high-speed standard interfaces such as GTL+, PCI-X, HSTL, SSTL, LVDS and Bus-LVDS. The sysHSI Blocks further extend this capability by providing high speed serial data transfer capability.

Devices in the family can operate at 3.3V, 2.5V or 1.8V core voltages and can be programmed in-system via an IEEE 1149.1 interface that is compliant with the IEEE 1532 standard. Voltages required for the I/O buffers are independent of the core voltage supply. This further enhances the flexibility of this family in system designs.

Typical applications for the ispGDX2 include multi-port multi-processor interfaces, wide data and address bus multiplexing, programmable control signal routing and programmable bus interfaces. Table 1 shows the members of the ispGDX2 family and their key features.

Architecture

The ispGDX2 devices consist of GDX Blocks interconnected by a Global Routing Pool (GRP). Signals interface with the external system via sysIO banks. In addition, each GDX Block is associated with a FIFO and a sysHSI Block to facilitate the transfer of data on- and off-chip. Figure 1 shows the ispGDX2 block diagram. Each GDX Block can be individually configured in one of four modes:

- Basic (No FIFO or SERDES)
- FIFO Only
- SERDES Only
- SERDES and FIFO

Each sysIO bank has its own I/O power supply and reference voltage. Designers can use any output standard within a bank that is compatible with the power supply. Any input standard may be used, providing it is compatible with the reference voltage. The banks are independent.

Global Routing Pool (GRP)

The ispGDX2 architecture is organized into GDX Blocks, which are connected via a Global Routing Pool. The innovative GRP is optimized for routability, flexibility and speed. All the signals enter via the GDX Block. The block supplies these either directly or in registered form to the GRP. The GRP routes the signals to different blocks, and provides separate data and control routing. The data path is optimized to achieve faster speed and routing flexibility for nibble oriented signals. The control routing is optimized to provide high-speed bit oriented routing of control signals.

There are some restrictions on the allocation of pins for optimal bus routing. These restrictions are considered by the software in the allocation of pins.

GDX Block

The blocks are organized in a “block” (nibble) manner, with each GDX Block providing data flow and control logic for 16 I/O buffers. The data flow is organized as four nibbles, each nibble containing four Multiplexer Register Blocks (MRBs). Data for the MRBs is provided from 64 lines from the GRP. Figure 2 illustrates the groups of signals going into and out of a GDX Block.

Control signals for the MRBs are provided from the Control Array. The Control Array receives the 32 signals from the GRP and generates 16 control signals: eight MUX Select, four Clock/Clock Enable, two Set/Reset and two Output Enable. Each nibble is controlled via two MUX select signals. The remaining control signals go to all the MRBs.

Besides the control signals from the Control Array, the following global signals are available to the MRBs in each GDX Block: four Clock/Clock Enable, one reset/preset, one power-on reset, two of four MUX select (two of two in 64 I/O), four Output Enable (two in 64 I/O) and Test Out Enable (TOE).

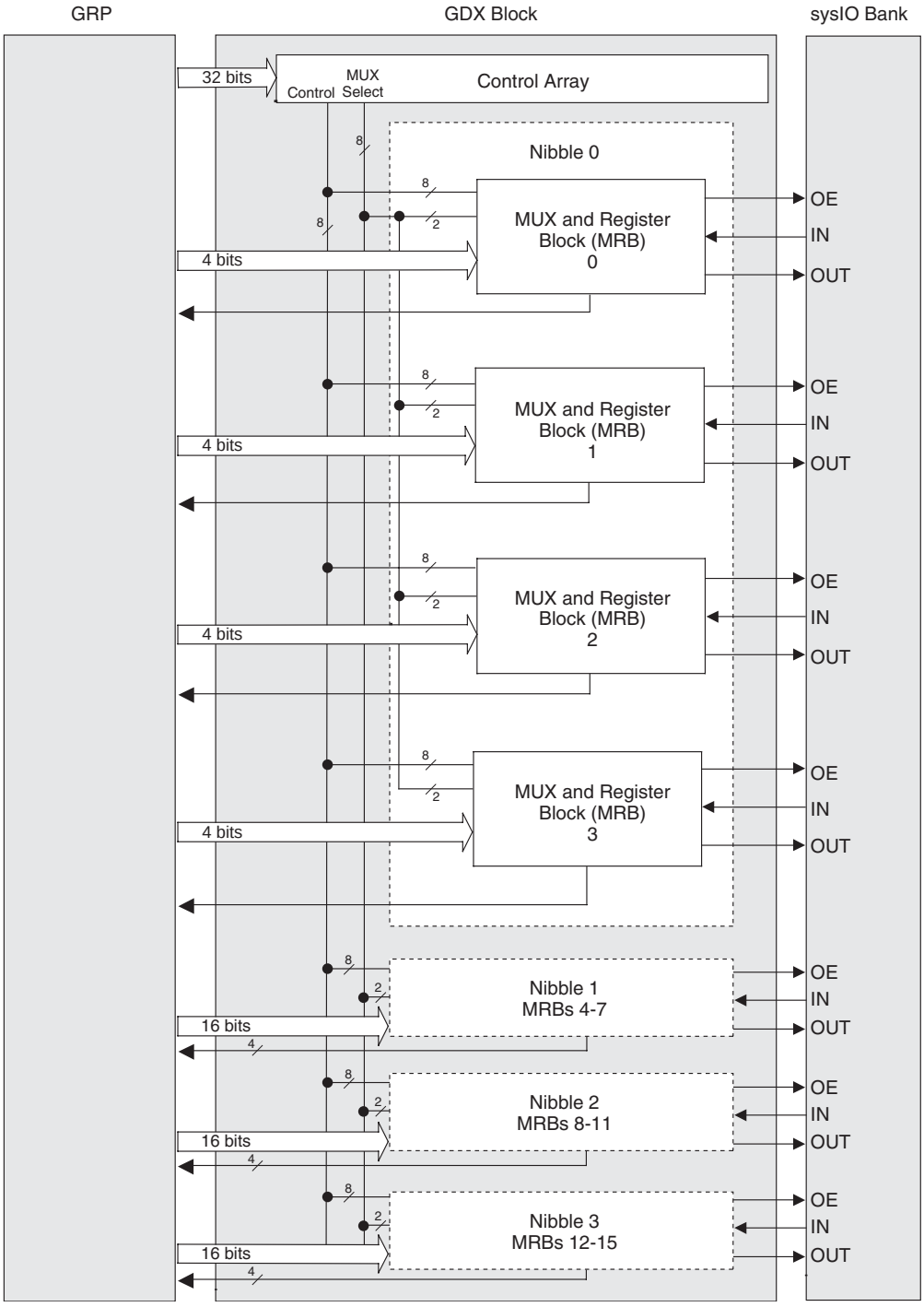
MUX and Register Block (MRB)

Every MRB Block has a 4:1 MUX (I/O MUX) and a set of three registers which are connected to the I/O buffers, FIFO and sysHSI Blocks. Multiple MRBs can be combined to form large multiplexers as described below. Figure 3 shows the structure of the MRB.

Each of the three registers in the MRB can be configured as edge-triggered D-type flip-flop or as a level sensitive latch. One register operates on the input data, the other output data and the last register synchronizes the output enable function. The input and output data signals can bypass each of their registers. The polarity of the data out and output enable signals can be selected.

The Output and OE register share the same clock and clock enable signals. The Input register has a separate clock and clock enable. The initialization signals of each register can be independently configured as Set or Reset. These registers have programmable polarity control for Clock, Clock Enable and Set/Reset. The output enable register input can be set either by one of the two output enables generated locally from the Control Array or from one of the four (two in 64 I/O) Global OE enable pins. In addition to the local clock and clock enable signals, each MRB has access to Global Clock, Clock Enable, Reset and TOE nets.

Figure 2. GDX Block



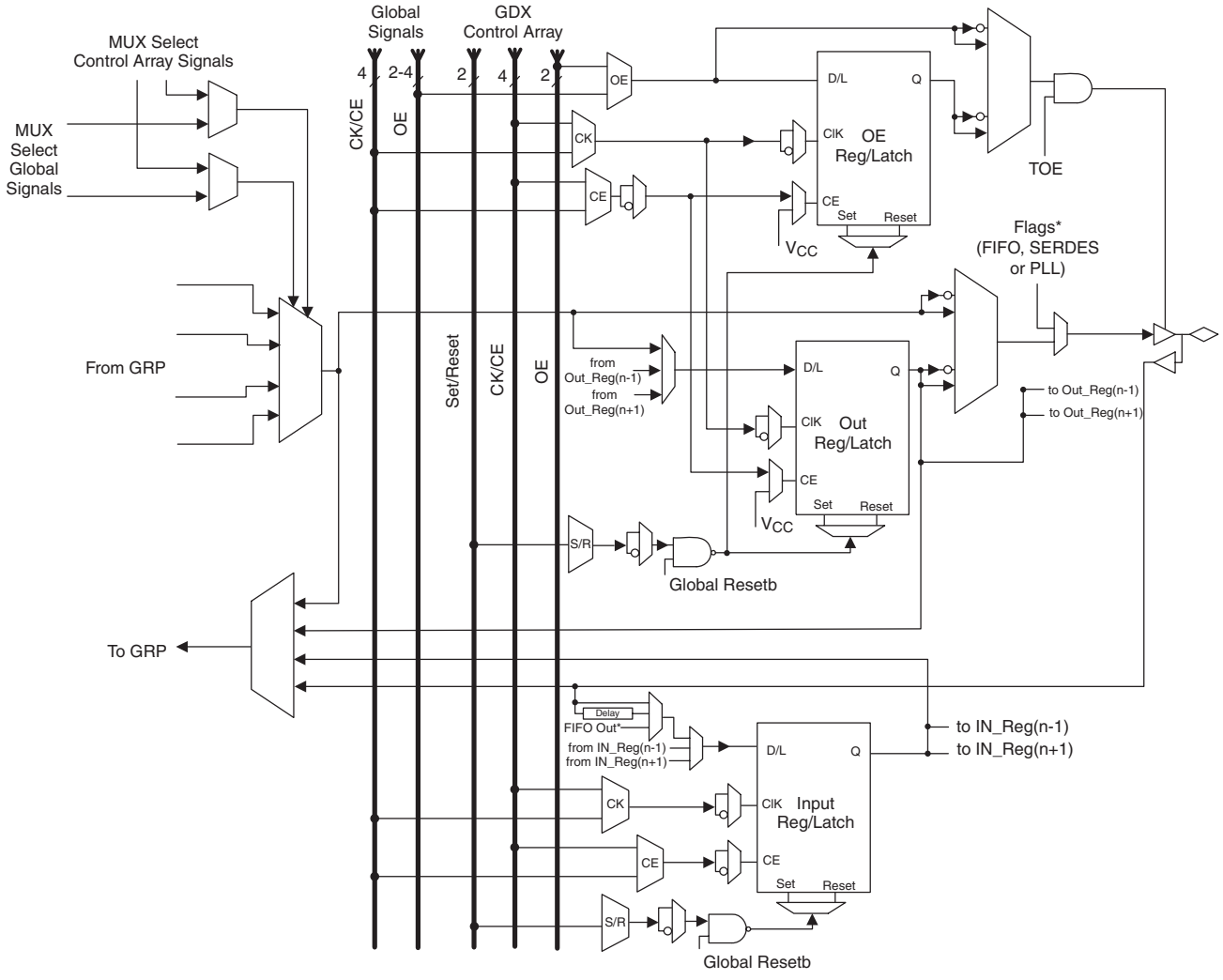
The output register of the MRB has a built-in bi-directional shift register capability. Each output register corresponding to MRB "n", receives data output from its two adjacent MRBs, MRB (n-1) and MRB (n+1), to provide shift register capability. Like the output register, each input register of the MRB has built-in shift register capability. Each input register can receive data from its two adjacent MRB input registers, to provide bi-directional shift register capability. The chaining crosses GDX Block boundaries. The chain of input registers and the chain of output registers can be combined as one shift register via the GRP.

The four data inputs to the 4:1 MUX come from the GRP. The output of this MUX connects to the output register. A fast feedback path from the MUX to the GRP allows wider MUXes to be built. Table 2 summarizes the various MUX sizes and delay levels.

Table 2. MUX Size Versus Internal Delay

MUX Sizes	Levels of Internal GRP Delays
4:1	One Level
Up to 16:1	Two Levels
Up to 64:1	Three Levels
Up to 188:1 (with ispGDX2-256)	Four Levels

Figure 3. ispGDX2 Family MRB

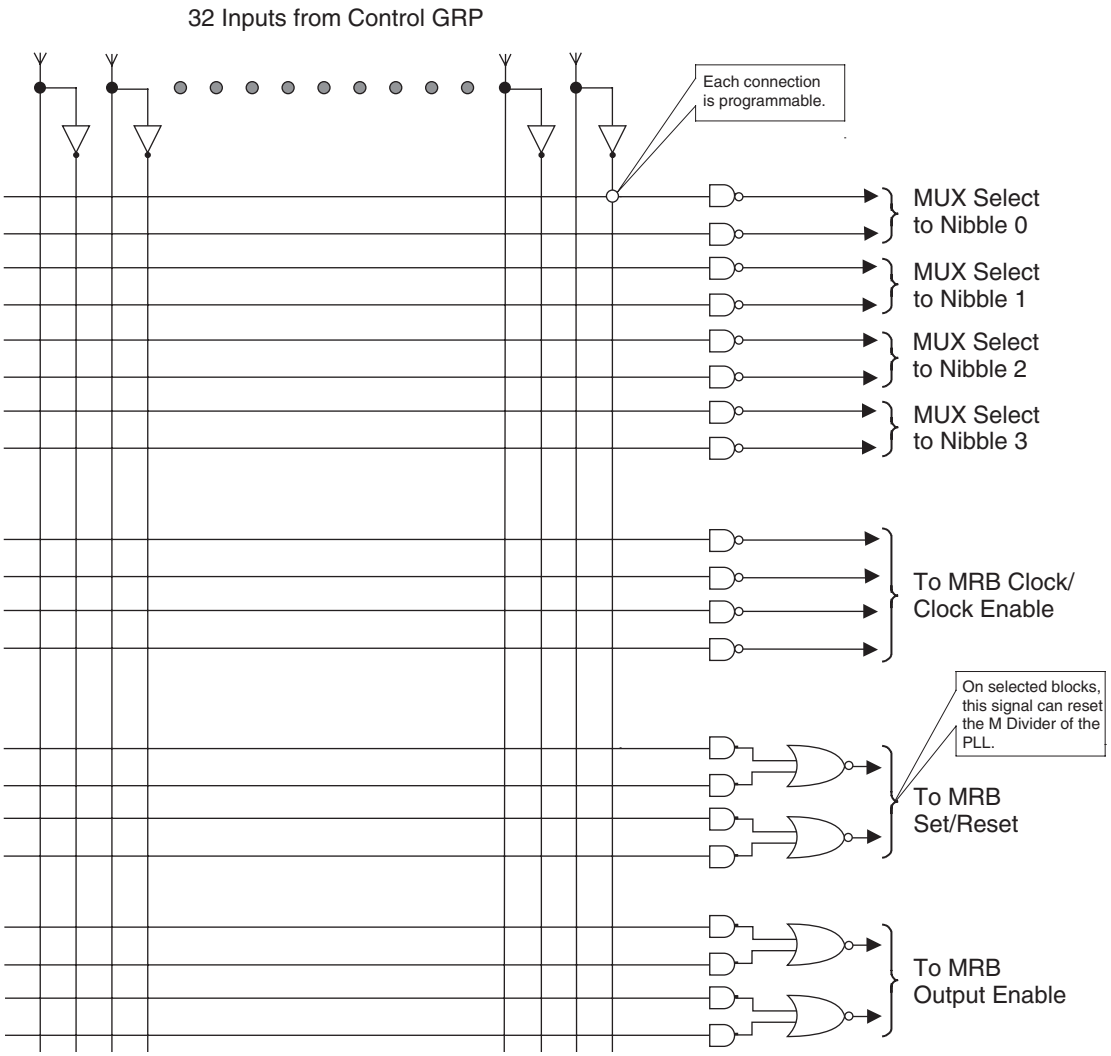


*Selected MRBs see Logic Signal Connection Table for details

Control Array

The control array generates control signals for the 16 MRBs within a GDX Block. The true and complement forms of 32 inputs from the GRP are available in the control array. The 20 NAND terms can use any or all of these inputs to form the control array outputs. Two AND terms are combined with a NOR term to form Set/Reset and OE signals. Figure 4 illustrates the control array.

Figure 4. ispGDX2 Family Control Array

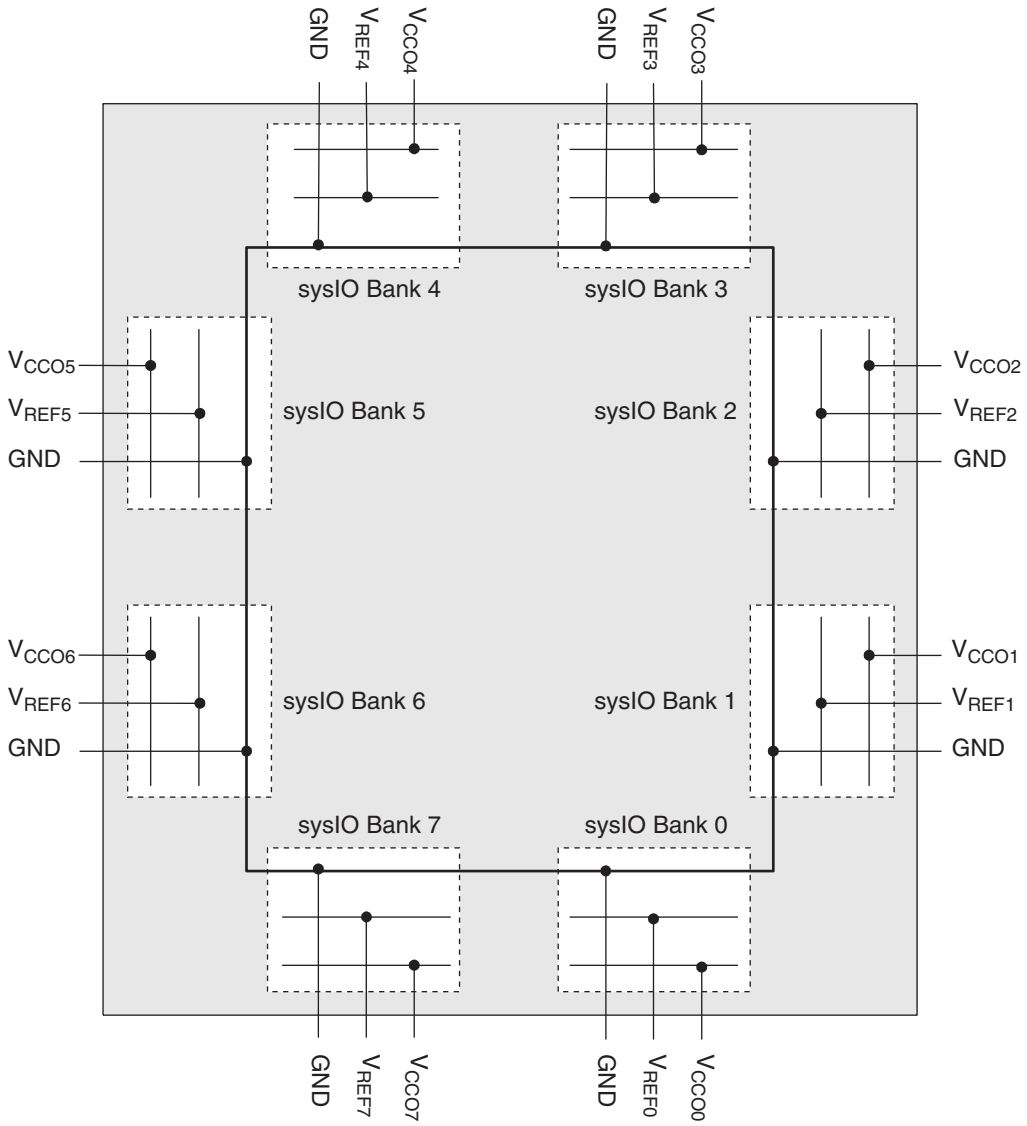


sysIO Banks

The inputs and outputs of ispGDX2 devices are divided into eight sysIO banks, where each bank is capable of supporting different I/O standards. The number of I/Os per bank is 32, 16 and 8 for the 256-, 128- and 64-I/O devices respectively. Each sysIO bank has its own I/O supply voltage (V_{CCO}) and reference voltage (V_{REF}), allowing each bank complete independence from the other banks. Each I/O within a bank can be individually configured to any standard consistent with the V_{CCO} and V_{REF} settings. Figure 5 shows the I/O banks for the ispGDX2-256 device.

The I/O of the ispGDX2 devices contain a programmable strength and slew rate tri-state output buffer, a programmable input buffer, a programmable pull-up resistor, a programmable pull-down resistor and a programmable bus-keeper latch. These programmable capabilities allow the support of a wide range of I/O standards.

Figure 5. ispGDX2-256 sysIO Banks



There are three classes of I/O interface standards implemented in the ispGDX2 devices. The first is the non-terminated, single-ended interface; it includes the 3.3V LVTTL standard along with the 1.8V, 2.5V and 3.3V LVCMOS interface standards. The slew rate and strength of these output buffers can be controlled individually. Additionally, PCI 3.3, PCI-X and AGP-1X are all subsets of this interface type. The second interface class implemented is the terminated, single-ended interface standard. This group of interfaces includes different versions of SSTL and HSTL interfaces along with CTT and GTL+. Use of these I/O interfaces requires an additional V_{REF} signal. At the system level, a termination voltage, V_{TT}, is also required. Typically, an output will be terminated to V_{TT} at the receiving end of the transmission line it is driving. The final types of interfaces implemented are the differential standards LVPECL, LVDS and Bus LVDS. Table 3 shows the I/O standards supported by the ispGDX2 devices along with nominal V_{CCO}, V_{REF} and V_{TT}.

The ispGDX2 family also features 5V tolerant I/O. I/O banks with V_{CCO} = 3.3V may have inputs driven to a maximum of 5.5V for easy interfacing with legacy systems. Up to 64 I/O pins per device may be driven by 5V inputs.

Table 3. ispGDX2 Supported I/O Standards

sysIO Standard	Nominal V_{CCO}	Nominal V_{REF}	Nominal V_{TT}
LVCMOS 3.3	3.3V	—	—
LVCMOS 2.5	2.5V	—	—
LVCMOS 1.8	1.8V	—	—
LVTTL	3.3V	—	—
PCI 3.3	3.3V	—	—
PCI -X	3.3V	—	—
AGP-1X	3.3V	—	—
SSTL3 class I & II	3.3V	1.5V	1.5V
SSTL2 class I & II	2.5V	1.25V	1.25V
CTT 3.3	3.3V	1.5V	1.5V
CTT 2.5	2.5V	1.25V	1.25V
HSTL class I	1.5V	0.75V	0.75V
HSTL class III	1.5V	0.9V	0.75V
HSTL class IV	1.5V	0.9V	1.5V
GTL+	1.8/2.5/3.3V	1.0V	1.5V
LVPECL[1, 2, 3]	3.3V	—	—
LVDS	2.5/3.3V	—	—
Bus-LVDS	2.5/3.3V	—	—

1. LVPECL drivers require three resistor pack (see Figure 17).
2. Depending on the driving LVPECL output specification, GDX2 LVPECL input driver may require terminating resistors.
3. For additional information on LVPECL refer to Lattice technical note number TN1000, *sysIO Design and Usage Guidelines.*

The dedicated inputs support a subset of the sysIO standards indicated in Table 4. These inputs are associated with a bank consistent with their location.

Table 4. I/O Standards Supported by Dedicated Inputs

	LVCMOS	LVDS	All other ASIC I/Os
Global OE Pins	Yes	No	Yes[2]
Global MUX Select Pins	Yes	No	Yes[2]
Resetb	Yes	No	Yes[2]
Global Clock/Clock Enables	Yes	Yes	Yes[2]
ispJTAG™ Port	Yes[1]	No	No
TOE	Yes	No	No

1. LVCMOS as defined by the V_{CCJ} pin voltage.
2. No PCI clamp.

For more information on the sysIO capability, please refer to Lattice technical note number TN1000, *sysIO Design and Usage Guidelines.*

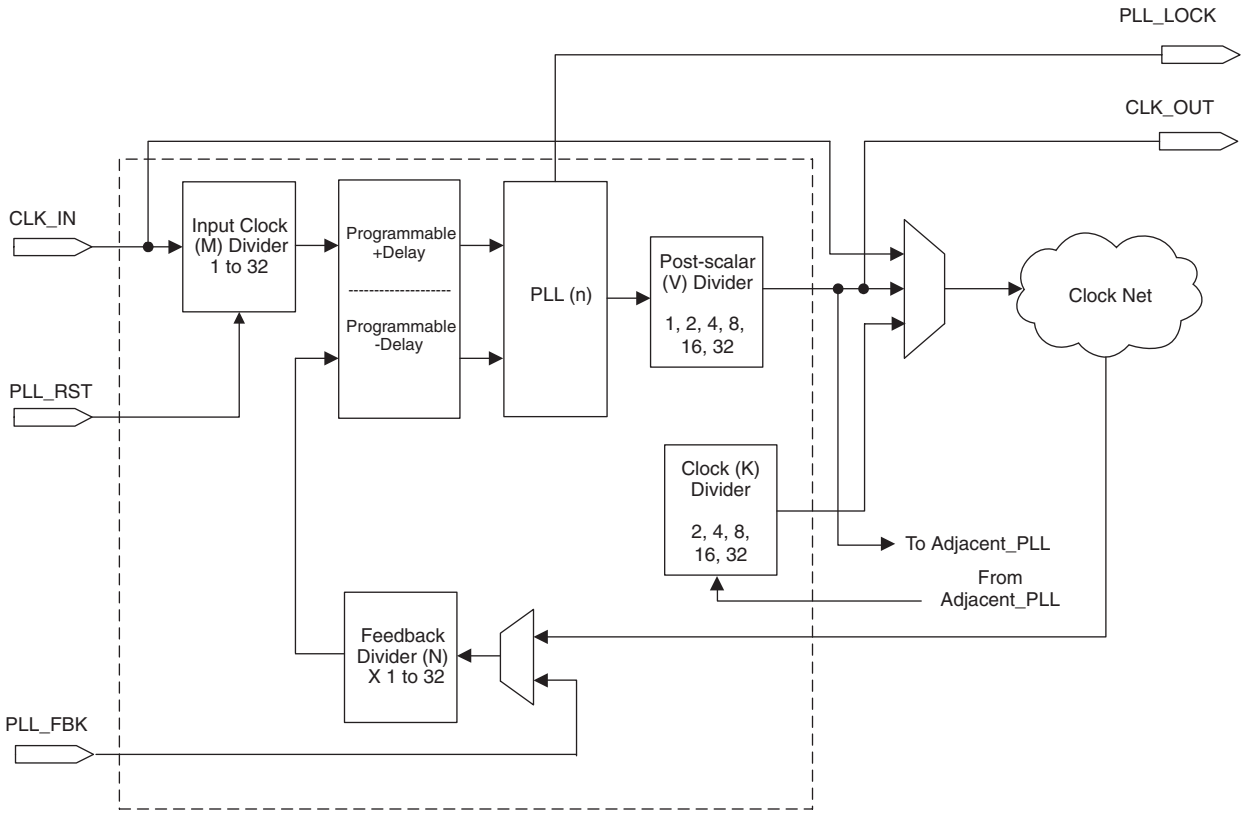
sysCLOCK PLL

The sysCLOCK PLL circuitry consists of Phase-Lock Loops (PLLs) along the various dividers and reset and feedback signals associated with the PLLs. This feature gives the user the ability to synthesize clock frequencies and generate multiple clock signals for routing within the device. Furthermore, it can generate clock signals that are deskewed either at the board level or the device level. Figure 6 shows the ispGDX2 PLL block diagram.

Each PLL has a set of PLL_RST, PLL_FBK and PLL_LOCK signals. In order to facilitate the multiply and divide capabilities of the PLL, each PLL has associated dividers. The M divider is used to divide the clock signal, while the

N divider is used to multiply the clock signal. The K divider is used to provide a divided clock frequency of the adjacent PLL. This output can be routed to the global clock net. The V divider is used to provide lower frequency output clocks, while maintaining a stable, high frequency output from the PLL's VCO circuit. The PLL also has a delay feature that allows the output clock to be advanced or delayed to improve set-up and clock-to-out times for better performance. For more information on the PLL, please refer to Lattice technical note number TN1003, *sysCLOCK PLL Design and Usage Guidelines*.

Figure 6. sysCLOCK PLL

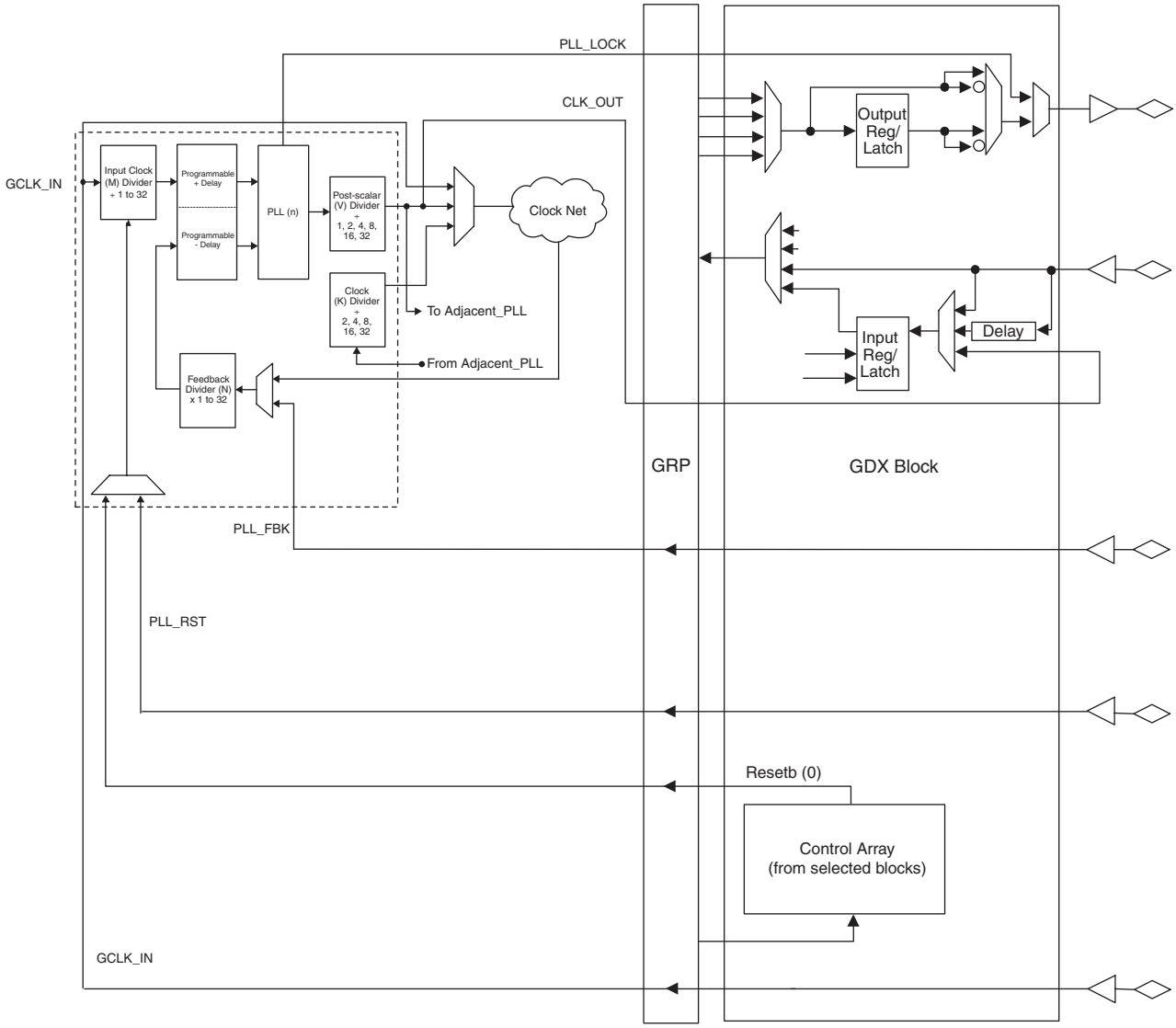


There are four global clock networks routed to each MRB block. These global clocks, CLK0-3, can either be generated by the PLL circuits or supplied externally. External clock pins can be configured as single-ended or differential (LVDS) input. Figure 7 illustrates how the sysCLOCK PLL inputs and outputs can be routed to the I/O pins or general routing. Figure 10 shows the clock network for the ispGDX2-256 and Figure 8 shows the clock networks for ispGDX2-128 and ispGDX2-64. The Reset (0) pin from the Control Array of selected GDX Blocks can be programmed to reset the M Divider of the PLLs. This provides a means for generating the reset signal internally. Table 5 details which GDX Block provides reset to the PLLs.

Table 5. Internal Reset Input of the PLL (M Divider)

	PLL0	PLL1	PLL2	PLL3
ispGDX2-256	GDX Block 5A	GDX Block 7B	GDX Block 1A	GDX Block 3B
ispGDX2-128	GDX Block 2A	—	GDX Block 0A	—
ispGDX2-64	GDX Block 0A	—	GDX Block 1B	—

Figure 7. I/O Pin Connection to the sysCLOCK PLL[1]



1. Some pins are shared. See Logic Signal Connections Table for details.

Figure 8. ispGDX2-64 CLOCK Network

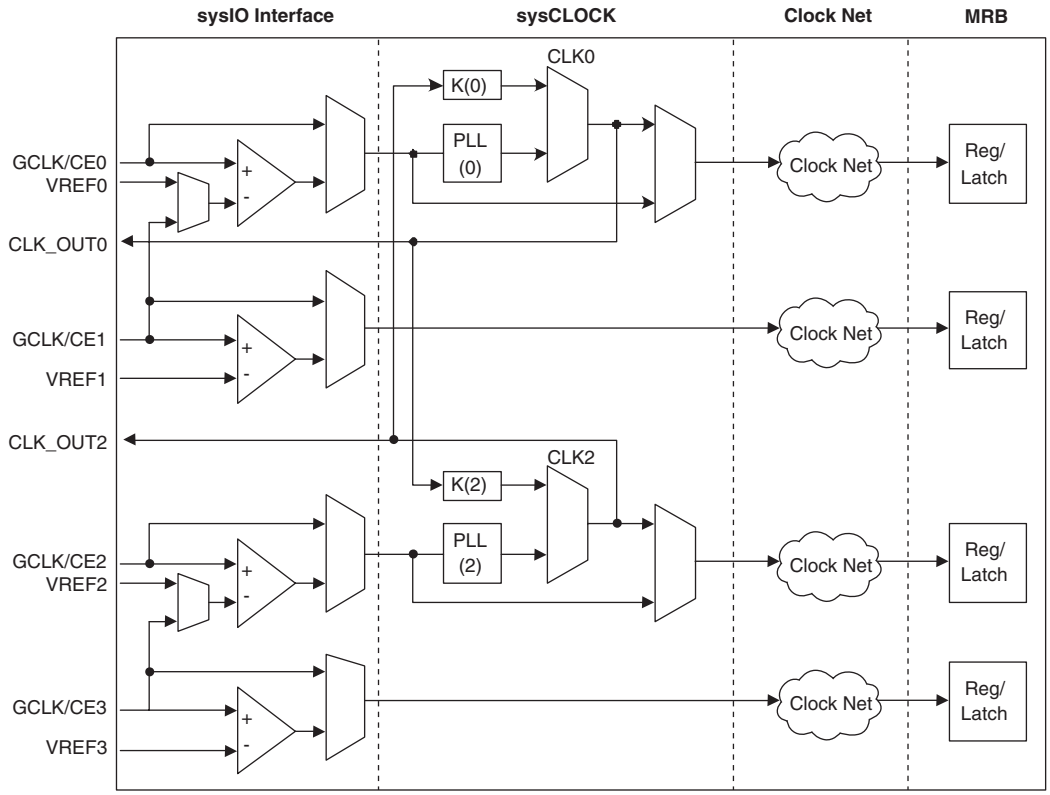


Figure 9. ispGDX2-128 CLOCK Network

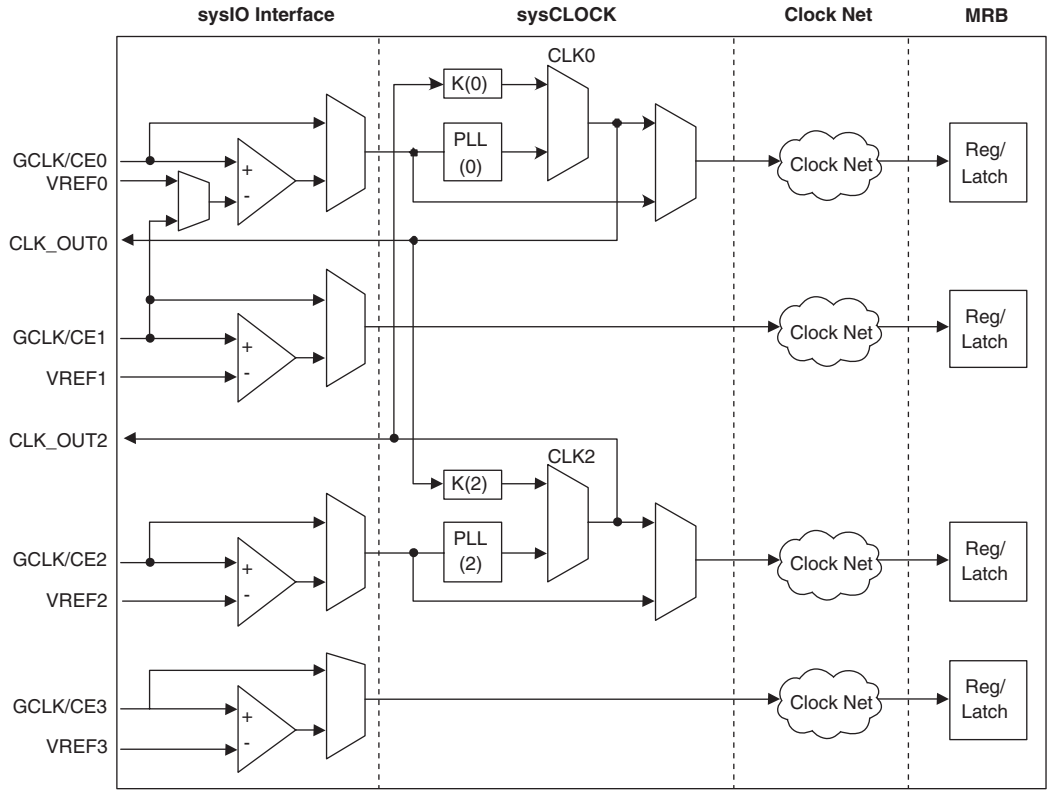
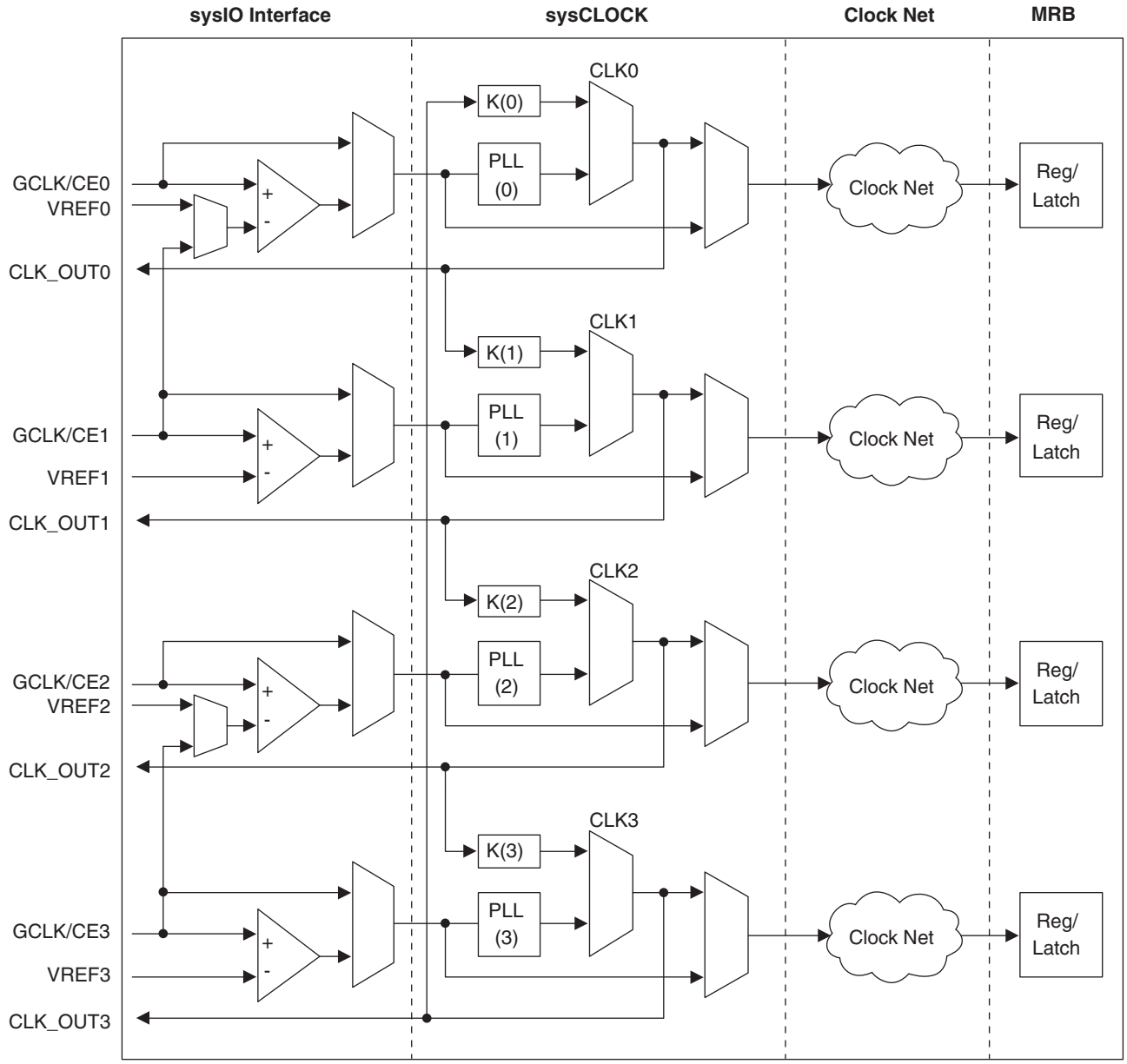


Figure 10. ispGDX2-256 CLOCK Network

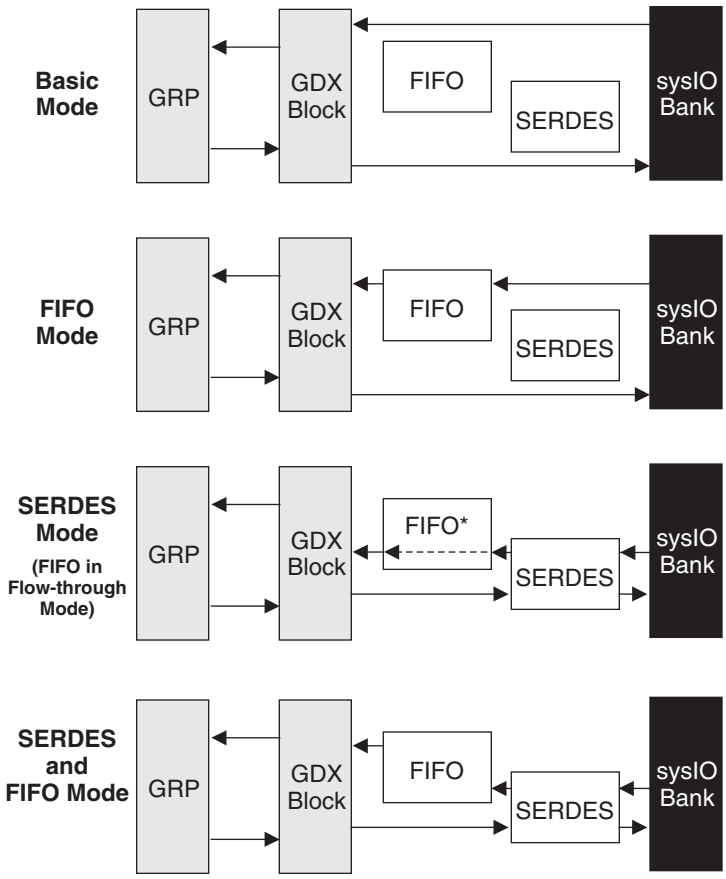


Operating Modes

All the GDX Blocks in the ispGDX2 family can be programmed in four modes: Basic, FIFO only, SERDES only, and FIFO with SERDES mode. In basic mode, the SERDES and FIFO are disabled and the MUX output of the MRB connects to the output register. Inputs are connected to the GRP via the MRB.

Figure 11 shows the four different operating modes. Precise detail of the FIFO and SERDES connections is provided in their respective sections.

Figure 11. Four Operating Modes of ispGDX2 Devices

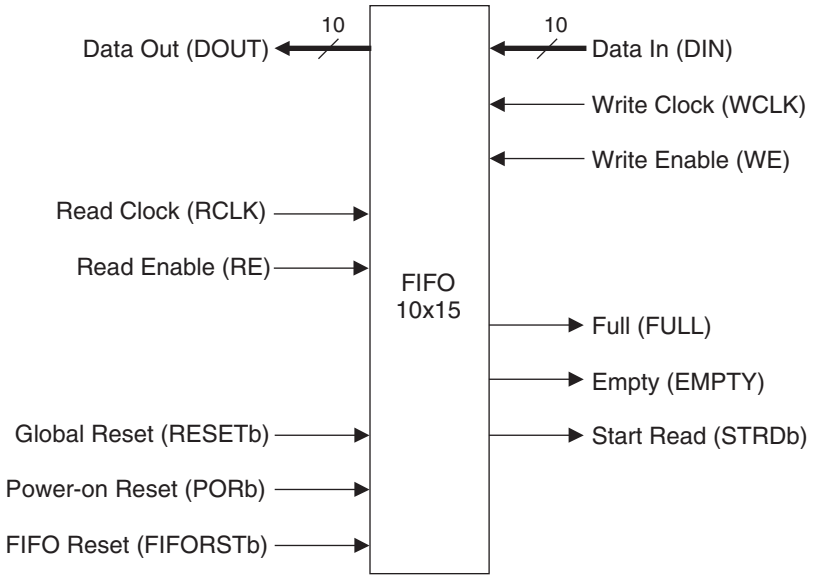


*FIFO held in RESET for SERDES-only mode.

FIFO Operations

Each GDX Block is associated with a 10-bit wide and 15-word deep (10x15) RAM. This RAM, combined with two address counters and two comparators, is used to implement a FIFO as a “circular queue”. The FIFO has separate clocks, the Read Clock (RCLK) and Write Clock (WCLK), for asynchronous operation. The FIFO has three additional control signals Write Enable, Read Enable and FIFO Reset. Three flags show the status of the FIFO: Empty, Full and Start Read. Each FIFO receives the global Power-on Reset and Reset signals. Figure 12 shows the connections to the FIFO.

Figure 12. ispGDX2 FIFO Signals

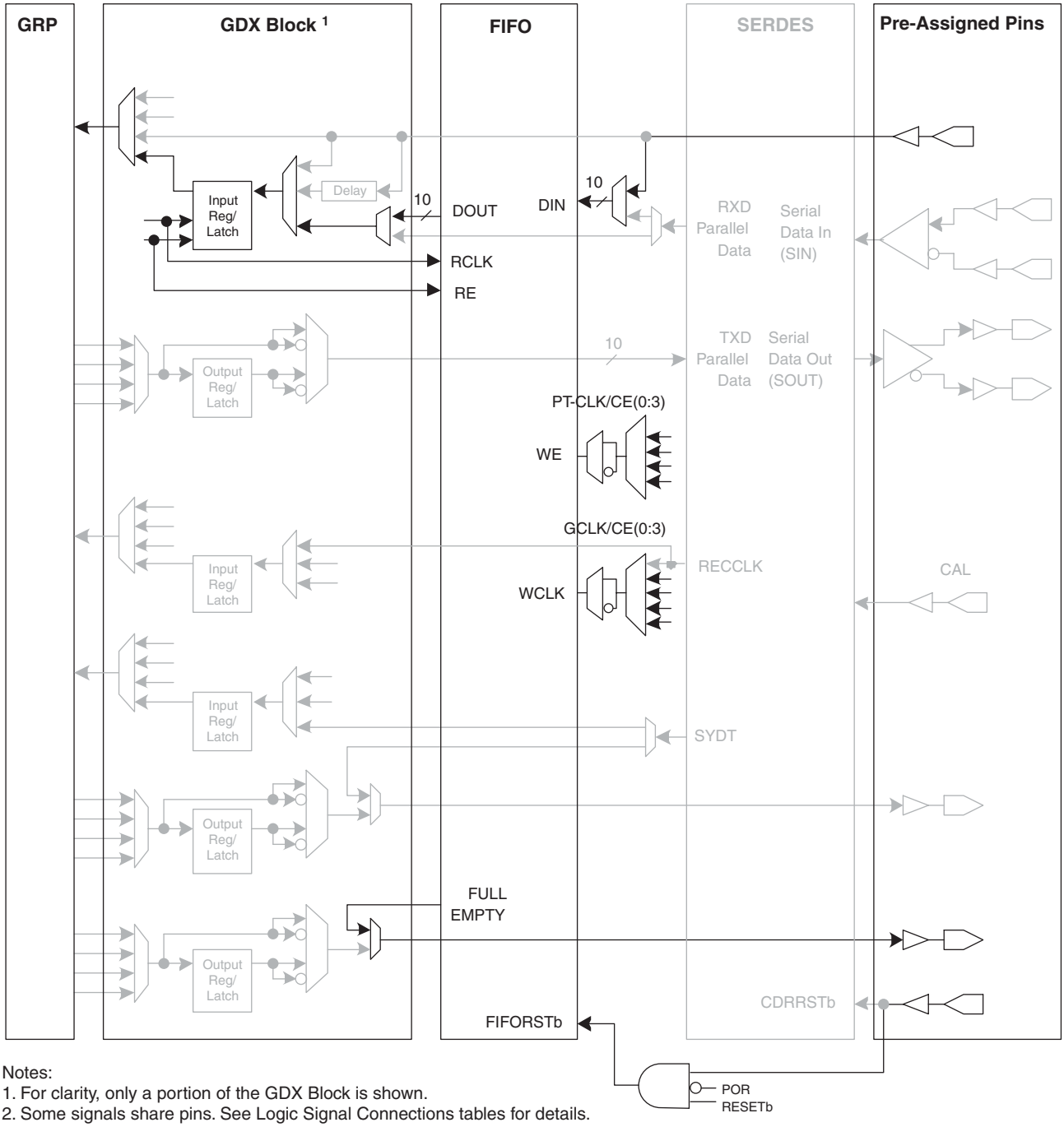


Read Clock and Read Enable are the same as the Clock and Clock Enable signals of the input registers of the associated MRB. These registers are used to register the FIFO outputs, and in modes that utilize the FIFO are configured to use the same clock and clock enable signals. The Write Clock is selected from one of the GCLK/CE signals or the RECCLK (Recovered Clock) signal from the associated SERDES. The Write Enable is selected from one of the local MRB product term CLK/CE signals. All FIFO operations occur on the rising edge of the clock although clock polarity of these signals can be programmed.

The flags from the FIFO, FULL, EMPTY and STRDb (Start Read) are each fed via a MUX in the MRB to an I/O buffer. The STRDb (half full) signal is used in conjunction with SERDES. STRDb is an active low signal, the signal is inactive (high) on FIFO RESET. After the FIFO reset when the FIFO contains data in five memory locations, at the following write clock transition the STRDb becomes active (low). Note, if the Read Clocks arrive before writing the sixth location, it may take longer than five write clocks before the STRDb becomes active. When the FIFO has data in the first six locations, at the next write clock transition the STRDb becomes inactive (high). Again, if the Read Clocks arrive before writing the seventh location, the STRDb may stay active for longer than one write clock period, even if the FIFO contains data in less than five locations. After this event, the STRDb stays inactive until the FIFO is RESET again. STRDb does not become active again even if less than six memory locations are occupied in the FIFO. It is the user's responsibility to monitor the FULL and EMPTY signals to avoid data underflow/overflow and to take appropriate actions.

Figure 13 shows how the FIFO is connected between the I/O banks and the GDX Blocks in FIFO mode. For more information on the FIFO, please refer to Lattice technical note number TN1020, *sysHSI Usage Guidelines*.

Figure 13. Operation in FIFO Mode[2]



Notes:
1. For clarity, only a portion of the GDX Block is shown.
2. Some signals share pins. See Logic Signal Connections tables for details.

High Speed Serial Interface Block (sysHSI Block)[1]

The High Speed Serial Interface (sysHSI) allows high speed serial data transfer over a pair of LVDS I/O. The ispGDX2 devices have multiple sysHSI Blocks.

Each sysHSI Block has two SERDES blocks which contain two main sub-blocks, Transmitter (with a serializer) and Receiver (with a deserializer) including Clock/Data Recovery Circuit (CDR). Each SERDES can be used as a full duplex channel. The two SERDES in a given sysHSI Block share a common clock and must operate at the same nominal frequency. Figure 14 shows the sysHSI Block.

Device features support two data coding modes: 10B/12B and 8B/10B (for use with other encoding schemes, see Lattice's sysHSI application notes). The encoding and decoding of the 10B/12B standard are performed within the device in dedicated logic. For the 8B/10B standard, the symbol boundaries are aligned internally but the encoding and decoding are performed outside the device.

Each SERDES block receives a single high speed serial data input stream (with embedded clock) from an input, and provide a low speed 10-bit wide data stream and a recovered clock to the device. For transmitting, the SERDES converts a 10-bit wide low-speed data stream to a single high-speed data stream with embedded clock for output.

Additionally, multiple sysHSI Blocks can be grouped together to form a source synchronous interface of between 1-8 channels.

Figure 15 shows the connections of the SERDES block with the FIFO, sysIO block and the MRB. Table 6 provides the descriptions of the SERDES.

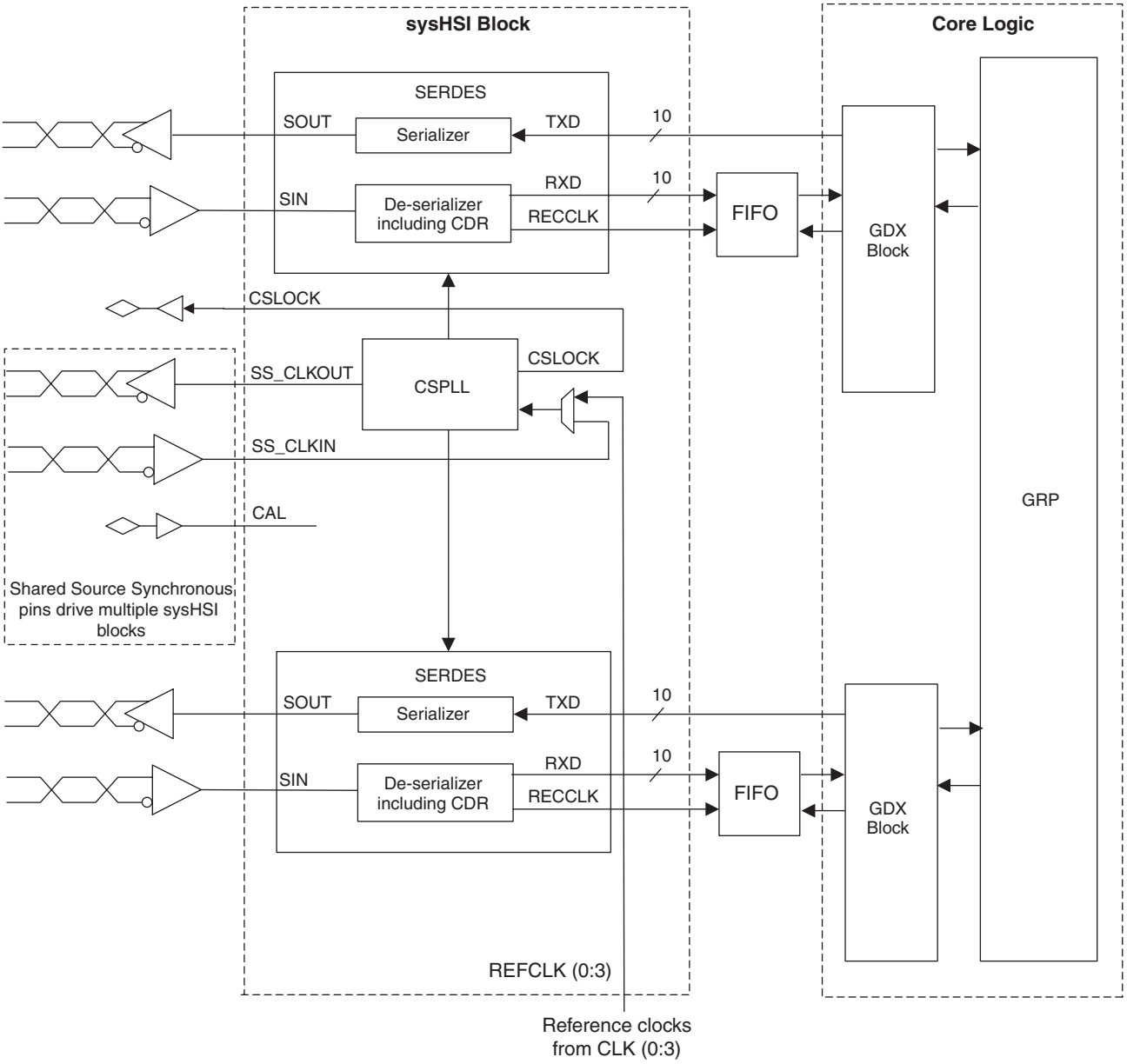
For more information on the SERDES/CDR, refer to Lattice technical note number TN1020, *sysHSI Usage Guidelines*.

Table 6. SERDES Signal Descriptions

Signal	I/O	Description
CDRRSTb	I	Resets the CDR circuit of sysHSI block
SYDT	O	Symbol alignment detect for sysHSI block
CAL	I	Initiates source synchronous calibration sequence
RXD	Internal	Parallel data in for sysHSI block
TXD	Internal	Parallel data out for sysHSI block
REFCLK	Internal	Reference clock received from the clock tree
SIN	I	Serial data input for sysHSI block (LVDS input)
SOUT	O	Serial data output for sysHSI block (LVDS output)
SS_CLKIN	I	Clock input for source synchronous group
SS_CLKOUT	O	Clock output for source synchronous group
RECCLK	Internal	Recovered clock from encoded data by CDR of sysHSI block
CSLOCK	Internal	Lock output of the PLL associated with sysHSI block

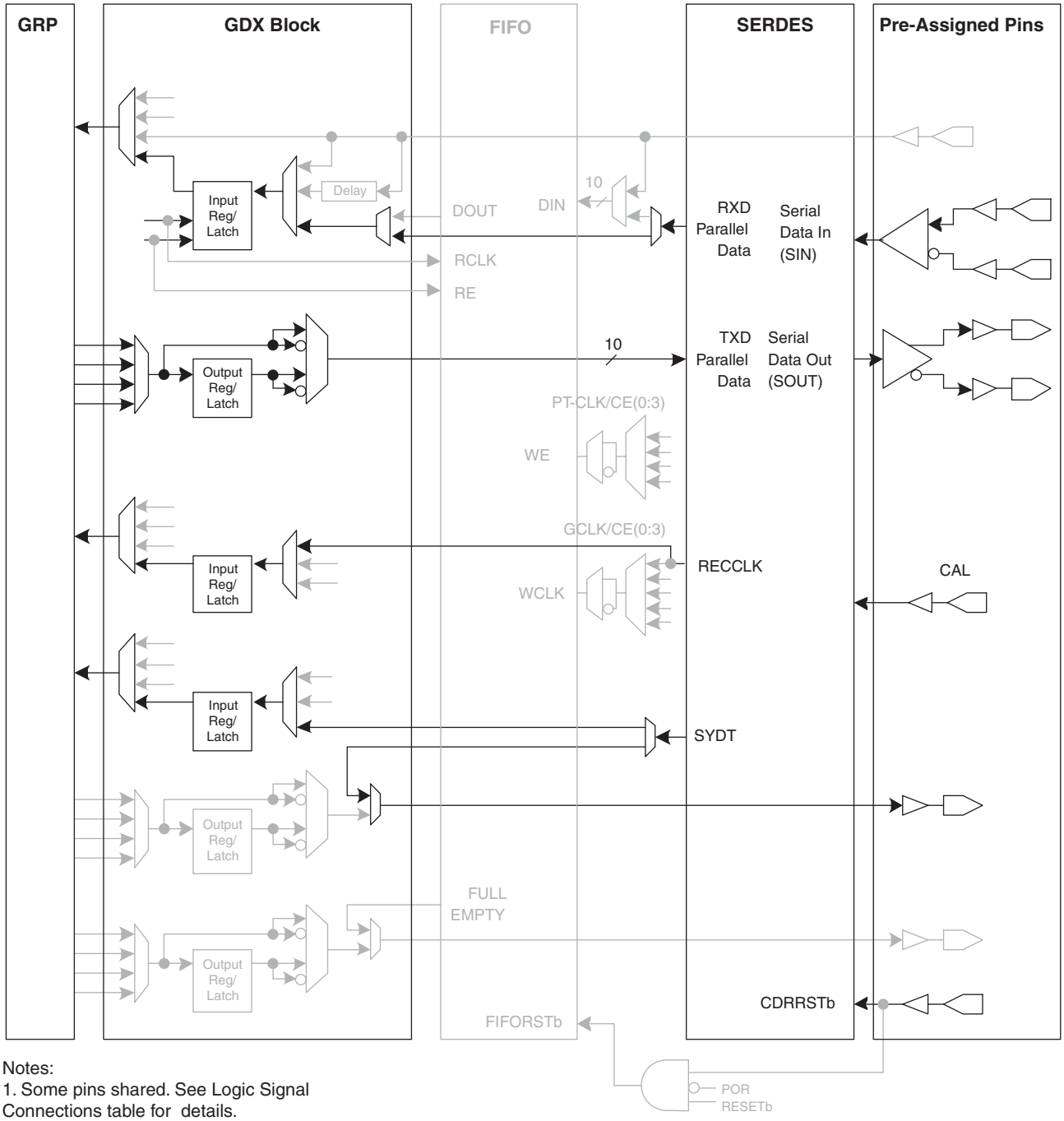
1. "E-Series" does not support sysHSI.

Figure 14. sysHSI Block with SERDES and FIFO



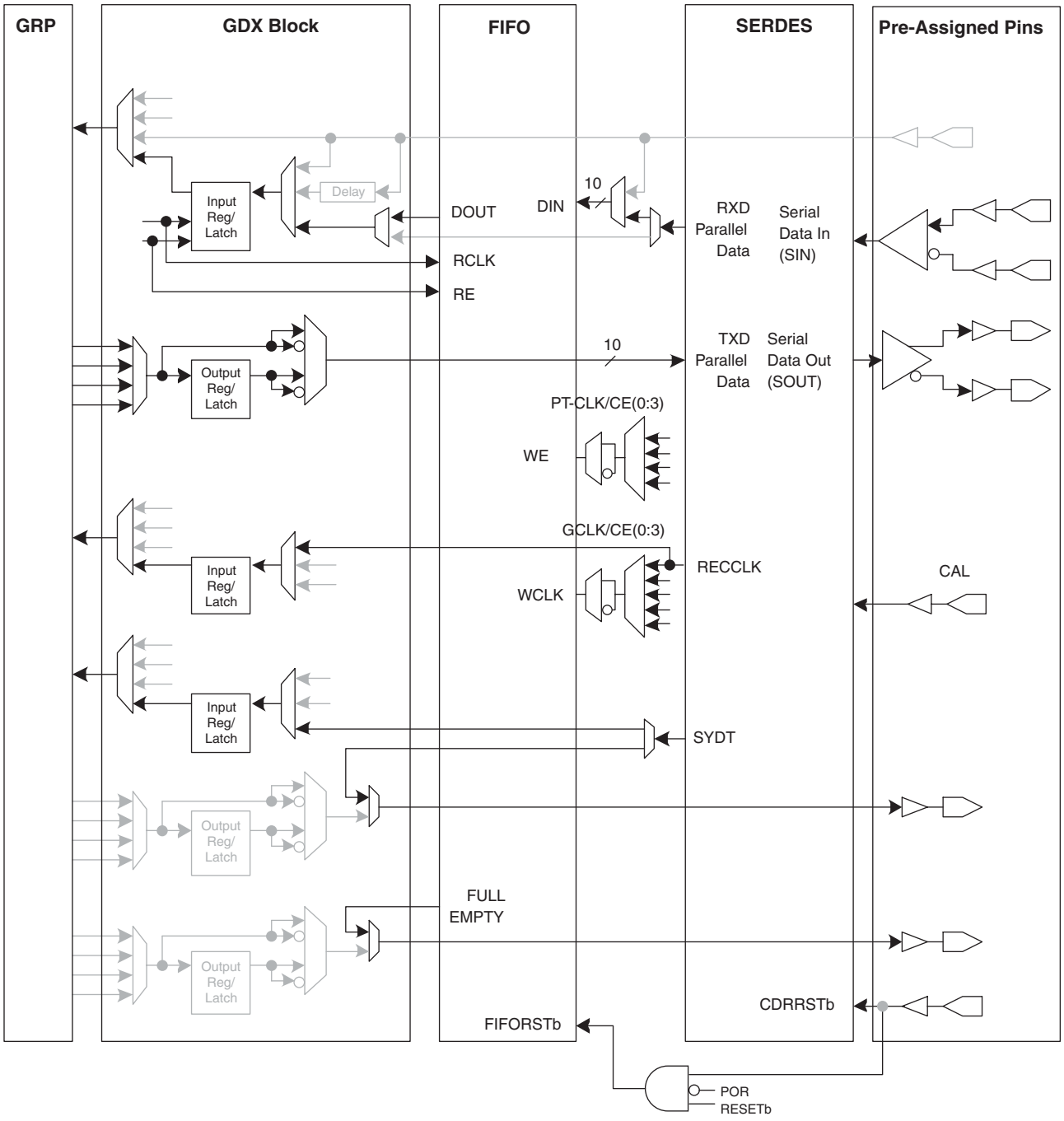
Note: Some pins are shared. See Logic Signal Connections table for details

Figure 15. Operation in SERDES Only Mode[1, 2]



Notes:
1. Some pins shared. See Logic Signal Connections table for details.
2. For SERDES only mode programmable bit holds FIFO in reset. Input registers used for DOUT, and RECCLK configured as latches and held in pass through.

Figure 16. Operation in SERDES with FIFO Mode



IEEE 1149.1-Compliant Boundary Scan Testability

All ispGDX2 devices have boundary scan cells and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic notes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more board-level testing. The test access port has its own supply voltage that can operate with LVCMOS3.3, 2.5 and 1.8 standards.

sysIO Quick Configuration

To facilitate the most efficient board test, the physical nature of the I/O cells must be set before running any continuity tests. As these tests are fast, by nature, the overhead and time that is required for configuration of the I/Os' physical nature should be minimal so that board test time is minimized. The ispGDX2 family of devices allows this by offering the user the ability to quickly configure the physical nature of the sysIO cells. This quick configuration takes milliseconds to complete, whereas it takes seconds for the entire device to be programmed. Lattice's ispVM™ System programming software can either perform the quick configuration through the PC parallel port, or can generate the ATE or test vectors necessary for a third-party test system.

IEEE 1532-Compliant In-System Programming

In-system programming of devices provides a number of significant benefits including rapid prototyping, lower inventory levels, higher quality and the ability to make in-field modifications. All ispGDX2 devices provide In-System Programming (ISP) capability through their Boundary Scan Test Access Port. This capability has been implemented in a manner that ensures that the port remains compliant to the IEEE 1532 standard. By using IEEE 1532 as the communication interface through which ISP is achieved, designers get the benefit of a standard, well defined interface.

The ispGDX2 devices can be programmed across the commercial temperature and voltage range. The PC-based Lattice software facilitates in-system programming of ispGDX2 devices. The software takes the JEDEC file output produced by the design implementation software, along with information about the scan chain, and creates a set of vectors used to drive the scan chain. The software can use these vectors to drive a scan chain via the parallel port of a PC. Alternatively, the software can output files in formats understood by common automated test equipment. This equipment can then be used to program ispGDX2 devices during the testing of a circuit board.

Security Scheme

A programmable security scheme is provided on the ispGDX2 devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this scheme prevents readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. The security scheme also prevents programming and verification. The entire device must be erased in order to reset the security scheme.

Hot Socketing

The ispGDX2 devices are well suited for those applications that require hot socketing capability. Hot socketing a device requires that the device, when powered down, can tolerate active signals on the I/Os and inputs without being damaged. Additionally, it requires that the effects of the powered-down device be minimal on active signals.

Absolute Maximum Ratings [1, 2, 3]

	ispGDX2C (1.8V)	ispGDX2B/V (2.5/3.3V)
Supply Voltage V_{CC}	-0.5 to 2.5V	-0.5 to 5.5V
PLL Supply Voltage V_{CCP}	-0.5 to 2.5V	-0.5 to 5.5V
Output Supply Voltage V_{CCO}	-0.5 to 4.5V	-0.5 to 4.5V
JTAG Supply Voltage (V_{CCJ})	-0.5 to 4.5V	-0.5 to 4.5V
Input or I/O Tristate Voltage Applied [4, 5]	-0.5 to 5.5V	-0.5 to 5.5V
Storage Temperature	-65 to 150°C	-65 to 150°C
Junction Temp. (T_J) with Power Applied	-55 to 150°C	-55 to 150°C

1. Stress above those listed under the Absolute Maximum Ratings may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied (while programming, following the programming specifications).
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of -2V to (V_{IH} (MAX)+2) volts is permitted for a duration of <20ns.
5. A maximum of 64 I/Os per device with V_{IN} > 3.6V is allowed.

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage for 1.8V Devices[1]	1.65	1.95	V
	Supply Voltage for 2.5V Devices	2.3	2.7	V
	Supply Voltage for 3.3V Devices	3	3.6	V
V_{CCP}	Supply Voltage for PLL and sysHSI Blocks, 1.8V Devices[1]	1.65	1.95	V
	Supply Voltage for PLL and sysHSI Blocks, 2.5V Devices	2.3	2.7	V
	Supply Voltage for PLL and sysHSI Blocks, 3.3V Devices	3	3.6	V
V_{CCJ}	Power Supply Voltage for JTAG Programming 1.8V Operation	1.65	1.95	V
	Power Supply Voltage for JTAG Programming 2.5V Operation	2.3	2.7	V
	Power Supply Voltage for JTAG Programming 3.3V Operation	3	3.6	V
T_J (COM)	Junction Commercial Operation	0	90	°C
T_J (IND)	Junction Industrial Operation	-40	105	°C

1. sysHSI specification is valid for V_{CC} and V_{CCP} = 1.7V to 1.9V.

Erase Reprogram Specifications

Parameter	Min	Max	Units
Erase/Reprogram Cycle	1,000	—	Cycles

Note: Valid over commercial temperature range.

Hot Socketing Specifications[1, 2, 3]

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DK}[4]	Input or Tristated I/O Leakage Current	0 ≤ V_{IN} ≤ 3.0V	—	+/-50	+/-800	µA

1. Insensitive to sequence of V_{CC} and V_{CCO}. However, assumes monotonic rise/fall rates for V_{CC} and V_{CCO}, provided (V_{IN} - V_{CCO}) ≤ 3.6V.
2. LVTTL, LVCMOS only.
3. 0 < V_{CC} ≤ V_{CC} (MAX), 0 < V_{CCO} ≤ V_{CCO} (MAX).
4. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}. Device defaults to pull-up until fuse circuitry is active.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1]	Input or I/O Low Leakage	$0 \le V_{IN} \le (V_{CCO} - 0.2V)$	—	—	10	µA
		$(V_{CCO} - 0.2V) < V_{IN} \le 3.6V$	—	—	30	µA
I_{IH}[3]	Input High Leakage Current	$3.6V < V_{IN} \le 5.5V$ and $3.0V \le V_{CCO} \le 3.6V$	—	—	3	mA
I_{PU}	I/O Active Pull-up Current	$0 \le V_{IN} \le 0.7\ V_{CCO}$	-30	—	-150	µA
I_{PD}	I/O Active Pull-down Current	V_{IL} (MAX) $\le V_{IN} \le V_{IH}$ (MAX)	30	—	150	µA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL}$ (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7\ V_{CCO}$	-30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive Current	$0 \le V_{IN} \le V_{IH}$ (MAX)	—	—	150	µA
I_{BHLH}	Bus Hold High Overdrive Current	$0 \le V_{IN} \le V_{IH}$ (MAX)	—	—	-150	µA
V_{BHT}	Bus Hold Trip Points		V_{CCO} * 0.35	—	V_{CCO} * 0.65	V
C_1	I/O Capacitance[2]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	8	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	
C_2	Clock Capacitance[2]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	6	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	
C_3	Global Input Capacitance[2]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	6	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A = 25°C, f = 1.0MHz.
3. 5V tolerant inputs and I/Os should be placed in banks where $3.0V \le V_{CCO} \le 3.6V$. The JTAG ports are not included for the 5V tolerant interface.

Supply Current

Over Recommended Operating Conditions (ispGDX2-256)[4]

Symbol	Description	Power Pins	Vcc (V)	Min.	Typ.	Max.	Units
I_{CC}[1,2]	Core Logic Power Supply Current	V_{CC}	3.3	—	59.6	—	mA
			2.5	—	58.7	—	mA
			1.8	—	60.0	—	mA
	GPLL/sysHSI Logic Power Supply Current		3.3	—	118.7	—	mA
			2.5	—	118.7	—	mA
			1.8	—	117.5	—	mA
I_{CCP}[2]	GPLL/sysHSI CSPLL Power Supply Current	V_{CCP}	3.3	—	14.7	—	mA
			2.5	—	14.7	—	mA
			1.8	—	17.4	—	mA
I_{CCO}[3]	Bank Power Supply Current	V_{CCO}	3.3	—	35	—	mA
			2.5	—	35	—	mA
			1.8	—	25	—	mA
I_{CCJ}	JTAG Programming Current	V_{CCJ}	3.3	—	1.5	—	mA
			2.5	—	1.0	—	mA
			1.8	—	800	—	µA

1. 64-input switching frequency at 20 MHz, with one GRP fanout.
2. One GPLL with f_{VCO} = 400 MHz and one sysHSI Block (two receivers and two transmitters) at 622 MHz data rate.
3. All 8-bank reference circuit currents, all I/Os in tristate, inputs held at valid logic levels, and bus maintenance circuits disabled.
4. T_A = 25°C

sysIO Recommended Operating Conditions

Standard	V_{CCO} (V)[1]			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVCMOS 3.3	3.0	3.3	3.6	-	-	-
LVCMOS 2.5	2.3	2.5	2.7	-	-	-
LVCMOS 1.8[2]	1.65	1.8	1.95	-	-	-
LVTTL	3.0	3.3	3.6	-	-	-
PCI 3.3	3.0	3.3	3.6	-	-	-
PCI-X	3.0	3.3	3.6	-	-	-
AGP-1X	3.15	3.3	3.45	-	-	-
SSTL 2	2.3	2.5	2.7	1.15	1.25	1.35
SSTL 3	3.0	3.3	3.6	1.3	1.5	1.7
CTT 3.3	3.0	3.3	3.6	1.35	1.5	1.65
CTT 2.5	2.3	2.5	2.7	1.35	1.5	1.65
HSTL Class I	1.4	1.5	1.6	0.68	0.75	0.9
HSTL Class III	1.4	1.5	1.6	-	0.9	-
HSTL Class IV	1.4	1.5	1.6	-	0.9	-
GTL+	1.4	-	3.6	0.882	1.0	1.122
LVPECL	3.0	3.3	3.6	-	-	-
LVDS	2.3	2.5/3.3	3.6	-	-	-
BLVDS	2.3	2.5/3.3	3.6	-	-	-

1. Inputs are independent of V_{CCO} setting. However, V_{CCO} must be set within the valid operating range for one of the supported standards.
2. Software default setting.

sysIO Single Ended DC Electrical Characteristics

Over Recommended Operating Conditions

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max (V)	V_{OH} Min (V)	I_{OL}[2] (mA)	I_{OH}[2] (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVCMOS 3.3	-0.3	0.8	2.0	5.5	0.4	2.4	20, 16, 12, 8, 5.33, 4	-20, -16, -12, -8, -5.33, -4
					0.2	V_{CCO} - 0.2	0.1	-0.1
LVTTL	-0.3	0.8	2.0	5.5	0.4	2.4	4	-4
					0.2	V_{CCO} - 0.2	0.1	-0.1
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	V_{CCO} - 0.4	16, 12, 8, 5.33, 4	-16, -12, -8, -5.33, -4
					0.2	V_{CCO} - 0.2	0.1	-0.1
LVCMOS 1.8[1, 3]	-0.3	0.68	1.07	3.6	0.4	V_{CCO} - 0.4	8	-8
LVCMOS 1.8[3]	-0.3	0.68	1.07	3.6	0.4	V_{CCO} -0.4	12, 5.33, 4	-12, -5.33, -4
					0.2	V_{CCO} - 0.2	0.1	-0.1
PCI 3.3[4]	-0.3	1.08	1.5	3.6	0.1 V_{CCO}	0.9 V_{CCO}	1.5	-0.5
PCI -X[5]	-0.3	1.26	1.5	3.6	0.1 V_{CCO}	0.9 V_{CCO}	1.5	-0.5
AGP-1X[4]	-0.3	1.08	1.5	3.6	0.1 V_{CCO}	0.9 V_{CCO}	1.5	-0.5
SSTL3 class I	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.7	V_{CCO} - 1.1	8	-8
SSTL3 class II	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.5	V_{CCO} - 0.9	16	-16
SSTL2 class I	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.54	V_{CCO} - 0.62	7.6	-7.6
SSTL2 class II	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.35	V_{CCO} - 0.43	15.2	-15.2
CTT 3.3	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	V_{REF} - 0.4	V_{REF} + 0.4	8	-8
CTT 2.5	-0.3	V_{REF} - 0.3	V_{REF} + 0.2	3.6	V_{REF} - 0.4	V_{REF} + 0.4	8	-8
HSTL class I	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} - 0.4	8	-8
HSTL class III	-0.3	V_{REF} - 0.2	V_{REF} + 0.1	3.6	0.4	V_{CCO} - 0.4	24	-8
HSTL class IV	-0.3	V_{REF} - 0.3	V_{REF} + 0.1	3.6	0.4	V_{CCO} - 0.4	48	-8
GTL+	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.6	n/a	36	n/a

1. Software default setting.
2. The average DC current drawn by I/Os between adjacent bank GND connections, or between the last GND in an I/O bank and the end of the I/O bank, as shown in the logic signals connection table, shall not exceed n*8mA. Where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.
3. For 1.8V devices (ispGDX2C) these specifications are V_{IL} = 0.35 V_{CC} and V_{IH} = 0.65V_{CC}
4. For 1.8V power supply devices these specifications are V_{IL} = 0.3 * V_{CC} * 3.3/1.8, V_{IH} = 0.5 * V_{CC} * 3.3/1.8
5. For 1.8V power supply devices these specifications are V_{IL} = 0.35 * V_{CC} * 3.3/1.8 and V_{IH} = 0.5 * V_{CC} * 3.3/1.8

sysIO Differential DC Electrical Characteristics

Over Recommended Operating Conditions

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
LVDS						
V_{INP} V_{INM}	Input Voltage	—	0	—	2.4	V
V_{THD}	Differential Input Threshold	0.2V ≤ V_{CM} ≤ 1.8V	+/-100	—	—	mV
I_{IN}	Input Current	Power On	—	—	+/-10	µA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	R_T = 100Ω	—	1.38	1.60	V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	R_T = 100Ω	0.9	1.03	—	V
V_{OD}	Output Voltage Differential	(V_{OP} - V_{OM}), R_T = 100Ω	250	350	450	mV
ΔV_{OD}	Change in V_{OD} Between High and Low	—	—	—	50	mV
V_{OS}	Output Voltage Offset	(V_{OP} - V_{OM})/2, R_T = 100Ω	1.125	1.25	1.375	V
ΔV_{OS}	Change in VOS Between H and L	—	—	—	50	mV
I_{OSD}	Output Short Circuit Current	V_{OD} = 0V. Driver Outputs Shorted.	—	—	24	mA
Bus LVDS[1]						
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	R_T = 27Ω	—	1.4	1.80	V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	R_T = 27Ω	0.95	1.1	—	V
V_{OD}	Output Voltage Differential	|V_{OP} - V_{OM}|, RT = 27Ω	240	300	460	mV
ΔV_{OD}	Change in V_{OD} Between H and L		—	—	27	mV
V_{OS}	Output Voltage Offset	|V_{OP} - VOM| /2, RT = 27Ω	1.1	1.3	1.5	V
ΔV_{OS}	Change in V_{OS} Between H and L		—	—	27	mV
I_{OSD}	Output Short Circuit Current	V_{OD} = 0. Driver Outputs Shorted.	—	36	65	mA

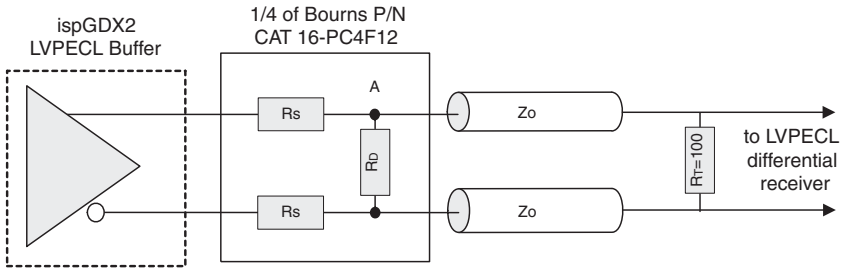
1. V_{OP} and V_{OM} are the two outputs of the LVDS output buffer.

LVPECL[1]

DC Parameter	Parameter Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
V_{CCO}	Output Supply Voltage	3.0		3.3		3.6		V
V_{IH}	Input Voltage High	1.49	2.72	1.49	2.72	1.49	2.72	V
V_{IL}	Input Voltage Low	0.86	2.125	0.86	2.125	0.86	2.125	V
V_{OH}	Output Voltage High	1.7	2.11	1.92	2.28	2.03	2.41	V
V_{OL}	Output Voltage Low	0.96	1.27	1.06	1.43	1.25	1.57	V
V_{DIFF}[2]	Differential Input voltage	0.3		0.3		0.3		V

1. These values are valid at the output of the source termination pack as shown above with 100-ohm differential load only (see Figure 17). The V_{OH} levels are 200mV below the standard LVPECL levels and are compatible with devices tolerant of the lower common mode ranges.
2. Valid for 0.2V ≤ V_{CM} ≤ 1.8V.

Figure 17. LVPECL Driver with Three Resistor Pack



ispGDX2V/B/C, ispGDX2EV/EB/EC External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description	-3		-32		-35		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Output Paths										
t_{PD}	Data From Input Pin to Output Pin	—	3.0	—	3.2	—	3.5	—	5.0	ns
t_{PD_SEL}	Data From Global Select Pin to Output Pin	—	2.8	—	3.0	—	3.3	—	4.7	ns
t_{CO}	Global Clock to Output	—	2.9	—	3.1	—	3.2	—	5.4	ns
t_{OPS}	Set-up Time Before Global Clock	2.0	—	2.0	—	2.0	—	3.0	—	ns
t_{OPH}	Hold Time After Global Clock	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{OPCES}	PT Clock Enable Setup Time Before Global Clock	3.0	—	3.0	—	4.1	—	6.9	—	ns
t_{OPCEH}	PT Clock Enable Hold Time After Global Clock	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{OPRSTO}	External Reset Pin to Output Delay	—	5.3	—	6.0	—	6.0	—	10.0	ns
Input Paths										
t_{IPS}	Set-up Time Before Global Clock	0.5	—	0.5	—	0.5	—	0.9	—	ns
t_{IPSZ}	Set-up Time Before Global Clock (Zero Hold Time)	2.0	—	2.0	—	2.0	—	3.0	—	ns
t_{IPH}	Hold Time After Global Clock	1.0	—	1.0	—	1.0	—	1.7	—	ns
t_{IPHZ}	Hold Time After Global Clock (Zero Hold Time)	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{IPCES}	PT Clock Enable Setup Time Before Global Clock	3.1	—	3.1	—	3.1	—	5.1	—	ns
t_{IPCEH}	PT Clock Enable Hold Time After Global Clock	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{IPRSTO}	External Reset Pin to Output Delay	—	5.6	—	6.5	—	7.5	—	12.5	ns
Output Enable Paths										
t_{OECO}	Global Clock to Output Enabled Pin	—	4.2	—	4.5	—	5.5	—	9.1	ns
t_{OES}	Output Enable Register Set-up Time Before Global Clock	1.6	—	1.6	—	2.0	—	3.4	—	ns
t_{OEH}	Hold Time After Global Clock	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{OECES}	PT Clock Enable Setup Time Before Global Clock	3.5	—	3.5	—	4.1	—	6.9	—	ns
t_{OECEH}	PT Clock Enable Hold Time After Global Clock	0.0	—	0.0	—	0.0	—	0.0	—	ns
$t_{GOE/DIS}$	Global OE Input to Output Enable/Disable	—	3.5	—	3.8	—	4.5	—	7.5	ns
$t_{TOE/DIS}$	Test OE Input to Output Enable/Disable	—	5.2	—	5.5	—	6.2	—	10.3	ns
$t_{EN/DIS}$	Input to Output Enable/Disable	—	5.2	—	5.5	—	6.2	—	10.3	ns
Clock and Reset Paths										
t_{RW}	Width of Reset Pulse	2.5	—	2.5	—	2.5	—	4.1	—	ns
t_{CW}	Clock Width	1.3	—	1.5	—	1.6	—	2.7	—	ns
t_{GW}	Clock Width	1.5	—	1.6	—	1.6	—	2.7	—	ns
f_{MAX} (Ext)	Clock Frequency with External Feedback $1/(t_{OPS} + t_{CO})$	—	204	—	196	—	192	—	119	MHz
f_{MAX} (Tog, No PLL)	Clock Frequency Maximum Toggle (No PLL)	—	360	—	330	—	300	—	180	MHz

ispGDX2V/B/C, ispGDX2EV/EB/EC External Switching Characteristics

Over Recommended Operating Conditions

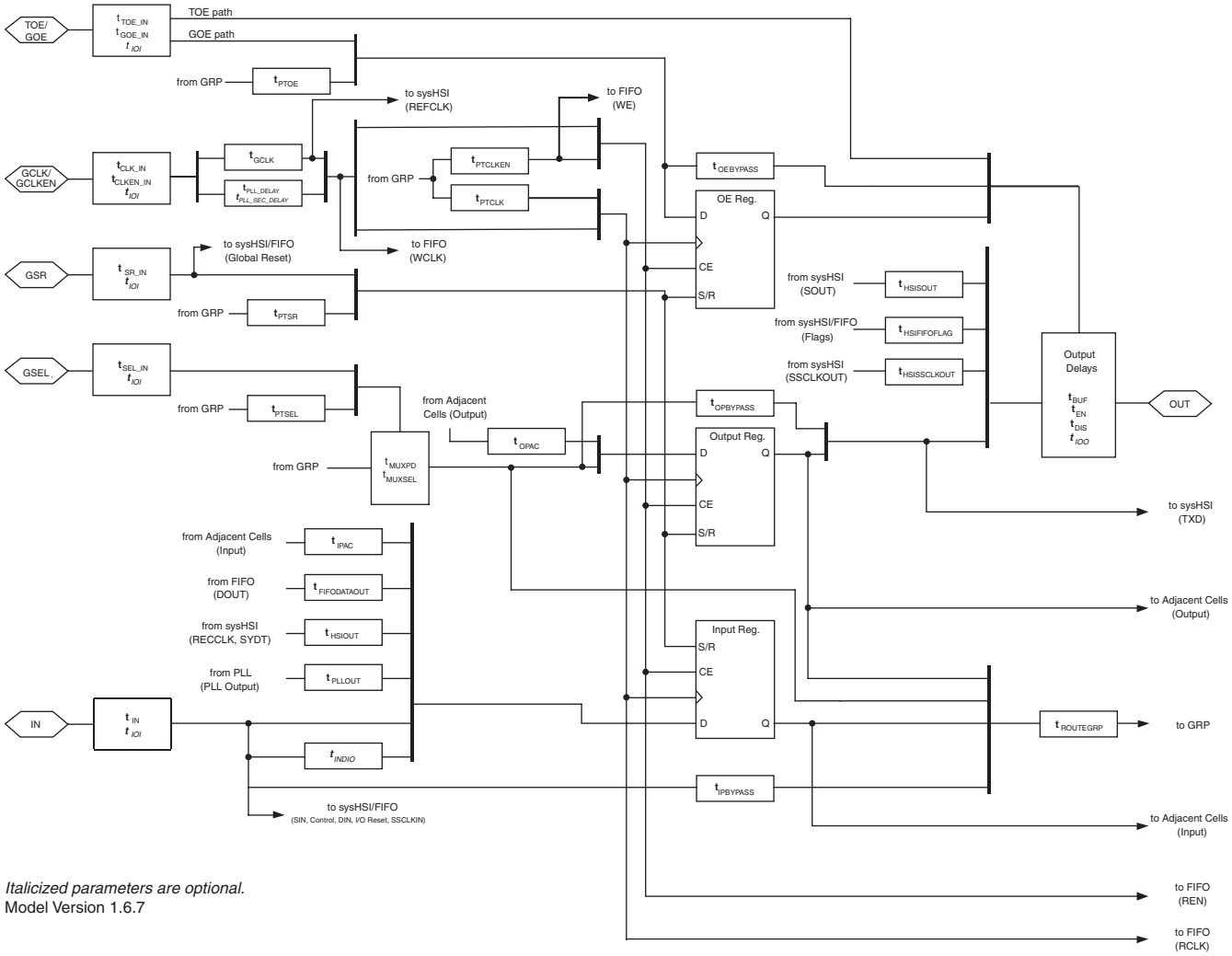
Parameter	Description	-3		-32		-35		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX} (Tog, PLL)	Clock Frequency Maximum Toggle (With PLL)	—	360	—	330	—	300	—	180	MHz

Timing v.2.2

Timing Model

The task of determining the timing through the ispGDX2 family is relatively simple. The timing model provided in Figure 18 shows the specific delay paths. Once the implementation of a given function is determined either conceptually or from the software report file, the delay path of the function can easily be determined from the timing model. The Lattice design tools report the timing delays based on the same timing model for a particular design. Note that the internal timing parameters are given for reference only, and are not tested. The external timing parameters are tested and guaranteed for every device.

Figure 18. ispGDX2 Timing Model Diagram (I/O Cell)



Italicized parameters are optional.
Model Version 1.6.7

Figure 19. ispGDX2 Timing Model Diagram (with sysHSI and FIFO Receive Mode)

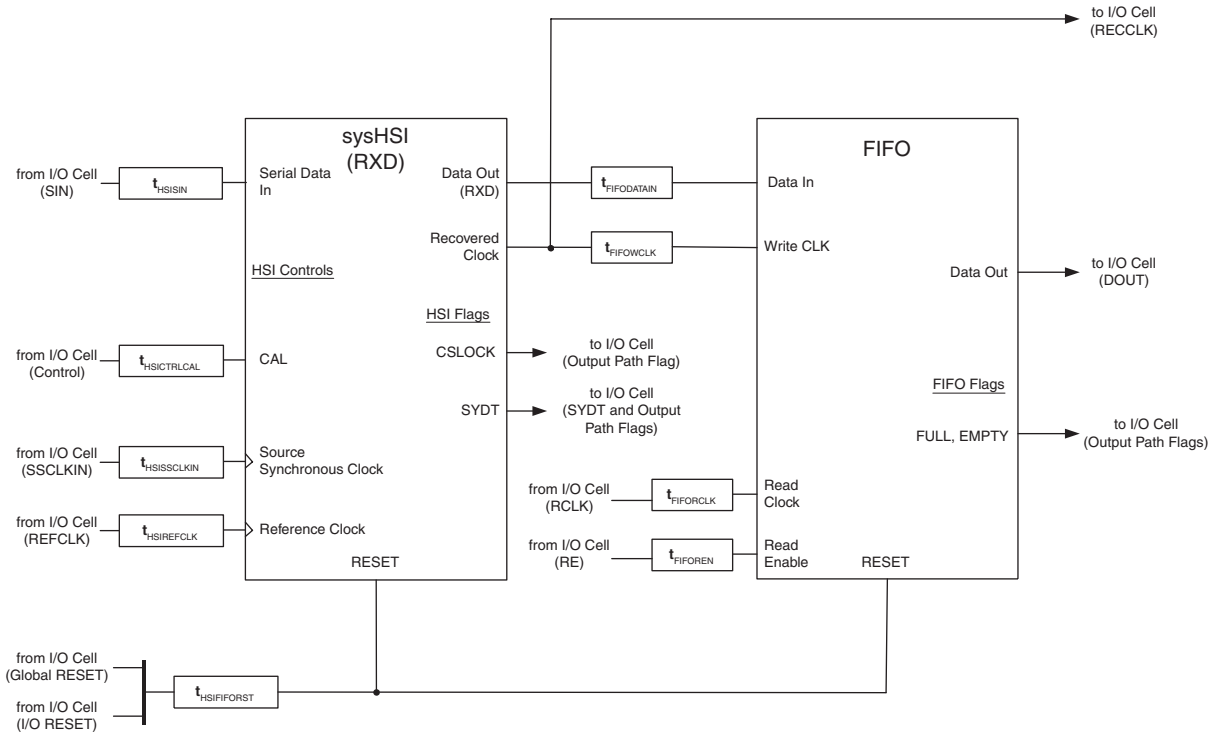


Figure 20. ispGDX2 Timing Model Diagram (with sysHSI Transmit Mode)

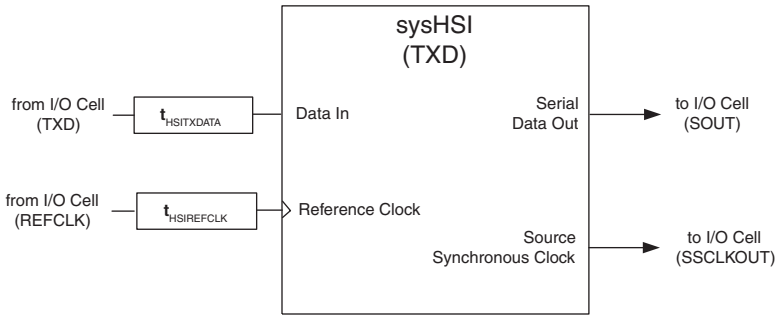
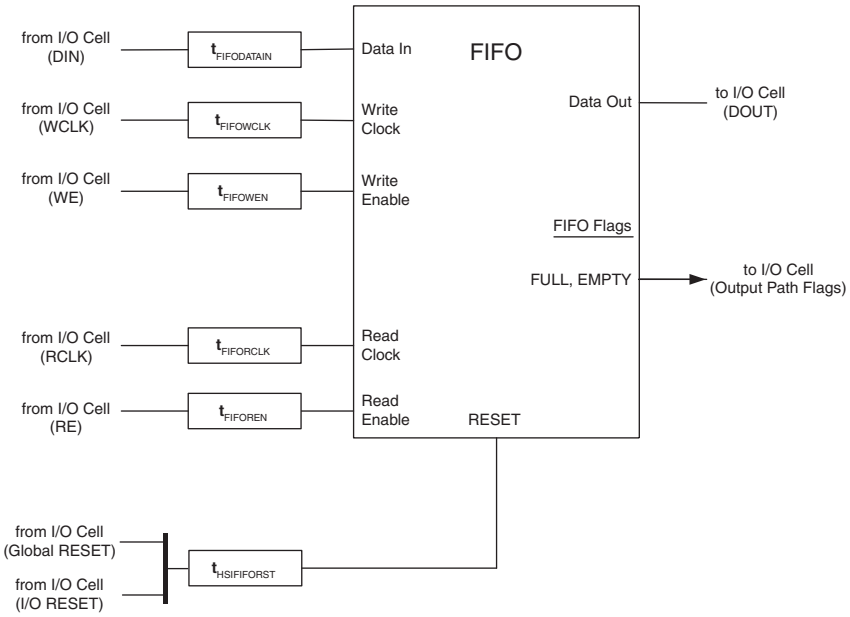


Figure 21. ispGDX2 Timing Model Diagram (in FIFO Only Mode)



Sample External Timing Calculations

The following equations illustrate the task of determining the timing through the ispGDX2 family. These are only a sample of equations to calculate the timing through the ispGDX2.

Figure 18 shows the specific delay paths and the Internal Timing Parameters table provides the parameter values. Note that the internal timing parameters are given for reference only and are not tested. The external timing parameters are tested and guaranteed for every device.

Data from global select pin to output pin:
$t_{PD\_SEL} = t_{SEL\_IN} + t_{MUXSEL} + t_{OPBYPASS} + t_{BUF}$

Global clock to output:
$t_{CO} = t_{CLK\_IN} + t_{GCLK} + t_{OPCOi} + t_{BUF}$

Input register or latch set-up time before global clock:
$t_{IPS} = t_{IN} + t_{IPS} - (t_{CLK} + t_{GCLK})$

Input register or latch hold time after global clock:
$t_{IPH} = (t_{CLK\_IN} + t_{GCLK}) + t_{IPHi} - t_{IN}$

Data from product term select to output pin:
$t_{PD\_PTSEL} = t_{IN} + t_{IPBYPASS} + t_{ROUTEGRP} + t_{PTSEL} + t_{MUXSEL} + t_{OPBYPASS} + t_{BUF}$

Product term clock to output:
$t_{CO\_PT} = t_{IN} + t_{IPBYPASS} + t_{ROUTEGRP} + t_{PTCLK} + t_{OPCOi} + t_{BUF}$

Input register or latch set-up time before product term clock:
$t_{IPS\_PT} = t_{IN} + t_{IPSi\_PT} - (t_{IN} + t_{IPBYPASS} + t_{ROUTEGRP} + t_{PTCLK})$

Input register or latch hold time after product term clock:
$t_{IPH\_PT} = (t_{IN} + t_{IPBYPASS} + t_{ROUTEGRP} + t_{PTCLK}) + t_{IPHi} - t_{IN}$

Global OE input to output enable/disable:
$t_{GOE/DIS} = t_{GOE\_IN} + t_{OEBYPASS} + t_{EN}$

External reset pin to output delay:
$t_{OPRSTO} = t_{SR\_IN} + t_{OPASROi} + t_{BUF}$

ispGDX2V/B/C, ispGDX2EV/EB/EC Internal Timing Parameters[1]

Over Recommended Operating Conditions

Parameter	Description	-3		-32		-35		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input/Output Delays										
t_{BUF}	Output Buffer Delay	—	0.80	—	0.80	—	0.80	—	1.14	ns
t_{CLK_IN}	Global Clock Input Delay	—	1.00	—	1.00	—	1.00	—	1.67	ns
t_{CLKEN_IN}	Global Clock Enable Input Delay	—	1.80	—	1.80	—	1.80	—	3.00	ns
t_{DIS}	Output Disable Delay	—	1.80	—	1.80	—	2.50	—	4.17	ns
t_{EN}	Output Enable Delay	—	1.50	—	1.80	—	2.50	—	4.17	ns
t_{GOE_IN}	Global Output Enable Path Delay	—	2.00	—	2.00	—	2.00	—	3.33	ns
t_{IN}	Input Pin Delay	—	0.40	—	0.40	—	0.40	—	0.57	ns
t_{SEL_IN}	Global MUX Select Input Delay	—	1.60	—	1.60	—	1.60	—	2.29	ns
t_{SR_IN}	Global Set/Reset Path Delay	—	2.00	—	2.70	—	2.70	—	4.50	ns
t_{TOE_IN}	Test Output Enable Path Delay	—	3.70	—	3.70	—	3.70	—	6.17	ns
Shift Register and MUX Delays										
t_{IPAC}	Input Path Adjacent I/O Cell Delay (Shift Register)	—	0.80	—	0.80	—	0.80	—	1.33	ns
t_{OPAC}	Output Path Adjacent I/O Cell Delay (Shift Register)	—	1.30	—	1.30	—	1.30	—	2.17	ns
t_{MUXPD}	MUX Data Path Delay	—	0.90	—	0.90	—	0.90	—	1.29	ns
t_{MUXSEL}	MUX Select Path Delay	—	0.40	—	0.40	—	0.40	—	0.57	ns
AND Arrays and Routing Delays										
$t_{FIFODATAOUT}$	FIFO Output to I/O Block Delay	—	0.00	—	0.00	—	0.00	—	0.00	ns
t_{GCLK}	Clock Tree Delay	—	0.40	—	0.40	—	0.40	—	0.67	ns
$t_{HSIFIFOFLAG}$	HSI/FIFO Flag to I/O Block Delay	—	0.00	—	0.00	—	0.00	—	0.00	ns
t_{HSIOUT}	HSI Output to I/O Cell Block Delay	—	0.00	—	0.00	—	0.00	—	0.00	ns
$t_{HSISSCLKOUT}$	HSI Source Synchronous Clock to I/O Cell Block Delay	—	0.00	—	0.00	—	0.00	—	0.00	ns
t_{PLL_DELAY}	PLL Delay Increment	—	0.33	—	0.33	—	0.33	—	0.33	ns
t_{PTCLK}	Clock AND Array Delay	—	2.20	—	2.20	—	2.20	—	3.67	ns
$t_{PTCLKEN}$	Clock Enable AND Array Delay	—	2.10	—	2.10	—	2.10	—	3.50	ns
t_{PTOE}	OE AND Array Delay	—	2.40	—	2.40	—	2.40	—	4.00	ns
t_{PTSEL}	Select AND Array Delay	—	1.70	—	1.70	—	1.70	—	2.83	ns
t_{PTSR}	Set/Reset AND Array Delay	—	1.40	—	1.40	—	2.70	—	4.50	ns
$t_{ROUTEGRP}$	Global Routing Pool Delay	—	0.90	—	0.90	—	0.90	—	1.29	ns
Register/Latch Delays, Output Paths										
$t_{OPASROi}$	Asynchronous Set/Reset to Output	—	2.50	—	2.50	—	2.50	—	4.17	ns
$t_{OPASRRi}$	Asynchronous Set/Reset Recovery	—	2.50	—	2.50	—	2.50	—	4.17	ns
$t_{OPBYPASS}$	Register/Latch Bypass Delay	—	0.00	—	0.20	—	0.50	—	0.71	ns
t_{OPCEHi}	Register Clock Enable Hold Time	1.30	—	1.30	—	1.30	—	2.17	—	ns
t_{OPCESi}	Register Clock Enable Setup Time (Global Clock Enable)	1.10	—	1.10	—	1.10	—	1.83	—	ns
t_{OPCESi_PT}	Register Clock Enable Setup Time (Product Term Clock Enable)	1.00	—	1.00	—	2.10	—	3.50	—	ns
t_{OPCOi}	Register Clock to Output Delay	—	0.70	—	0.90	—	1.00	—	1.67	ns
t_{OPHi}	Register Hold Time	0.80	—	0.80	—	0.80	—	1.33	—	ns

ispGDX2V/B/C, ispGDX2EV/EB/EC Internal Timing Parameters[1] (Continued)

Over Recommended Operating Conditions

Parameter	Description	-3		-32		-35		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{OPLGOi}	Latch Gate to Output Delay	—	1.00	—	1.00	—	1.00	—	1.67	ns
t_{OPLHi}	Latch Hold Time	0.80	—	0.80	—	0.80	—	1.33	—	ns
t_{OPLPDi}	Latch Propagation Delay (Transparent Mode)	—	0.30	—	0.30	—	0.30	—	0.50	ns
t_{OPLSi}	Latch Setup Time (Global Gate)	1.20	—	1.20	—	1.20	—	2.00	—	ns
t_{OPLSi_PT}	Latch Setup Time (Product Term Gate)	1.00	—	1.00	—	1.00	—	1.67	—	ns
t_{OPSi}	Register Setup Time (Global Clock)	1.20	—	1.20	—	1.20	—	2.00	—	ns
t_{OPSi_PT}	Register Setup Time (Product Term Clock)	1.00	—	1.00	—	1.00	—	1.67	—	ns
$t_{OPSRPWi}$	Asynchronous Set/Reset Pulse Width	—	2.50	—	2.50	—	2.50	—	4.17	ns
Register/Latch Delays, Input Paths										
$t_{IPASROi}$	Asynchronous Set/Reset to Output	—	1.00	—	1.00	—	1.70	—	2.83	ns
$t_{IPASRRi}$	Asynchronous Set/Reset Recovery	—	2.50	—	2.50	—	2.50	—	4.17	ns
$t_{IPBYPASS}$	Register/Latch Bypass Delay	—	0.00	—	0.00	—	0.00	—	0.00	ns
t_{IPCEHi}	Register Clock Enable Hold Time	1.30	—	1.30	—	1.30	—	2.17	—	ns
t_{IPCESi}	Register Clock Enable Setup Time (Global Clock Enable)	1.10	—	1.10	—	1.10	—	1.83	—	ns
t_{IPCESi_PT}	Register Clock Enable Setup Time (Product Term Clock Enable)	1.10	—	1.10	—	1.10	—	1.83	—	ns
t_{IPCOi}	Register Clock to Output Delay	—	0.80	—	1.00	—	1.00	—	1.67	ns
t_{IPHi}	Register Hold Time	0.00	—	0.00	—	0.00	—	0.00	—	ns
t_{IPLGOi}	Latch Gate to Output Delay	—	1.00	—	1.00	—	1.00	—	1.67	ns
t_{IPLHi}	Latch Hold Time	0.00	—	0.00	—	0.00	—	0.00	—	ns
t_{IPLPDi}	Latch Propagation Delay (Transparent Mode)	—	0.30	—	0.30	—	0.30	—	0.50	ns
t_{IPLSi}	Latch Setup Time (Global Term)	1.50	—	1.50	—	1.50	—	2.50	—	ns
t_{IPLSi_PT}	Latch Setup Time (Product Term Gate)	1.50	—	1.50	—	1.50	—	2.50	—	ns
t_{IPSi}	Register Setup Time (Global Clock)	1.50	—	1.50	—	1.50	—	2.50	—	ns
t_{IPSi_PT}	Register Setup Time (Product Term Clock)	1.50	—	1.50	—	1.50	—	2.50	—	ns
$t_{IPSRPWi}$	Asynchronous Set/Reset Pulse Width	—	2.50	—	2.50	—	2.50	—	4.17	ns
OE Paths										
$t_{OEASROi}$	Asynchronous Set/Reset to Output	—	2.50	—	2.50	—	2.50	—	4.17	ns
$t_{OEASRRi}$	Asynchronous Set/Reset Recovery	—	2.50	—	2.50	—	2.50	—	4.17	ns
$t_{OEBYPASS}$	Register/Latch Bypass Delay	—	0.00	—	0.00	—	0.00	—	0.00	ns
t_{OECEHi}	Register Clock Enable Hold Time	1.30	—	1.30	—	0.80	—	1.33	—	ns
t_{OECESi}	Register Clock Enable Setup Time (Global Clock Enable)	1.20	—	1.20	—	1.20	—	2.00	—	ns
t_{OECESi_PT}	Register Clock Enable Setup Time (Product Term Clock Enable)	1.50	—	1.50	—	2.10	—	3.50	—	ns
t_{OECOi}	Register Clock to Output Delay	—	1.30	—	1.30	—	1.60	—	2.67	ns
t_{OEHi}	Register Hold Time	0.40	—	0.40	—	0.40	—	0.67	—	ns
t_{OELGOi}	Latch Gate to Output Delay	—	1.60	—	1.60	—	1.60	—	2.67	ns
t_{OELHi}	Latch Hold Time	0.40	—	0.40	—	0.40	—	0.67	—	ns
t_{OELPDi}	Latch Propagation Delay (Transparent Mode)	—	0.30	—	0.30	—	0.30	—	0.50	ns

ispGDX2V/B/C, ispGDX2EV/EB/EC Internal Timing Parameters[1] (Continued)

Over Recommended Operating Conditions

Parameter	Description	-3		-32		-35		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{OELSi}	Latch Setup Time (Global Gate)	1.40	—	1.40	—	1.40	—	2.33	—	ns
t_{OELSi_PT}	Latch Setup Time (Product Term Gate)	1.00	—	1.00	—	1.00	—	1.67	—	ns
t_{OESi}	Register Setup Time (Global Clock)	1.00	—	1.00	—	1.40	—	2.33	—	ns
t_{OESi_PT}	Register Setup Time (Product Term Clock)	1.00	—	1.00	—	1.00	—	1.67	—	ns
$t_{OESRPWi}$	Asynchronous Set/Reset Pulse Width	—	2.50	—	2.50	—	2.50	—	4.17	ns

Timing v.2.2

1. Internal parameters are not tested and are for reference only. Refer to the timing model in this data sheet for details.
2. t_{PLL_DELAY} is the unit of increment by which the clock signal can be incremented. The PLL can adjust the clock signal by up to t_{RANGE} (as given in the sysCLOCK PLL Timing section) in either direction in steps of size t_{PLL_DELAY}.

ispGDX2V/B/C, ispGDX2EV/EB/EC Timing Adjusters

Parameter	Description	-3		-32		-35		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Optional Adders										
t_{INDIO}	Input Delay	—	1.50	—	1.50	—	1.50	—	2.50	ns
$t_{PLL\_SEC\_DELAY}$	Secondary PLL Output Delay	—	1.30	—	1.30	—	1.30	—	1.30	ns
t_{IOO} Output Adjusters										
Slow Slew	Using Slow Slew (LVTTL and LVCMOS Outputs Only)	—	0.90	—	0.90	—	0.90	—	0.90	ns
LVTTL_out	Using 3.3V TTL Drive	—	1.20	—	1.20	—	1.20	—	1.20	ns
LVCMOS_18_4mA_out	Using 1.8V CMOS Standard, 4mA Drive	—	0.30	—	0.30	—	0.30	—	0.30	ns
LVCMOS_18_5.33mA_out	Using 1.8V CMOS Standard, 5.33mA Drive	—	0.30	—	0.30	—	0.30	—	0.30	ns
LVCMOS_18_8mA_out	Using 1.8V CMOS Standard, 8mA Drive	—	0.00	—	0.00	—	0.00	—	0.00	ns
LVCMOS_18_12mA_out	Using 1.8V CMOS Standard, 12mA Drive	—	0.00	—	0.00	—	0.00	—	0.00	ns
LVCMOS_25_4mA_out	Using 2.5V CMOS Standard, 4mA Drive	—	1.20	—	1.20	—	1.20	—	1.20	ns
LVCMOS_25_5.33mA_out	Using 2.5V CMOS Standard, 5.33mA Drive	—	1.00	—	1.00	—	1.00	—	1.00	ns
LVCMOS_25_8mA_out	Using 2.5V CMOS Standard, 8mA Drive	—	0.40	—	0.40	—	0.40	—	0.40	ns
LVCMOS_25_12mA_out	Using 2.5V CMOS Standard, 12mA Drive	—	0.40	—	0.40	—	0.40	—	0.40	ns
LVCMOS_25_16mA_out	Using 2.5V CMOS Standard, 16mA Drive	—	0.40	—	0.40	—	0.40	—	0.40	ns
LVCMOS_33_4mA_out	Using 3.3V CMOS Standard, 4mA Drive	—	1.20	—	1.20	—	1.20	—	1.20	ns
LVCMOS_33_5.33mA_out	Using 3.3V CMOS Standard, 5.33mA Drive	—	1.20	—	1.20	—	1.20	—	1.20	ns
LVCMOS_33_8mA_out	Using 3.3V CMOS Standard, 8mA Drive	—	0.80	—	0.80	—	0.80	—	0.80	ns
LVCMOS_33_12mA_out	Using 3.3V CMOS Standard, 12mA Drive	—	0.60	—	0.60	—	0.60	—	0.60	ns
LVCMOS_33_16mA_out	Using 3.3V CMOS Standard, 16mA Drive	—	0.60	—	0.60	—	0.60	—	0.60	ns
LVCMOS_33_20mA_out	Using 3.3V CMOS Standard, 20mA Drive	—	0.30	—	0.30	—	0.30	—	0.30	ns
AGP_1X_out	Using AGP 1x Standard	—	0.60	—	0.60	—	0.60	—	0.60	ns
BLVDS_out	Using Bus Low Voltage Differential Signaling (BLVDS)	—	1.00	—	1.00	—	1.00	—	1.00	ns
CTT25_out	Using CTT 2.5v	—	0.30	—	0.30	—	0.30	—	0.30	ns
CTT33_out	Using CTT 3.3v	—	0.20	—	0.20	—	0.20	—	0.20	ns
GTL+_out	Using GTL+	—	0.50	—	0.50	—	0.50	—	0.50	ns
HSTL_I_out	Using HSTL 2.5V, Class I	—	0.50	—	0.50	—	0.50	—	0.50	ns
HSTL_III_out	Using HSTL 2.5V, Class III	—	0.60	—	0.60	—	0.60	—	0.60	ns
HSTL_IV_out	Using HSTL 2.5V, Class IV	—	0.60	—	0.60	—	0.60	—	0.60	ns

ispGDX2V/B/C, ispGDX2EV/EB/EC Timing Adjusters (Continued)

Parameter	Description	-3		-32		-35		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
LVPECL_out	Using LVPECL Differential Signaling	—	0.30	—	0.30	—	0.30	—	0.30	ns
LVDS_out	Using Low Voltage Differential Signaling (LVDS)	—	0.80	—	0.80	—	0.80	—	0.80	ns
PCI_out	Using PCI Standard	—	0.60	—	0.60	—	0.60	—	0.60	ns
PCI_X_out	Using PCI-X Standard	—	0.60	—	0.60	—	0.60	—	0.60	ns
SSTL2_I_out	Using SSTL 2.5V, Class I	—	0.30	—	0.30	—	0.30	—	0.30	ns
SSTL2_II_out	Using SSTL 2.5V, Class II	—	0.50	—	0.50	—	0.50	—	0.50	ns
SSTL3_I_out	Using SSTL 3.3V, Class I	—	0.20	—	0.20	—	0.20	—	0.20	ns
SSTL3_II_out	Using SSTL 3.3V, Class II	—	0.40	—	0.40	—	0.40	—	0.40	ns
t_{IOI} Input Adjusters										
LVTTL_in	Using 3.3V TTL	—	0.00	—	0.00	—	0.00	—	0.00	ns
LVCMOS_18_in	Using 1.8V CMOS	—	0.00	—	0.00	—	0.00	—	0.00	ns
LVCMOS_25_in	Using 2.5V CMOS	—	0.00	—	0.00	—	0.00	—	0.00	ns
LVCMOS_33_in	Using 3.3V CMOS	—	0.00	—	0.00	—	0.00	—	0.00	ns
AGP_1X_in	Using AGP 1x	—	1.00	—	1.00	—	1.00	—	1.00	ns
BLVDS_in	Using Bus Low Voltage Differential Signaling (BLVDS)	—	0.50	—	0.50	—	0.50	—	0.50	ns
CTT25_in	Using CTT 2.5V	—	1.00	—	1.00	—	1.00	—	1.00	ns
CTT33_in	Using CTT 3.3V	—	1.00	—	1.00	—	1.00	—	1.00	ns
GTL+_in	Using GTL+	—	0.50	—	0.50	—	0.50	—	0.50	ns
HSTL_I_in	Using HSTL 2.5V, Class I	—	0.50	—	0.50	—	0.50	—	0.50	ns
HSTL_III_in	Using HSTL 2.5V, Class III	—	0.60	—	0.60	—	0.60	—	0.60	ns
HSTL_IV_in	Using HSTL 2.5V, Class IV	—	0.60	—	0.60	—	0.60	—	0.60	ns
LVPECL_in	Using Differential Signaling (LVPECL)	—	0.00	—	0.00	—	0.00	—	0.00	ns
LVDS_in	Using Low Voltage Differential Signaling (LVDS)	—	0.50	—	0.50	—	0.50	—	0.50	ns
PCI_in	Using PCI	—	1.00	—	1.00	—	1.00	—	1.00	ns
PCI_X_in	Using PCI-X	—	1.00	—	1.00	—	1.00	—	1.00	ns
SSTL2_I_in	Using SSTL 2.5V, Class I	—	0.50	—	0.50	—	0.50	—	0.50	ns
SSTL2_II_in	Using SSTL 2.5V, Class II	—	0.50	—	0.50	—	0.50	—	0.50	ns
SSTL3_I_in	Using SSTL 3.3V, Class I	—	0.60	—	0.60	—	0.60	—	0.60	ns
SSTL3_II_in	Using SSTL 3.3V, Class II	—	0.60	—	0.60	—	0.60	—	0.60	ns

Timing v.2.2

ispGDX2V/B/C, ispGDX2EV/EB/EC FIFO Internal Timing

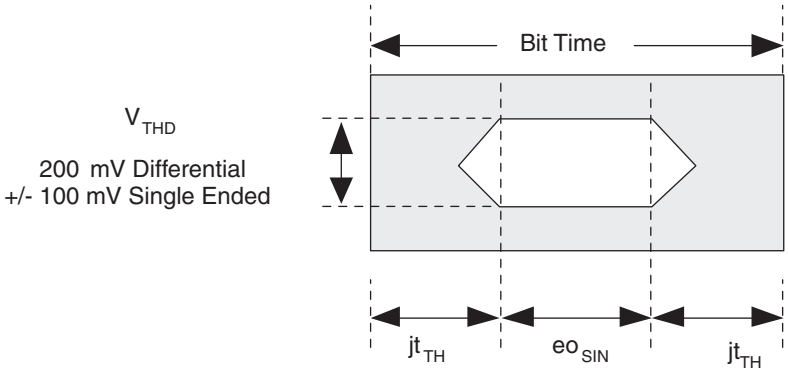
Parameter	Description	-3		-32		-35		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Routing Delays										
$t_{FIFODATAIN}$	FIFO Input Delay	—	0.00	—	0.00	—	0.00	—	0.00	ns
$t_{FIFODATAOUT}$	FIFO Output to I/O Core Delay	—	0.00	—	0.00	—	0.00	—	0.00	ns
$t_{FIFORCLK}$	Read Clock Input Delay	—	0.00	—	0.00	—	0.00	—	0.00	ns
$t_{FIFOREN}$	Read Clock Enable Input Delay	—	0.00	—	0.00	—	0.00	—	0.00	ns
$t_{FIFOWCLK}$	Write Clock Input Delay	—	0.00	—	0.00	—	0.00	—	0.00	ns
$t_{FIFOWEN}$	Write Clock Enable Input Delay	—	0.00	—	0.00	—	0.00	—	0.00	ns
Core Delays										
$t_{FIFOCLKSKEW}$	Global Read Clock to Write Clock Skew	—	2.00	—	2.00	—	2.00	—	3.33	ns
$t_{FIFOEMPTY}$	Read Clock to Empty Flag Delay	—	1.30	—	1.80	—	1.80	—	3.00	ns
$t_{FIFOFULL}$	Write Clock to Full Flag Delay	—	1.30	—	1.80	—	1.80	—	3.00	ns
$t_{FIFORCEH}$	Read Clock Hold after Read Clock Enable Time	—	0.00	—	0.00	—	0.00	—	0.00	ns
$t_{FIFORCES}$	Read Clock Setup before Read Clock Enable Time	—	1.50	—	1.50	—	1.50	—	2.50	ns
$t_{FIFORCLKO}$	Read Clock to FIFO Out Delay	—	0.50	—	0.50	—	0.50	—	0.83	ns
$t_{FIFORSTO}$	Reset to Output Delay	—	0.70	—	0.70	—	0.70	—	1.17	ns
$t_{FIFORSTPW}$	Reset Pulse Width	—	2.00	—	2.00	—	2.00	—	3.33	ns
$t_{FIFORSTR}$	Reset Recovery Time	—	1.20	—	1.50	—	2.00	—	3.33	ns
$t_{FIFOSTRD}$	Write Clock to Start Read Flag Delay	—	0.00	—	0.00	—	0.00	—	0.00	ns
$t_{FIFOTHRU}$	Flow Through Delay	—	0.00	—	0.00	—	0.00	—	0.00	ns
$t_{FIFOWCEH}$	Write Clock hold after Write Clock Enable Time	—	2.00	—	2.00	—	2.00	—	3.33	ns
$t_{FIFOWCES}$	Write Clock Setup before Write Clock Enable Time	—	0.00	—	0.00	—	0.00	—	0.00	ns
$t_{FIFOWCLKH}$	Write Data Hold after Write Clock Time	—	0.50	—	0.50	—	0.70	—	1.17	ns
$t_{FIFOWCLKS}$	Write Data Setup before Write Clock Time	—	1.00	—	1.00	—	1.00	—	1.67	ns

Timing v.2.2

sysHSI Block Timing

Figure 22 provides a graphical representation of the SERDES receiver input requirements. It provides guidance on a number of input parameters, including signal amplitude and rise time limits, noise and jitter limits, and P and N input skew tolerance.

Figure 22. Receive Data Eye Diagram Template (Differential)



jt_{TH} : Optimum Threshold Crossing Jitter

The data pattern eye opening at the receive end of a link is considered the ultimate measure of received signal quality. Almost all detrimental characteristics of a transmit signal and the interconnection link design result in eye closure. This combined with the eye-opening limitations of the line receiver can provide a good indication of a link's ability to transfer error-free data.

Signal jitter is of special interest to system designers. It is often the primary limiting characteristic of long digital links and of systems with high noise level environments. An interesting characteristic of the clock and data recovery (CDR) portion of the ispGDX2 SERDES receiver is its ability to filter incoming signal jitter that is below the clock recovery PLL bandwidth. For signals with high levels of low frequency jitter, the receiver can detect incoming data error free, with eye openings significantly less than that shown in Figure 22.

sysHSI Block AC Specifications

Operating Frequency Ranges

Symbol	Description	Mode	Test Condition	Min.	Max.	Units
f_{CLK}	Reference Clock Frequency	SS:CAL		50	200	MHz
		10B12B		33	67	MHz
		8B10B		40	80	MHz
f_{SIN}[2]	Serial Input	SS:CAL	with eo_{SIN}	400	800[1]	Mbps
		10B12B	with eo_{SIN}	400	800[1]	Mbps
		8B10B	with eo_{SIN}	400	800[1]	Mbps
f_{SOUT}[2]	Serial Out	LVDS	C_L = 5 pF, R_L = 100 Ohms, f_{CLK} with no jitter	400	800[1]	Mbps

1. f_{SIN} (8B/10B and 10B/12B) 800Mbps limit applicable only to the fastest speed grade. Limit is 700Mbps for the lower speed grade.
2. f_{SIN} and f_{SOUT} speeds are supported at V_{CC} and V_{CCP} at 1.7V to 1.9V for ispGDX2C devices.

LOCKIN Time

Symbol	Description	Mode	Condition	Min.	Max.	Units
t_{SCLOCK}	CSPLL Lock Time	All	After input is stabilized		25	µS
$t_{CDRLOCK}$	CDRPLL Lock-in Time	SS	With SS mode sync pattern		1024	t_{RCP}[1]
		10B12B	With 10B12B sync pattern		1024	t_{RCP}
		8B10B	With 8B10B idle pattern		960	t_{RCP}
t_{SYNC}	SyncPat Length	SS		1200		t_{RCP}
t_{CAL}	CAL Duration	SS		1100		t_{RCP}
t_{SUSYNC}	SyncPat Set-up Time to CAL	SS		50		t_{RCP}
t_{HDSYNC}	SyncPat Hold Time from CAL	SS		50		t_{RCP}

1. REFCLK clock period.

REFCLK and SS_CLKIN Timing

Symbol	Description	Mode	Condition	Min.	Max.	Units
$t_{DREFCLK}$	Frequency Deviation Between TX REFCLK and CDRX REFCLK on One Link	8B10B/ 10B12B		-100	100	ppm
$t_{JPPREFCLK}$	REFCLK, SS_CLKIN Peak-to-Peak Period Jitter	All	Random Jitter		0.01	UIPP
$t_{PWREFCLK}$	REFCLK, SS_CLKIN Pulse Width, (80% to 80% or 20% to 20%).	All		1		ns
$t_{RFREFCLK}$	REFCLK, SS_CLKIN Rise/Fall Time (20% to 80% or 80% to 20%)	All			2	ns

Serializer Timing[2]

Symbol	Description	Mode	Condition	Min.	Max.	Units
$t_{JPPSOUT}$	SOUT Peak-to-Peak Output Data Jitter	All	f_{CLK} with no jitter		0.25	UIPP
$t_{JPP8B10B}$	SOUT Peak-to-Peak Random Jitter	8B10B	800 Mbps w/K28.7-		130	ps
	SOUT Peak-to-Peak Deterministic Jitter	8B10B	800 Mbps w/K28.5+		160	ps
t_{RFSOUT}	SOUT Output Data Rise/Fall Time (20%, 80%)	LVDS			700	ps
		BLVDS			900	ps
t_{COSOUT}	REFCLK to SOUT Delay	SS/8B10B		$2Bt^{1}$ + 2	$2Bt^{1}$ +10	ns
		10B12B		$1Bt^{1}$ + 2	$1Bt^{1}$ +10	ns
t_{SKTX}	Skew of SOUT with Respect to SS_CLKOUT	SS			250	ps
$t_{CKOSOUT}$	SS_CLKOUT to bit0 of SOUT	SS		$2Bt^{1}$ - t_{SKTX}	$2Bt^{1}$ + t_{SKTX}	ns
$t_{HSITXDDATAS}$	TXD Data Setup Time	All	Note 3	1.5		ns
$t_{HSITXDDATAH}$	TXD Data Hold Time	All	Note 3		1.0	ns

1. Bt: Bit Time Period. High Speed Serial Bit Time.
2. The SIN and SOUT jitter specifications listed above are under the condition that the clock tree that drives the REFCLK to sysHSI Block is in sysCLOCK PLL BYPASS mode.
3. Internal timing for reference only.

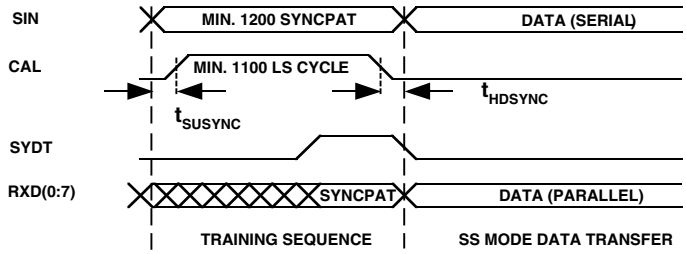
Deserializer Timing

Symbol	Description	Mode	Conditions	Min.	Max.	Units
f_{DSIN}	SIN Frequency Deviation from REFCLK	8B10B/ 10B12B		-100	100	ppm
eo_{SIN}	SIN Eye Opening Tolerance	All	Notes 1, 2	0.45		UIPP
ber	Bit Error Rate	All			10^{-12}	Bits
$t_{HSIOUTVALIDPRE}$	RXD, SYDT Valid Time Before RECCLK Falling Edge	All	Note 3	$t_{RCP}/2$ - 0.7		ns
$t_{HSIOUTVALIDPOST}$	RXD, SYDT Valid Time After RECCLK Falling Edge	All	Note 3	$t_{RCP}/2$ - 0.7		ns
t_{DSIN}	Bit 0 of SIN Delay to RXD Valid at RECCLK Falling edge	All		1.5 t_{RCP} + 4.5Bt + 2	1.5 t_{RCP} + 4.5Bt + 10	ns

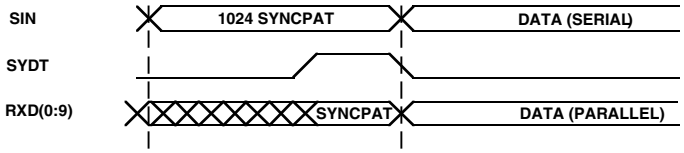
1. Eye opening based on jitter frequency of 100KHz.
2. Lower frequency operation assumes maximum eye closure of 800ps.
3. Internal timing for reference only.

Lock-in Timing

CDRX_SS LOCK-IN (DE-SKEW) TIMING

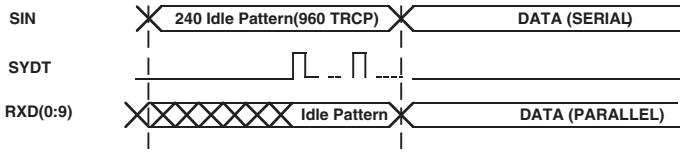


CDR_10B12B LOCK-IN TIMING



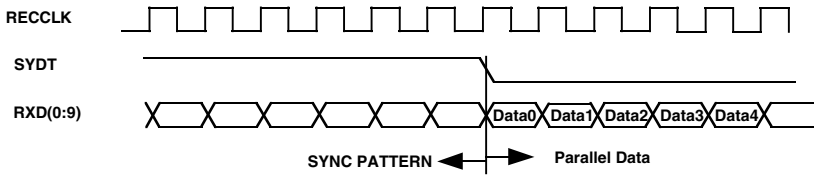
Lock-in Timing (Continued)

CDR_8B10B LOCK-IN TIMING

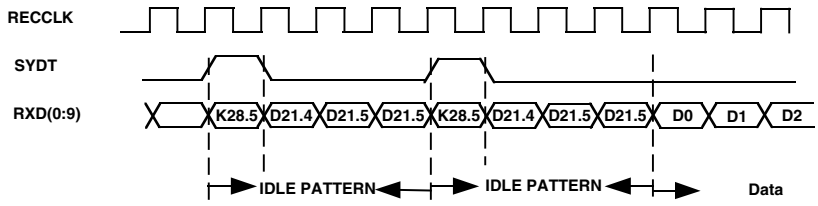


SYDT Timing

SYDT TIMING FOR CDRX_10B12B

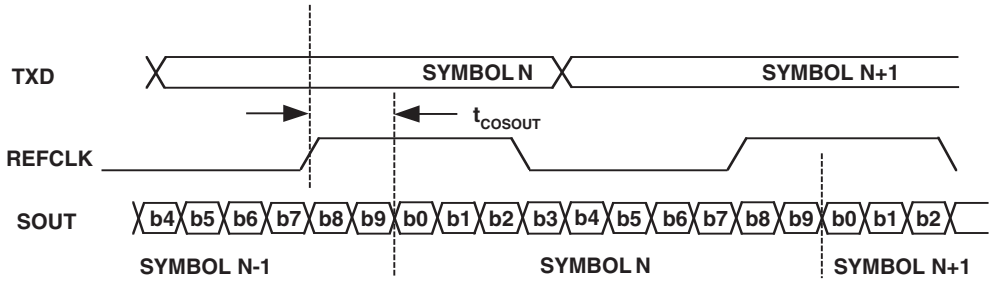


SYDT TIMING FOR CDRX_8B10B

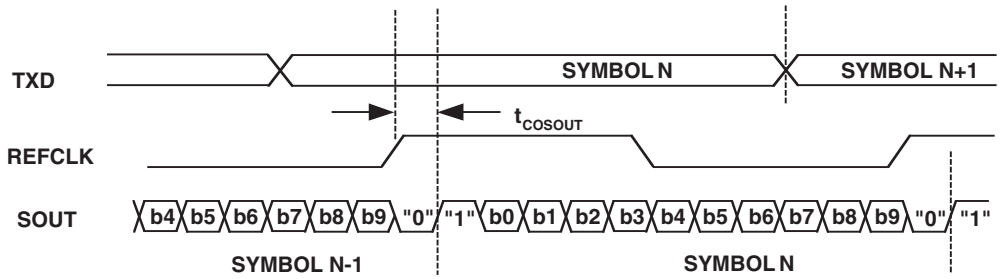


Serializer Timing

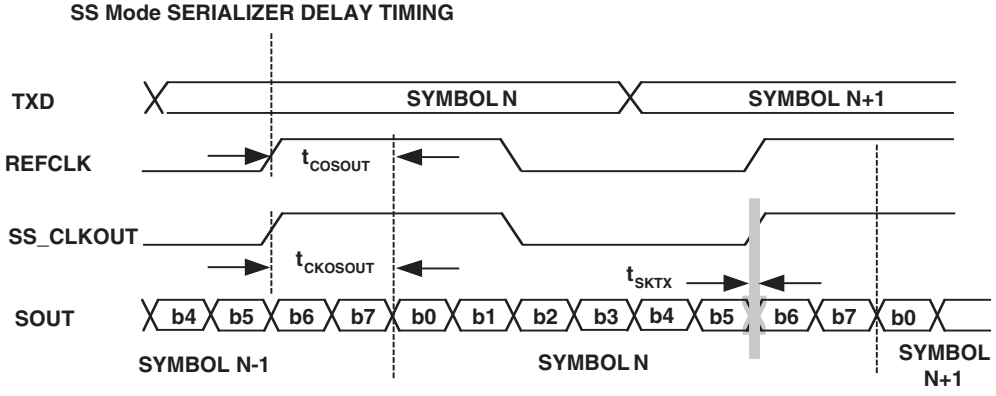
8B/10B SERIALIZER DELAY TIMING



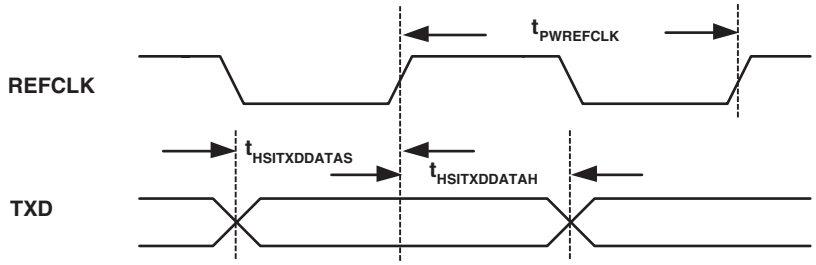
10B/12B SERIALIZER DELAY TIMING



SS Mode SERIALIZER DELAY TIMING

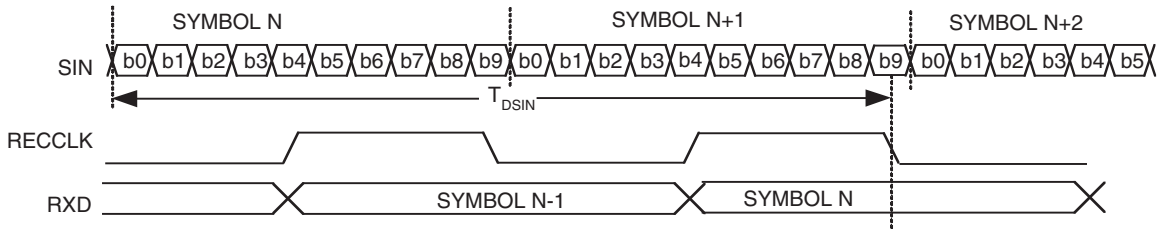


INTERNAL TIMING FOR sysHSI BLOCK

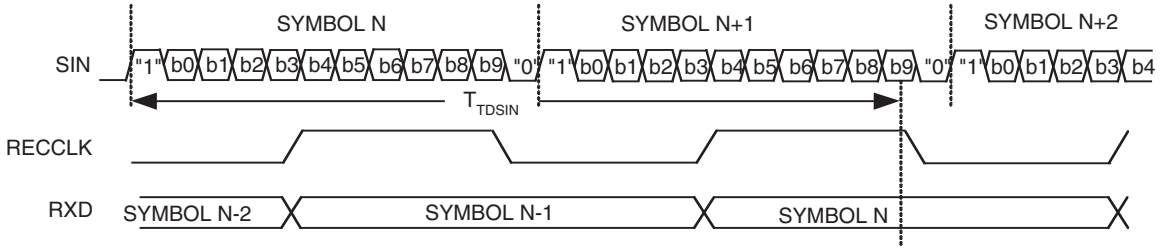


Deserializer Timing

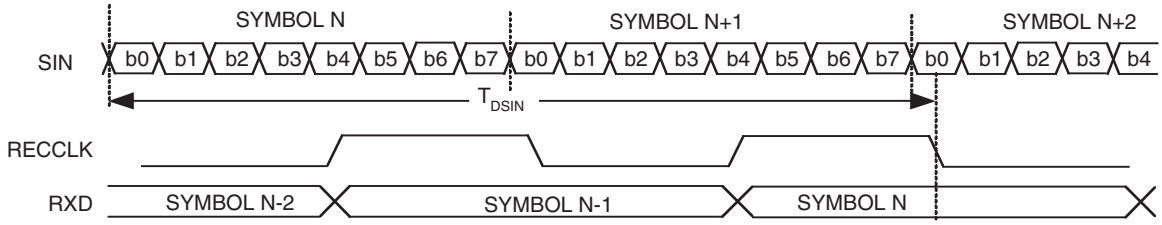
8B/10B DESERIALIZER DELAY TIMING



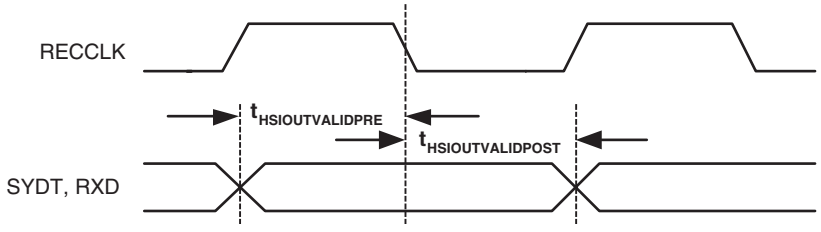
10B/12B DESERIALIZER DELAY TIMING



CDRX_SS DESERIALIZER DELAY TIMING



INTERNAL TIMING FOR sysHSI BLOCK



sysCLOCK PLL Timing

Over Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Units
t_{PWH}	Input clock, high time	80% to 80%	0.5	—	ns
t_{PWL}	Input clock, low time	20% to 20%	0.5	—	ns
t_R, t_F	Input Clock, rise and fall time	20% to 80%	—	3.0	ns
t_{INSTB}	Input clock stability, cycle to cycle (peak)		—	+/- 300	ps
f_{MDIVIN}	M Divider input, frequency range		10	320	MHz
$f_{MDIVOUT}$	M Divider output, frequency range		10	320	MHz
f_{NDIVIN}	N Divider input, frequency range		10	320	MHz
$f_{NDIVOUT}$	N Divider output, frequency range		10	320	MHz
f_{VDIVIN}	V Divider input, frequency range		100	400	MHz
$f_{VDIVOUT}$	V Divider output, frequency range		10	320	MHz
$t_{OUTDUTY}$	Output clock, duty cycle		40	60	%
$t_{JIT(CC)}$	Output clock, cycle to cycle jitter (peak)	Clean reference[1]: 10 MHz ≤ $f_{MDIVOUT}$ ≤ 40 MHz or 100 MHz ≤ f_{VDIVIN} ≤ 160 MHz	—	+/- 600	ps
		Clean reference[1]: 40 MHz ≤ $f_{MDIVOUT}$ ≤ 320 MHz and 160 MHz ≤ f_{VDIVIN} ≤ 400 MHz	—	+/- 150	ps
$T_{JIT(PERIOD)}$[2]	Output clock, period jitter (peak)	Clean reference[1]: 10 MHz ≤ $f_{MDIVOUT}$ ≤ 40 MHz or 100 MHz ≤ f_{VDIVIN} ≤ 160 MHz	—	+/- 600	ps
		Clean reference[1]: 40 MHz ≤ $f_{MDIVOUT}$ ≤ 320 MHz and 160 MHz ≤ f_{VDIVIN} ≤ 400 MHz	—	+/- 150	ps
$t_{CLK\_OUT\_DLY}$	Input clock to CLK_OUT delay	Internal feedback	—	3.4	ns
t_{PHASE}	Input clock to external feedback delta	External feedback	—	500	ps
t_{LOCK}	Time to acquire phase lock after input stable		—	25	us
t_{PLL_DELAY}	Delay increment (Lead/Lag)	Typical = +/- 250ps	+/- 120	+/- 550	ps
t_{RANGE}	Total output delay range (lead/lag)		+/- 0.84	+/- 3.85	ns
t_{PLL_RSTW}	Minimum reset pulse width		1.8	—	ns

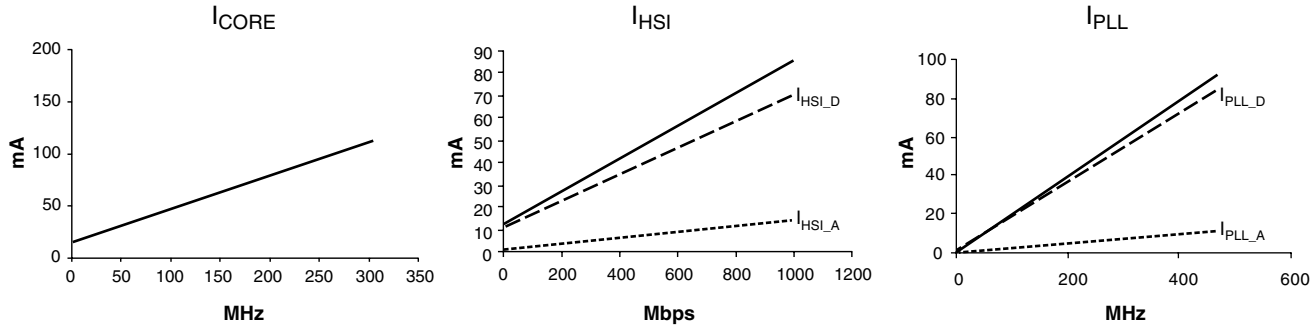
1. This condition assures that the output phase jitter will remain within specification. Jitter specification is based on optimized M, N and V settings determined by the ispLEVER software.
2. Accumulated jitter measured over 10,000 waveform samples

Boundary Scan Timing Specifications

Over Recommended Operating Conditions

Parameter	Description	Min	Max	Units
t_{BTCP}	TCK [BSCAN] clock pulse width	40	—	ns
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	8	—	ns
t_{BTH}	TCK [BSCAN] hold time	10	—	ns
t_{BTRF}	TCK [BSCAN] rise/fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	10	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

Power Consumption



Power Estimation Coefficients – Core and PLL

Device	V_{CC}	I_{DC} (mA)	K_{REF}	K_{IN}	K_{CORE}	K_{PLLD}	K_{PLLA}
ispGDX2-256	3.3	10.0	3.25	0.0139	0.292	0.157	0.024
	2.5	10.0	3.13	0.0139	0.292	0.157	0.024
	1.8	4.0	3.00	0.0213	0.239	0.179	0.024

I_{DC}: Blank chip background current
K_{REF}: Reference voltage circuit current per bank
K_{IN}: I/O current per input per MHz
K_{CORE}: Core current per MHz with GRP fanout of 1
K_{PLLD}: PLL logic current per MHz per PLL
K_{PLLA}: PLL analog portion current per MHz per PLL

Power Estimation Coefficients – sysHSI

Device	V_{CC}	K_{RXD}	K_{RXSTBY}	K_{RXA}	K_{TXD}	K_{TXSTBY}	K_{TXA}
ispGDX2-256	3.3	0.027	1.3	0.0023	0.011	2.4	0.0018
	2.5	0.027	1.3	0.0023	0.011	2.4	0.0018
	1.8	0.019	3.7	0.0040	0.011	1.2	0.0023

K_{RXD}: Receiver Logic current per Mbps
K_{RXSTBY}: Receiver Logic standby current
K_{RXA}: Receiver Analog portion current per Mbps
K_{TXD}: Transmitter Logic current per Mbps
K_{TXSTBY}: Transmitter Logic standby current
K_{TXA}: Transmitter Analog portion current per Mbps

Power Consumption (Continued)

Power consumption in the ispGDX2 family is the sum of three components:

$I_{CC\text{-}TOTAL} = I_{CORE} + I_{PLL} + I_{HSI}$ ($I_{CC\text{-}TOTAL}$ combines current supplied via V_{CC} pins and V_{CCP} pins)

$I_{CORE} = I_{DC} + I_{REF} + I_{IN}$
= Blank chip background current
+ K_{REF} * Number of Banks with V_{REF} active
+ (K_{IN} * Number of inputs + K_{CORE}) * Average Input Switching Frequency (MHz)

$I_{PLL} = I_{PLL\_D} + I_{PLL\_A}$
= [K_{PLLD} * F_{VCO} * Number of PLLs used] + [K_{PLLA} * F_{VCO} * Number of PLLs used]
= [(K_{PLLD} + K_{PLLA}) * F_{VCO}] * Number of PLLs used

$I_{HSI} = I_{RX} + I_{TX}$
= [(K_{RXD} + K_{RXA}) * F_{RX} + I_{RXSTBY}] * Number of Receiver Channels
+ [(K_{TXD} + K_{TXA}) * F_{TX} + I_{TXSTBY}] * Number of Transmitter Channels

Where:

F_{VCO}: sysClock PLL VCO Frequency in MHz
F_{RX}: sysHSI Receiver Serial Data Rate
F_{TX}: sysHSI Transmitter Serial Data Rate

I_{HSI} can also be determined by calculating I_{HSI_D}, the current supplied by the V_{CC} pin, and I_{HSI_A}, the current supplied by the V_{CCP0} and V_{CCP1}.

$I_{HSI} = I_{HSI\_D} + I_{HSI\_A}$
= [(K_{RXD} * F_{RX} + I_{RXSTBY})* Number of Receiver Channels
+ (K_{TXD} * F_{TX} + I_{TXSTBY}) * Number of Transmitter Channels]
+[(K_{RXA} * F_{RX}) * Number of Receiver Channels
+ (K_{TXA} * F_{TX}) * Number of Transmitter Channels]

The I_{CCP} is supplied through V_{CCP0} and V_{CCP1} pins for PLL and sysHSI analog portion. The equation for I_{CCP} can be derived from the equations below.

$I_{CCP} = I_{PLL\_A} + I_{HSI\_A}$
= [(K_{PLLA} * F_{VCO}) * Number of PLLs used]
+ [(K_{RXA} * F_{RX}) * Number of Receiver Channels
+ (K_{TXA} * F_{TX}) * Number of Transmitter Channels]

Where:

I_{PLL_A}: PLL Analog Portion Current
I_{HSI_A}: HSI Analog Portion Current

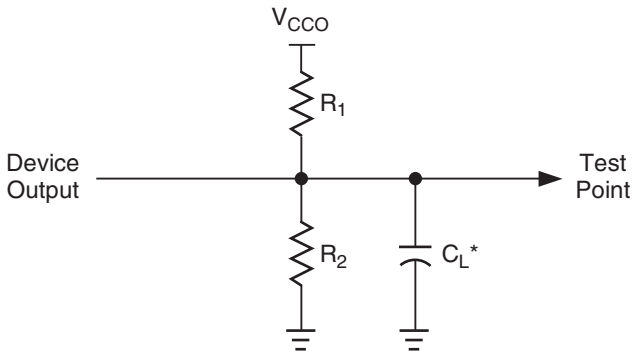
Note: For further information about the use of these coefficients, refer to Technical Note TN1034, *Power Estimation in the ispGDX2 Family.*

$I_{CC\text{-}TOTAL}$ estimates are based on typical conditions. These values are for estimates only. Since the value of $I_{CC\text{-}TOTAL}$ is sensitive to operating conditions and the program in the device, the actual current should be verified.

Switching Test Conditions

Figure 23 shows the output test load used for AC testing. Specific values for resistance, capacitance, voltage and other test conditions are shown in Table 7.

Figure 23. Output Test Load, LVTTL and LVCMOS Standards (1.8V)



*C_L includes Test Fixture and Probe Capacitance.

Table 7. Test Fixture Required Components

Test Condition	R_1	R_2	C_L	Timing Ref.	V_{CCO}
Default LVCMOS 1.8 I/O (L -> H, H -> L)	106	106	35pF	$V_{CCO}/2$	1.8V
LVCMOS I/O (L -> H, H -> L)	—	—	35pF	LVCMOS3.3 = 1.5V	LVCMOS3.3 = 3.0V
				LVCMOS2.5 = $V_{CCO}/2$	LVCMOS2.5 = 2.3V
				LVCMOS1.8 = $V_{CCO}/2$	LVCMOS1.8 = 1.65V
Default LVCMOS 1.8 I/O (Z -> H)	—	106	35pF	$V_{CCO}/2$	1.65V
Default LVCMOS 1.8 I/O (Z -> L)	106	—	35pF	$V_{CCO}/2$	1.65V
Default LVCMOS 1.8 I/O (H -> Z)	—	106	5pF	V_{OH} - 0.15	1.65V
Default LVCMOS 1.8 I/O (L -> Z)	106	—	5pF	V_{OL} + 0.15	1.65V

Note: Output test conditions for all other interfaces are determined by the respective standards.

Signal Descriptions[1]

Signal Names	Description
General Purpose	
BKx_IOy	Input/Output – General purpose I/O number y in I/O Bank X.
GCLK/CE0, GCLK/CE1, GCLK/CE2, GCLK/CE3	Input – Global clock/clock enable inputs.
SEL0, SEL1, SEL2[2], SEL3[2]	Input – Global MUX select inputs.
GOE0, GOE1, GOE2[2], GOE3[2]	Input – Global output enable inputs.
RESETb	Input – Global RESET signal (active low).
NC	No connect.
GND	GND – Ground.
V_{CC}	VCC – The power supply pins for core logic.
V_{CCJ}	VCC – The power supply for the JTAG logic.
V_{CCOx}	VCC – The power supply pins for I/O Bank X.
V_{REFx}	Input – Defines the reference voltage for I/O Bank X.
Testing and Programming	
TMS	Input – Test Mode Select input, used to control the 1149.1 state machine.
TCK	Input – Test Clock Input pin, used to clock the 1149.1 state machine.
TDI	Input – Test Data In pin, used to load data into device using 1149.1 state machine.
TDO	Output – Test Data Out pin used to shift data out of device using 1149.1.
TOE	Input – Test Output Enable pin. TOE tristates all I/O pins when driven low.
PLL Functions	
PLL_FBKz	Input – Optional feedback input allows external feedback for PLL z.
PLL_RSTz	Input – Optional input resets the M divider in PLL z.
CLK_OUTz	Output – Optional clock output from PLL z (clock signal occupies the input path of this I/O pad).
PLL_LOCKz	Output – Optional lock output from PLL z (lock signal occupies the input path of this I/O pad).
GND_{P0}, GND_{P1}	GND – Ground for PLLs.
V_{CCP0}, V_{CCP1}	VCC – The power supply pins for PLLs.
FIFO Functions	
FIFOy_DIN*w*	Input – DATA IN Bit w of FIFO y.
FIFOy_DOUT*w*	Internal Signal – DATA OUT Bit w of FIFO y
FIFOy_FIFORSTb	Input – Reset input for FIFO y (active low).
FIFOy_FULL	Output – FULL flag for FIFO y.
FIFOy_EMPTY	Output – EMPTY flag for FIFO y.
FIFOy_STRDb	Output – Start read (STRDb) flag for FIFO y.
SERDES Functions	
HSImA_SINP, HSImB_SINP	Input – Positive sense serial input for sysHSI BLOCK m channel A, B.
HSImA_SINN, HSImB_SINN	Input – Negative (minus) sense serial input for sysHSI BLOCK m channel A, B.
HSImA_SOUTP, HSImB_SOUTP	Output – Positive sense serial output for sysHSI BLOCK m channel A, B.
HSImA_SOUTN, HSImB_SOUTN	Output – Negative (minus) sense serial output for sysHSI BLOCK m channel A, B.
HSImA_SYDT, HSImB_ SYDT	Output – Symbol alignment detect for sysHSI BLOCK m channel A, B.
HSImA_RECCLK, HSImB_RECCLK	Internal Signal – Recovered clock for sysHSI BLOCK m channel A, B.
HSImA_CDRRSTb, HSImB_CDRRSTb	Input – Resets the CDR circuit of sysHSI BLOCK m channel A, B.
HSIm_CSLOCK	Output – LOCK output of the PLL associated with channel m.

Signal Descriptions[1] (Continued)

Signal Names	Description
HSImA_TXDw, HSImB_ TXD*w*	Internal Signal – Parallel data in bit w for sysHSI BLOCK m channel A, B.
HSImA_RXDw, HSImB_ RXD*w*	Internal Signal – Parallel data out bit w for sysHSI BLOCK m channel A, B.
Source Synchronous Functions	
SS_SCLKIN0P, SS_SCLKIN1P	Input – Positive sense clock input for Source Synchronous group A, B.
SS_SCLKIN0N, SS_SCLKIN1N	Input – Negative (minus) sense clock input for Source Synchronous group A, B.
SS_CLKOUT0N, SS_CLKOUT1P	Output – Positive sense clock output for Source Synchronous group A, B.
SS_CLKOUT0N, SS_CLKOUT1N	Output – Negative (minus) sense clock output for Source Synchronous group A, B.
CAL	Input – Initiates source synchronous calibration sequence.

1. m, w, x, y and z are variables.
2. Not on ispGDX2-64

ispGDX2-64 Power Supply and NC Connections[1]

Signal	ispGDX2-64 (100-Ball fpBGA)[2]
V_{CC}	A1, K10
V_{CCO0}	J7
V_{CCO1}	F10
V_{CCO2}	E10
V_{CCO3}	B7
V_{CCO4}	B4
V_{CCO5}	E1
V_{CCO6}	F1
V_{CCO7}	K4
V_{CCJ}	K1
V_{CCP0}	G6
GND_{P0}	G5
GND	A10, B9, C8, E6, E5, F6, F5, H3, J2

1. All grounds must be electrically connected at the board level.
2. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.

ispGDX2 Power Supply and NC Connections[1]

Signal	ispGDX2-128 (208-Ball fpBGA)[3]	ispGDX2-256 (484-Ball fpBGA)[3]
V_{CC}	B15, C14, R15, B2, C3, P3, R2,	AA3, AA20, B3, B20, C2, C11, C12, C21, H9, H10, H11, H12, H13, H14, J8, J15, K8, K15, L8, L15, L20, M3, M8, M15, M20, N8, N15, P8, P15, R9, R10, R11, R12, R13, R14, Y2, Y11, Y12, Y21
V_{CCO0}	N11, T12	AA14, AB20, Y17
V_{CCO1}	L13, M16	P21, U20, Y22
V_{CCO2}	E16, F13	C22, E20, J21
V_{CCO3}	A12, D11	A20, B14, C17
V_{CCO4}	A5, D6	A3, B9, C6
V_{CCO5}	E1, F4	C1, F3, J2
V_{CCO6}	L4, M1	P2, U3, Y1
V_{CCO7}	N6, T5	AA9, AB3, Y6
V_{CCJ}	P14	L3
V_{CCP0}	J1	K1
V_{CCP1}	J16	N22
GND_{P0}	H1	J1
GND_{P1}	H16	K22
GND	A16, D13, H15, J15, N13, T16, A1, B9, B8, D4, H2, J2, N4, R8, R9, T1, G7, G8, G9, G10, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10	A2, A11, A12, A21, A1, A22, AA1, AA2, AA11, AA12, AA21, AA22, AB1, AB2, AB11, AB12, AB21, AB22, B1, B2, B11, B12, B21, B22, C3, C20, D4, D19, E5, E18, F6, F17, G7, G16, H8, H15, J9, J10, J11, J12, J13, J14, K9, K10, K11, K12, K13, K14, L1, L2, L7, L9, L10, L11, L12, L13, L14,L16, L21, L22, M1, M2, M7, M9, M10, M11, M12,M13, M14, M16, M21, M22, N9, N10, N11, N12, N13, N14, P9, P10, P11, P12, P13, P14, R8, R15, T7, T16, U6, U17, V5, V18, W4, W19,Y3, Y20
NC[2]	A11, B16	D8, D11, E6, E7, E8, E9, E12, E13, E14, E15, E16, F7, F16, G5, G6, G18, G19, H19, K4, K19, L19, M4, M19, N4, P4, P19, R4, R18, T4, T5, T17, T18, U5, U7, U16, V7, V8, V9, V10, V11, V12, V15, V16, V17, W14, Y18

1. All grounds must be electrically connected at the board level.
2. NC pins should not be connected to any active signals, V_{CC} or GND.
3. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.

ispGDX2-64 Logic Signal Connections

Signal Name	sysIO Bank	LVDS Pair/Polarity	GDX Block	MRB	SERDES Mode I/O Pin[1]	SERDES Mode I/O Cell[2]	FIFO Mode I/O Cell/Pin[3]	100 fpBGA
GOE0	-	-	-	-	-	-	-	H6
BK0_IO0/PLL_LOCK0	0	0N	0A	0	-	-	FIFO0_FULL	J6
BK0_IO1	0	0P	0A	1	HSI0A_CDRRSTb	-	FIFO0_FIFORSTb	K6
GND	0	-	-	-	-	-	-	GND
BK0_IO2	0	1N	0A	2	HSI0A_SINN	HSI0A_RECCLK	-	G7
BK0_IO3	0	1P	0A	3	HSI0A_SINP	-	-	H7
GND	0	-	-	-	-	-	-	GND
BK0_IO4/PLL_RST0	0	2N	0A	4	-	HSI0A_RXD0/TXD0	FIFO0_DIN0/DOUT0	K7
BK0_IO5	0	2P	0A	5	-	HSI0A_RXD1/TXD1	FIFO0_DIN1/DOUT1	K8
BK0_IO6	0	3N	0A	6	-	HSI0A_RXD2/TXD2	FIFO0_DIN2/DOUT2	J8
BK0_IO7	0	3P	0A	7	Note 4	HSI0A_RXD3/TXD3	FIFO0_DIN3/DOUT3	K9
GND	0	-	-	-	-	-	-	GND
TCK	-	-	-	-	-	-	-	J10
RESETb	-	-	-	-	-	-	-	J9
BK1_IO0/PLL_FBK0	1	4P	0A	8	HSI0A_SYDT[5]	HSI0A_RXD4/TXD4	FIFO0_DIN4/DOUT4	H10
BK1_IO1	1	4N	0A	9	-	HSI0A_RXD5/TXD5	FIFO0_DIN5/DOUT5	H9
BK1_IO2	1	5P	0A	10	-	HSI0A_RXD6/TXD6	FIFO0_DIN6/DOUT6	H8
BK1_IO3/VREF(0,1)	1	5N	0A	11	FIFO0_STRDb[6]	HSI0A_RXD7/TXD7	FIFO0_DIN7/DOUT7	G10
GND	1	-	-	-	-	-	-	GND
BK1_IO4	1	6P	0A	12	HSI0A_SOUTP	HSI0A_RXD8/TXD8	FIFO0_DIN8/DOUT8	G9
BK1_IO5	1	6N	0A	13	HSI0A_SOUTN	HSI0A_RXD9/TXD9	FIFO0_DIN9/DOUT9	G8
GND	1				-	-	-	GND
BK1_IO6	1	7P	0A	14	SS_CLKIN1P	HSI0A_SYDT[5]	-	F9
BK1_IO7	1	7N	0A	15	SS_CLKIN1N	-	FIFO0_ EMPTY	F8
GCLK/CE2	-	CLK2P	-	-	-	-	-	F7
GCLK/CE3	-	CLK2N	-	-	-	-	-	E7
BK2_IO0	2	8N	0B	0	SS_CLKOUT0N	-	FIFO1_FULL	E8
BK2_IO1	2	8P	0B	1	SS_CLKOUT0P	-	FIFO1_EMPTY	E9
GND	2	-	-	-	-	-	-	GND
BK2_IO2	2	9N	0B	2	HSI0B_SOUTN	HSI0BA_SYDT[5]	-	D8
BK2_IO3	2	9P	0B	3	HSI0B_SOUTP	HSI0B_RXD0/TXD0	FIFO1_DIN0	D9
GND	2	-	-	-	-	-	-	GND
BK2_IO4/V_{REF} (2,3)	2	10N	0B	4	-	HSI0B_RXD1/TXD1	FIFO1_DIN1/DOUT1	D10
BK2_IO5	2	10P	0B	5	-	HSI0B_RXD2/TXD2	FIFO1_DIN2/DOUT2	C9
BK2_IO6	2	11N	0B	6	HSI0_CSLOCK	HSI0B_RXD3/TXD3	FIFO1_DIN3/DOUT3	C10
BK2_IO7	2	11P	0B	7	Note 4	HSI0B_RXD4/TXD4	FIFO1_DIN4/DOUT4	B10
BK3_IO0	3	12P	0B	8	-	HSI0B_RXD5/TXD5	FIFO1_DIN5/DOUT5	A9
BK3_IO1	3	12N	0B	9	HSI0B_SYDT[5]	HSI0B_RXD6/TXD6	FIFO1_DIN6/DOUT6	B8
BK3_IO2	3	13P	0B	10		HSI0B_RXD7/TXD7	FIFO1_DIN7/DOUT7	A8
BK3_IO3	3	13N	0B	11	-	HSI0B_RXD8/TXD8	FIFO1_DIN8/DOUT8	A7
GND	3	-	-	-	-	-	-	GND
BK3_IO4	3	14P	0B	12	HSI0B_SINP	HSI0B_RXD9/TXD9	FIFO1_DIN9/DOUT9	C7
BK3_IO5	3	14N	0B	13	HSI0B_SINN	HSI0B_RECCLK	-	D7
GND	3	-	-	-	-	-	-	GND
BK3_IO6	3	15P	0B	14	FIFO1_STRDb[6]	-	-	B6
BK3_IO7/CLK_OUT0	3	15N	0B	15	HSI0B_CDRRSTb	-	FIFO1_FIFORSTb	C6

ispGDX2-64 Logic Signal Connections (Continued)

Signal Name	sysIO Bank	LVDS Pair/Polarity	GDX Block	MRB	SERDES Mode I/O Pin[1]	SERDES Mode I/O Cell[2]	FIFO Mode I/O Cell/Pin[3]	100 fpBGA
SEL0	-	-	-	-	-	-	-	D6
SEL1	-	-	-	-	-	-	-	D5
BK4_IO0/CLK_OUT2	4	16N	1A[7]	0	HSI1A_CDRRSTb	-	FIFO2_FIFORSTb	C5
BK4_IO1	4	16P	1A[7]	1	FIFO2_STRDb[6]	-	-	B5
GND	4	-	-	-	-	-	-	GND
BK4_IO2	4	17N	1A[7]	2	HSI1A_SINN	HSI1A_RECCLK	-	D4
BK4_IO3	4	17P	1A[7]	3	HSI1A_SINP	HSI1A_RXD9/TXD9	FIFO2_DIN9/DOUT9	C4
GND	4				-	-	-	GND
BK4_IO4	4	18N	1A[7]	4	-	HSI1A_RXD8/TXD8	FIFO2_DIN8/DOUT8	A6
BK4_IO5	4	18P	1A[7]	5	CAL	HSI1A_RXD7/TXD7	FIFO2_DIN7/DOUT7	A5
BK4_IO6	4	19N	1A[7]	6	HSI1A_SYDT[5]	HSI1A_RXD6/TXD6	FIFO2_DIN6/DOUT6	A4
BK4_IO7	4	19P	1A[7]	7	-	HSI1A_RXD5/TXD5	FIFO2_DIN5/DOUT5	A3
TMS	-		-	-	-	-	-	B3
TDI	-	-	-	-	-	-	-	A2
GND	-	-	-	-	-	-	-	GND
TDO	-	-	-	-	-	-	-	B1
TOE	-	-	-	-	-	-	-	B2
BK5_IO0	5	20P	1A[7]	8	Note 4	HSI1A_RXD4/TXD4	FIFO2_DIN4/DOUT4	C1
BK5_IO1	5	20N	1A[7]	9	HSI1_CSLOCK	HSI1A_RXD3/TXD3	FIFO2_DIN3/DOUT3	C2
BK5_IO2	5	21P	1A[7]	10	-	HSI1A_RXD2/TXD2	FIFO2_DIN2/DOUT2	C3
BK5_IO3/Vref(4,5)	5	21N	1A[7]	11	-	HSI1A_RXD1/TXD1	FIFO2_DIN1/DOUT1	D1
GND	5	-	-	-	-	-	-	GND
BK5_IO4	5	22P	1A[7]	12	HSI1A_SOUTP	HSI1A_RXD0/TXD0	FIFO2_DIN0/DOUT0	D3
BK5_IO5	5	22N	1A[7]	13	HSI1A_SOUTN	HSI1A_SYDT[5]	-	D2
GND	5	-	-		-	-	-	GND
BK5_IO6	5	23P	1A[7]	14	SS_CLKIN1P	-	FIFO2_EMPTY	E2
BK5_IO7	5	23N	1A[7]	15	SS_CLKIN1N	-	FIFO2_FULL	E3
GCLK/CE0	-	CLK0P	-	-	-	-	-	E4
GCLK/CE1	-	CLK0N	-	-	-	-	-	F4
BK6_IO0	6	24N	1B	0	SS_CLKOUT1N	-	FIFO3_EMPTY	F3
BK6_IO1	6	24P	1B	1	SS_CLKOUT1P	HSI1B_SYDT[5]	-	F2
GND	6	-	-	-	-	-	-	GND
BK6_IO2	6	25N	1B	2	HSI1B_SOUTN	HSI1B_RXD9/TXD9	FIFO3_DIN9/DOUT9	G3
BK6_IO3	6	25P	1B	3	HSI1B_SOUTP	HSI1B_RXD8/TXD8	FIFO3_DIN8/DOUT8	G2
GND	6	-	-	-	-	-	-	GND
BK6_IO4/Vref(Bank6,7)	6	26N	1B	4	FIFO3_STRDb[6]	HSI1B_RXD7/TXD7	FIFO3_DIN7/DOUT7	G1
BK6_IO5	6	26P	1B	5	-	HSI1B_RXD6/TXD6	FIFO3_DIN6/DOUT6	H1
BK6_IO6	6	27N	1B	6	-	HSI1B_RXD5/TXD5	FIFO3_DIN5/DOUT5	H2
BK6_IO7/PLL_FBK2	6	27P	1B	7	HSI1B_SYDT[5]	HSI1B_RXD4/TXD4	FIFO3_DIN4/DOUT4	J1
BK7_IO0	7	28P	1B	8	Note 4	HSI1B_RXD3/TXD3	FIFO3_DIN3/DOUT3	J3
BK7_IO1	7	28N	1B	9	-	HSI1B_RXD2/TXD2	FIFO3_DIN2/DOUT2	K2
BK7_IO2	7	29P	1B	10	-	HSI1B_RXD1/TXD1	FIFO3_DIN1/DOUT1	J4
BK7_IO3/PLL_RST2	7	29N	1B	11	-	HSI1B_RXD0/TXD0	FIFO3_DIN0/DOUT0	K3
GND	7	-	-	-	-	-	-	GND
BK7_IO4	7	30P	1B	12	HSI1B_SINP	-	-	G4
BK7_IO5	7	30N	1B	13	HSI1B_SINN	HSI1B_RECCLK	-	H4

ispGDX2-64 Logic Signal Connections (Continued)

Signal Name	sysIO Bank	LVDS Pair/Polarity	GDX Block	MRB	SERDES Mode I/O Pin[1]	SERDES Mode I/O Cell[2]	FIFO Mode I/O Cell/Pin[3]	100 fpBGA
GND	7	-	-	-	-	-	-	GND
BK7_IO6	7	31P	1B	14	HSI1B_CDRRSTb	-	FIFO3_FIFORSTb	K5
BK7_IO7/PLL_LOCK2	7	31N	1B	15	-	-	FIFO3_FULL	J5
GOE1	7	-	-	-	-	-	-	H5

1. The signals in this column route to/from the assigned pins of the associated I/O cell.
2. The signals in this column use the I/O cell. If a receiver signal is present in the I/O cell, the associated pin is available for output only. When transmit data (TXD) is present in the cell, the associated pin is available for input only.
3. The DOUT outputs are routed to GRP through the input register of the cell and the DIN inputs are routed direct from the associated pins in FIFO only mode. In SERDES with FIFO mode, the FULL and EMPTY flags are routed to the associated pins through the output MUX and the pins.
4. If the Source Synchronous Receiver is used in the HSI Block, this pin is unavailable for another use and must be left unconnected.
5. The SYDT signal has two routing options. If direct output through the dedicated pin is used, the I/O cell (the whole HSI Block) is not available for transmitter. The SYDT in the I/O Cell column is routed to the GRP through the input register of the cell and frees the I/O cell for transmitter.
6. FIFO_STRDb flag output is used in SERDES with FIFO Mode only.
7. sysHSI Source Synchronous Receive Mode is not available for channel 1A.

ispGDX2-128 Logic Signal Connections

Signal Name	sysIO Bank	LVDS Pair/Polarity	GDX Block	MRB	SERDES Mode I/O Pin[1]	SERDES Mode I/O Cell[2]	FIFO Mode I/O Cell/Pin[3]	208 fpBGA
TOE	-		-	-	-	-	-	P8
BK0_IO0	0	0N	0A	0	-	-	FIFO0A_FULL	P9
BK0_IO1	0	0P	0A	1	-	-	-	T10
BK0_IO2 / PLL_LOCK2 / PLL_RST2	0	1N	0A	2	-	-	-	R10
BK0_IO3	0	1P	0A	3	-	HSI0A_SYDT[5]	FIFO0A_ EMPTY	T11
GND	0		-	-	-	-	-	GND
BK0_IO4	0	2N	0A	4	HSI0A_SINN	HSI0A_RXD0/TXD0	FIFO0A_DIN0/DOUT0	P10
BK0_IO5	0	2P	0A	5	HSI0A_SINP	HSI0A_RXD1/TXD1	FIFO0A_DIN1/DOUT1	N10
BK0_IO6	0	3N		6	-	HSI0A_RXD2/TXD2	FIFO0A_DIN2/DOUT2	R11
BK0_IO7	0	3P	0A	7	-	HSI0A_RXD3/TXD3	FIFO0A_DIN3/DOUT3	T13
BK0_IO8	0	4N	0A	8	Note 4	HSI0A_RXD4/TXD4	FIFO0A_DIN4/DOUT4	P11
BK0_IO9 / PLL_FB2	0	4P	0A	9	-	HSI0A_RXD5/TXD5	FIFO0A_DIN5/DOUT5	R12
BK0_IO10	0	5N	0A	10	HSI0A_SOUTN	HSI0A_RXD6/TXD6	FIFO0A_DIN6/DOUT6	P12
BK0_IO11	0	5P	0A	11	HSI0A_SOUTP	HSI0A_RXD7/TXD7	FIFO0A_DIN7/DOUT7	N12
GND	0		-	-	-	-	-	GND
BK0_IO12	0	6N	0A	12	-	HSI0A_RXD8/TXD8	FIFO0A_DIN8/DOUT8	T14
BK0_IO13	0	6P	0A	13	HSI0A_SYDT[5]	HSI0A_RXD9/TXD9	FIFO0A_DIN9/DOUT9	R13
BK0_IO14	0	7N	0A	14	HSI0A_CDRRSTb	HSI0A_RECCLK	FIFO0A_FIFORSTb	T15
BK0_IO15 / VREF0	0	7P	0A	15	FIFO0A_STRDb[6]	-	-	P13
GOE3	-		-	-	-	-	-	T9
TDO	-		-	-	-	-	-	R16
GND	1		-	-	-	-	-	GND
BK1_IO0 / VREF1	1	8P	0B	0	-	HSI0B_SYDT[5]	FIFO0B_FULL	N14
BK1_IO1	1	8N	0B	1	-	HSI0B_RXD0/TXD0	FIFO0B_DIN0/DOUT0	P15
BK1_IO2	1	9P	0B	2	Note 4	HSI0B_RXD1/TXD1	FIFO0B_DIN1/DOUT1	N15
BK1_IO3	1	9N	0B	3	-	HSI0B_RXD2/TXD2	FIFO0B_DIN2/DOUT2	L14
BK1_IO4	1	10P	0B	4	HSI0B_SOUTP	HSI0B_RXD3/TXD3	FIFO0B_DIN3/DOUT3	M14
BK1_IO5	1	10N	0B	5	HSI0B_SOUTN	HSI0B_RXD4/TXD4	FIFO0B_DIN4/DOUT4	M13
BK1_IO6	1	11P	0B	6	HSI0_CSLOCK	HSI0B_RXD5/TXD5	FIFO0B_DIN5/DOUT5	M15
BK1_IO7	1	11N	0B	7	HSI0B_SYDT[5]	HSI0B_RXD6/TXD6	FIFO0B_DIN6/DOUT6	L15
BK1_IO8	1	12P	0B	8	-	HSI0B_RXD7/TXD7	FIFO0B_DIN7/DOUT7	P16
BK1_IO9	1	12N	0B	9	-	HSI0B_RXD8/TXD8	FIFO0B_DIN8/DOUT8	N16
BK1_IO10	1	13P	0B	10	HSI0B_SINP	HSI0B_RXD9/TXD9	FIFO0B_DIN9/DOUT9	K14
BK1_IO11	1	13N	0B	11	HSI0B_SINN	HSI0B_RECCLK	-	K13
GND	1		-	-	-	-	-	GND
BK1_IO12	1	14P	0B	12	FIFO0B_STRDb[6]	-	-	K15
BK1_IO13	1	14N	0B	13	HSI0B_CDRRSTb	-	FIFO0B_FIFORSTb	L16
BK1_IO14	1	15P	0B	14	SS_CLKIN1P	-	-	J14
BK1_IO15 / CLK_OUT2	1	15N	0B	15	SS_CLKIN1N	-	FIFO0B_ EMPTY	J13
GCLK/CE2	-		-	-	-	-	-	N8
SEL2	-		-	-	-	-	-	K16
SEL3	-		-	-	-	-	-	G16
GCLK/CE3	-		-	-	-	-	-	N9
BK2_IO0	2	16N	1A[7]	0	SS_CLKOUT1N	-	FIFO1A_FULL	H13
BK2_IO1	2	16P	1A[7]	1	SS_CLKOUT1P	-	-	H14
BK2_IO2	2	17N	1A[7]	2	-	HSI1A_SYDT[5]	-	G15

ispGDX2-128 Logic Signal Connections (Continued)

Signal Name	sysIO Bank	LVDS Pair/Polarity	GDX Block	MRB	SERDES Mode I/O Pin[1]	SERDES Mode I/O Cell[2]	FIFO Mode I/O Cell/Pin[3]	208 fpBGA
BK2_IO3	2	17P	1A[7]	3	-	HSI1A_RXD0/TXD0	FIFO1A_DIN0/DOUT0	F16
GND	2		-	-	-	-	-	GND
BK2_IO4	2	18N	1A[7]	4	HSI1A_SINN	HSI1A_RXD1/TXD1	FIFO1A_DIN1/DOUT1	G13
BK2_IO5	2	18P	1A[7]	5	HSI1A_SINP	HSI1A_RXD2/TXD2	FIFO1A_DIN2/DOUT2	G14
BK2_IO6	2	19N	1A[7]	6	HSI1_CSLOCK	HSI1A_RXD3/TXD3	FIFO1A_DIN3/DOUT3	F14
BK2_IO7	2	19P	1A[7]	7	Note 4	HSI1A_RXD4/TXD4	FIFO1A_DIN4/DOUT4	F15
BK2_IO8	2	20N	1A[7]	8	CAL	HSI1A_RXD5/TXD5	FIFO1A_DIN5/DOUT5	D16
BK2_IO9	2	20P	1A[7]	9	-	HSI1A_RXD6/TXD6	FIFO1A_DIN6/DOUT6	E15
BK2_IO10	2	21N	1A[7]	10	HSI1A_SOUTN	HSI1A_RXD7/TXD7	FIFO1A_DIN7/DOUT7	E13
BK2_IO11	2	21P	1A[7]	11	HSI1A_SOUTP	HSI1A_RXD8/TXD8	FIFO1A_DIN8/DOUT8	E14
GND	2		-	-	-	-	-	GND
BK2_IO12	2	22N	1A[7]	12	HSI1A_SYDT[5]	HSI1A_RXD9/TXD9	FIFO1A_DIN9/DOUT9	C16
BK2_IO13	2	22P	1A[7]	13	HSI1A_CDRRSTb	HSI1A_RECCLK	FIFO1A_FIFORSTb	D15
BK2_IO14	2	23N	1A[7]	14	FIFO1A_STRDb[6]	-	-	C15
BK2_IO15 / VREF2	2	23P	1A[7]	15	-	-	FIFO1A_EMPTY	D14
TCK	-		-	-	-	-	-	R14
GOE2	-		-	-	-	-	-	A9
BK3_IO0 / VREF3	3	24P	1B	0	-	HSI1B_RXD0/TXD0	FIFO1B_DIN0/DOUT0	C13
BK3_IO1	3	24N	1B	1	Note 4	HSI1B_RXD1/TXD1	FIFO1B_DIN1/DOUT1	B14
BK3_IO2	3	25P	1B	2	-	HSI1B_RXD2/TXD2	FIFO1B_DIN2/DOUT2	A15
BK3_IO3	3	25N	1B	3	-	HSI1B_RXD3/TXD3	FIFO1B_DIN3/DOUT3	B13
GND	3			-	-	-	-	GND
BK3_IO4	3	26P	1B	4	HSI1B_SOUTP	HSI1B_RXD4/TXD4	FIFO1B_DIN4/DOUT4	D12
BK3_IO5	3	26N	1B	5	HSI1B_SOUTN	HSI1B_RXD5/TXD5	FIFO1B_DIN5/DOUT5	C12
BK3_IO6	3	27P	1B	6	-	HSI1B_RXD6/TXD6	FIFO1B_DIN6/DOUT6	A14
BK3_IO7	3	27N	1B	7	-	HSI1B_RXD7/TXD7	FIFO1B_DIN7/DOUT7 / FIFO1B_STRDb	A13
BK3_IO8	3	28P	1B	8	-	HSI1B_RXD8/TXD8	FIFO1B_DIN8/DOUT8	B12
BK3_IO9	3	28N	1B	9	HSI1B_SYDT[5]	HSI1B_RXD9/TXD9	FIFO1B_DIN9/DOUT9	C11
BK3_IO10	3	29P	1B	10	HSI1B_SINP	HSI1B_RECCLK	-	D10
BK3_IO11	3	29N	1B	11	HSI1B_SINN	-	-	C10
GND	3		-	-	-	-	-	GND
BK3_IO12	3	30P	1B	12	-	HSI1B_SYDT[5]	FIFO1B_FULL	B11
BK3_IO13	3	30N	1B	13	HSI1B_CDRRSTb	-	FIFO1B_FIFORSTb	B10
BK3_IO14	3	31P	1B	14	-	-	-	A10
BK3_IO15	3	31N	1B	15	-	-	FIFO1B_ EMPTY	C9
RESET	-		-	-	-	-	-	A7
BK4_IO0	4	32N	2A	0	-	-	FIFO2A_EMPTY	C8
BK4_IO1 / PLL_LOCK0 / PLL_RST0	4	32P	2A	1	-	-	-	B7
BK4_IO2	4	33N	2A	2	HSI2A_CDRRSTb	-	FIFO2A_FIFORSTb	A6
BK4_IO3	4	33P	2A	3	-	HSI2A_SYDT[5]	FIFO2A_FULL	B6
GND	4				-	-	-	GND
BK4_IO4	4	34N	2A	4	HSI2A_SINN	-	-	C7
BK4_IO5	4	34P	2A	5	HSI2A_SINP	HSI2A_RECCLK	-	D7
BK4_IO6	4	35N	2A	6	HSI2A_SYDT[5]	HSI2A_RXD9/TXD9	FIFO2A_DIN9/DOUT9	C6
BK4_IO7	4	35P	2A	7	-	HSI2A_RXD8/TXD8	FIFO2A_DIN8/DOUT8	B5

ispGDX2-128 Logic Signal Connections (Continued)

Signal Name	sysIO Bank	LVDS Pair/Polarity	GDX Block	MRB	SERDES Mode I/O Pin[1]	SERDES Mode I/O Cell[2]	FIFO Mode I/O Cell/Pin[3]	208 fpBGA
BK4_IO8	4	36N	2A	8	FIFO2A_STRDb[6]	HSI2A_RXD7/TXD7	FIFO2A_DIN7/DOUT7	A4
BK4_IO9 / PLL_FB0	4	36P	2A	9	-	HSI2A_RXD6/TXD6	FIFO2A_DIN6/DOUT6	A3
BK4_IO10	4	37N	2A	10	HSI2A_SOUTN	HSI2A_RXD5/TXD5	FIFO2A_DIN5/DOUT5	C5
BK4_IO11	4	37P	2A	11	HSI2A_SOUTP	HSI2A_RXD4/TXD4	FIFO2A_DIN4/DOUT4	D5
GND	4			-	-	-	-	GND
BK4_IO12	4	38N	2A	12	-	HSI2A_RXD3/TXD3	FIFO2A_DIN3/DOUT3	B4
BK4_IO13	4	38P	2A	13	-	HSI2A_RXD2/TXD2	FIFO2A_DIN2/DOUT2	A2
BK4_IO14	4	39N	2A	14	Note 4	HSI2A_RXD1/TXD1	FIFO2A_DIN1/DOUT1	B3
BK4_IO15 / VREF4	4	39P	2A	15	-	HSI2A_RXD0/TXD0	FIFO2A_DIN0/DOUT0	C4
GOE1	-			-	-	-	-	A8
TMS	-		-	-	-	-	-	R1
GND	5		-	-	-	-	-	GND
BK5_IO0 / VREF5	5	40P	2B	0	-	-	FIFO2B_EMPTY	D3
BK5_IO1	5	40N	2B	1	FIFO2B_STRDb[6]	-	-	C2
BK5_IO2	5	41P	2B	2	HSI2B_CDRRSTb	HSI2B_RECCLK	FIFO2B_FIFORSTb	D2
BK5_IO3	5	41N	2B	3	HSI2B_SYDT[5]	HSI2B_RXD9/TXD9	FIFO2B_DIN9/DOUT9	B1
BK5_IO4	5	42P	2B	4	HSI2B_SOUTP	HSI2B_RXD8/TXD8	FIFO2B_DIN8/DOUT8	E3
BK5_IO5	5	42N	2B	5	HSI2B_SOUTN	HSI2B_RXD7/TXD7	FIFO2B_DIN7/DOUT7	E4
BK5_IO6	5	43P	2B	6	-	HSI2B_RXD6/TXD6	FIFO2B_DIN6/DOUT6	F3
BK5_IO7	5	43N	2B	7	-	HSI2B_RXD5/TXD5	FIFO2B_DIN5/DOUT5	E2
BK5_IO8	5	44P	2B	8	Note 4	HSI2B_RXD4/TXD4	FIFO2B_DIN4/DOUT4	F2
BK5_IO9	5	44N	2B	9	HSI2_CSLOCK	HSI2B_RXD3/TXD3	FIFO2B_DIN3/DOUT3	C1
BK5_IO10	5	45P	2B	10	HSI2B_SINP	HSI2B_RXD2/TXD2	FIFO2B_DIN2/DOUT2	G3
BK5_IO11	5	45N	2B	11	HSI2B_SINN	HSI2B_RXD1/TXD1	FIFO2B_DIN1/DOUT1	G4
GND	5		-	-	-	-	-	GND
BK5_IO12	5	46P	2B	12	-	HSI2B_RXD0/TXD0	FIFO2B_DIN0/DOUT0	D1
BK5_IO13	5	46N	2B	13	-	HSI2B_SYDT[5]	-	G2
BK5_IO14	5	47P	2B	14	SS_CLKIN0P	-	-	H4
BK5_IO15 / CLK_OUT0	5	47N	2B	15	SS_CLKIN0N	-	FIFO2B_FULL	H3
GCLK/CE0	-	CLK0P	-	-	-	-	-	D9
SEL0	-		-	-	-	-	-	F1
SEL1	-		-	-	-	-	-	G1
GCLK/CE1	-	CLK0N	-	-	-	-	-	D8
BK6_IO0	6	48N	3A	0	SS_CLKOUT0N	-	FIFO3A_EMPTY	J4
BK6_IO1	6	48P	3A	1	SS_CLKOUT0P	-	-	J3
BK6_IO2	6	49N	3A	2	HSI3A_CDRRSTb	-	FIFO3A_FIFORSTb	K1
BK6_IO3	6	49P	3A	3	FIFO3A_STRDb[6]	-	-	K2
GND	6		-	-	-	-	-	GND
BK6_IO4	6	50N	3A	4	HSI3A_SINN	HSI3A_RECCLK	-	K4
BK6_IO5	6	50P	3A	5	HSI3A_SINP	HSI3A_RXD9/TXD9	FIFO3A_DIN9/DOUT9	K3
BK6_IO6	6	51N	3A	6	-	HSI3A_RXD8/TXD8	FIFO3A_DIN8/DOUT8	L1
BK6_IO7	6	51P	3A	7	-	HSI3A_RXD7/TXD7	FIFO3A_DIN7/DOUT7	L2
BK6_IO8	6	52N	3A	8	HSI3A_SYDT[5]	HSI3A_RXD6/TXD6	FIFO3A_DIN6/DOUT6	N1
BK6_IO9	6	52P	3A	9	HSI3_CSLOCK	HSI3A_RXD5/TXD5	FIFO3A_DIN5/DOUT5	M2
BK6_IO10	6	53N	3A	10	HSI3A_SOUTN	HSI3A_RXD4/TXD4	FIFO3A_DIN4/DOUT4	M4
BK6_IO11	6	53P	3A	11	HSI3A_SOUTP	HSI3A_RXD3/TXD3	FIFO3A_DIN3/DOUT3	M3

ispGDX2-128 Logic Signal Connections (Continued)

Signal Name	sysIO Bank	LVDS Pair/Polarity	GDX Block	MRB	SERDES Mode I/O Pin[1]	SERDES Mode I/O Cell[2]	FIFO Mode I/O Cell/Pin[3]	208 fpBGA
GND	6		-	-	-	-	-	GND
BK6_IO12	6	54N	3A	12	-	HSI3A_RXD2/TXD2	FIFO3A_DIN2/DOUT2	L3
BK6_IO13	6	54P	3A	13	Note 4	HSI3A_RXD1/TXD1	FIFO3A_DIN1/DOUT1	N2
BK6_IO14	6	55N	3A	14	-	HSI3A_RXD0/TXD0	FIFO3A_DIN0/DOUT0	P1
BK6_IO15 / VREF6	6	55P	3A	15	-	HSI3A_SYDT[5]	FIFO3A_ FULL	P2
TDI	-		-	-	-	-	-	N3
GOE0	-		-	-	-	-	-	T8
GND	7		-	-	-	-	-	GND
BK7_IO0 / VREF7	7	56P	3B	0	FIFO3B_STRDb[6]	-	-	T2
BK7_IO1	7	56N	3B	1	HSI3B_CDRRSTb	HSI3B_RECCLK	FIFO3B_FIFORSTb	R3
BK7_IO2	7	57P	3B	2	HSI3B_SYDT[5]	HSI3B_RXD9/TXD9	FIFO3B_DIN9/DOUT9	P4
BK7_IO3	7	57N	3B	3	-	HSI3B_RXD8/TXD8	FIFO3B_DIN8/DOUT8	T3
BK7_IO4	7	58P	3B	4	HSI3B_SOUTP	HSI3B_RXD7/TXD7	FIFO3B_DIN7/DOUT7	N5
BK7_IO5	7	58N	3B	5	HSI3B_SOUTN	HSI3B_RXD6/TXD6	FIFO3B_DIN6/DOUT6	P5
BK7_IO6	7	59P	3B	6	-	HSI3B_RXD5/TXD5	FIFO3B_DIN5/DOUT5	R4
BK7_IO7	7	59N	3B	7	Note 4	HSI3B_RXD4/TXD4	FIFO3B_DIN4/DOUT4	T4
BK7_IO8	7	60P	3B	8	-	HSI3B_RXD3/TXD3	FIFO3B_DIN3/DOUT3	R5
BK7_IO9	7	60N	3B	9	-	HSI3B_RXD2/TXD2	FIFO3B_DIN2/DOUT2	P6
BK7_IO10	7	61P	3B	10	HSI3B_SINP	HSI3B_RXD1/TXD1	FIFO3B_DIN1/DOUT1	N7
BK7_IO11	7	61N	3B	11	HSI3B_SINN	HSI3B_RXD0/TXD0	FIFO3B_DIN0/DOUT0	P7
GND	7		-	-	-	-	-	GND
BK7_IO12	7	62P	3B	12	-	HSI3B_SYDT[5]	FIFO3B_ EMPTY	R6
BK7_IO13	7	62N	3B	13	-	-	-	T6
BK7_IO14	7	63P	3B	14	-	-	-	R7
BK7_IO15	7	63N	3B	15	-	-	FIFO3B_FULL	T7

1. The signals in this column route to/from the assigned pins of the associated I/O cell.
2. The signals in this column use the I/O cell. If a receiver signal is present in the I/O cell, the associated pin is available for output only. When transmit data (TXD) is present in the cell, the associated pin is available for input only.
3. The DOUT outputs are routed to GRP through the input register of the cell and the DIN inputs are routed direct from the associated pins in FIFO only mode. In SERDES with FIFO mode, the FULL and EMPTY flags are routed to the associated pins through the output MUX and the pins.
4. If the Source Synchronous Receiver is used in the HSI Block, this pin is unavailable for another use and must be left unconnected.
5. The SYDT signal has two routing options. If direct output through the dedicated pin is used, the I/O cell (the whole HSI Block) is not available for transmitter. The SYDT in the I/O Cell column is routed to the GRP through the input register of the cell and frees the I/O cell for transmitter.
6. FIFO_STRDb flag output is used in SERDES with FIFO Mode only.
7. sysHSI Source Synchronous Receive Mode is not available for channel 1A.

ispGDX2-256 Logic Signal Connections

Signal Name	sysIO Bank	LVDS Pair/Polarity	GDX Block	MRB	SERDES Mode I/O Pin[1]	SERDES Mode I/O Cell[2]	FIFO Mode I/O Cell/Pin[3]	484 fpBGA
BK0_IO0	0	0N	0A	0	-	-	FIFO0A_FULL	AB13
BK0_IO1	0	0P	0A	1	-	-	-	AA13
BK0_IO2/ PLL_LOCK2	0	1N	0A	2	-	-	-	V13
BK0_IO3	0	1P	0A	3	-	-	FIFO0A_ EMPTY	V14
GND	0	-	-	-	-	SYDT_HSI0A[5]	-	GND
BK0_IO4	0	2N	0A	4	HSI0A_SINN	HSI0A_RXD0/TXD0	FIFO0A_DIN0/DOUT0	U12
BK0_IO5	0	2P	0A	5	HSI0A_SINP	HSI0A_RXD1/TXD1	FIFO0A_DIN1/DOUT1	U13
BK0_IO6	0	3N		6	-	HSI0A_RXD2/TXD2	FIFO0A_DIN2/DOUT2	W12
BK0_IO7	0	3P	0A	7	-	HSI0A_RXD3/TXD3	FIFO0A_DIN3/DOUT3	Y13
BK0_IO8	0	4N	0A	8	Note 4	HSI0A_RXD4/TXD4	FIFO0A_DIN4/DOUT4	W13
BK0_IO9/ PLL_FB2	0	4P	0A	9	-	HSI0A_RXD5/TXD5	FIFO0A_DIN5/DOUT5	Y14
BK0_IO10	0	5N	0A	10	HSI0A_SOUTN	HSI0A_RXD6/TXD6	FIFO0A_DIN6/DOUT6	T12
BK0_IO11	0	5P	0A	11	HSI0A_SOUTP	HSI0A_RXD7/TXD7	FIFO0A_DIN7/DOUT7	T13
GND	0	-	-	-	-	-	-	GND
BK0_IO12	0	6N	0A	12	-	HSI0A_RXD8/TXD8	FIFO0A_DIN8/DOUT8	AB14
BK0_IO13	0	6P	0A	13	HSI0A_SYDT[5]	HSI0A_RXD9/TXD9	FIFO0A_DIN9/DOUT9	AB15
BK0_IO14	0	7N	0A	14	HSI0A_CDRRSTb	HSI0A_RECCLK	FIFO0A_FIFORSTb	Y15
BK0_IO15	0	7P	0A	15	FIFO0A_STRDb[6]	-	-	W15
BK0_IO16	0	8N	1A	0	-	-	FIFO1A_FULL	AA15
BK0_IO17/ PLL_RST2	0	8P	1A	1	-	-	-	AA16
BK0_IO18	0	9N	1A	2	-	HSI1A_SYDT[5]	-	Y16
BK0_IO19	0	9P	1A	3	-	HSI1A_RXD0/TXD0	FIFO1A_DIN0/DOUT0	W16
GND	0	-	-	-	-	-	-	GND
BK0_IO20	0	10N	1A	4	HSI1A_SOUTN	HSI1A_RXD1/TXD1	FIFO1A_DIN1/DOUT1	U14
BK0_IO21/ VREF0	0	10P	1A	5	HSI1A_SOUTP	HSI1A_RXD2/TXD2	FIFO1A_DIN2/DOUT2	U15
BK0_IO22	0	11N	1A	6	-	HSI1A_RXD3/TXD3	FIFO1A_DIN3/DOUT3	AB16
BK0_IO23	0	11P	1A	7	Note 4	HSI1A_RXD4/TXD4	FIFO1A_DIN4/DOUT4	AB17
BK0_IO24	0	12N	1A	8	-	HSI1A_RXD5/TXD5	FIFO1A_DIN5/DOUT5	AA17
BK0_IO25	0	12P	1A	9	-	HSI1A_RXD6/TXD6	FIFO1A_DIN6/DOUT6	W17
BK0_IO26	0	13N	1A	10	HSI1A_SINN	HSI1A_RXD7/TXD7	FIFO1A_DIN7/DOUT7	T14
BK0_IO27	0	13P	1A	11	HSI1A_SINP	HSI1A_RXD8/TXD8	FIFO1A_DIN8/DOUT8	T15
BK0_IO28	0	14N	1A	12	HSI1A_SYDT[5]	HSI1A_RXD9/TXD9	FIFO1A_DIN9/DOUT9	AA18
BK0_IO29	0	14P	1A	13	HSI1A_CDRRSTb[5]	HSI1A_RECCLK	FIFO1A_FIFORSTb	AB18
BK0_IO30	0	15N	1A	14	FIFO1A_STRDb[6]	-	-	W18
BK0_IO31	0	15P	1A	15	-	-	FIFO1A_EMPTY	Y19
GND	0	-	-	-	-	-	-	GND
GOE3	-	-	-	-	-	-	-	AA19
TDO	-	-	-	-	-	-	-	AB19
GND	1	-	-	-	-	-	-	GND
BK1_IO0	1	16P	0B	0	-	-	FIFO0B_ FULL	W21
BK1_IO1	1	16N	0B	1	-	HSI0B_SYDT[5]	-	W20
BK1_IO2	1	17P	0B	2	-	HSI0B_RXD0/TXD0	FIFO0B_DIN0/DOUT0	V22
BK1_IO3	1	17N	0B	3	Note 4	HSI0B_RXD1/TXD1	FIFO0B_DIN1/DOUT1	W22
BK1_IO4	1	18P	0B	4	HSI0B_SINP	HSI0B_RXD2/TXD2	FIFO0B_DIN2/DOUT2	P16

ispGDX2-256 Logic Signal Connections (Continued)

Signal Name	sysIO Bank	LVDS Pair/Polarity	GDX Block	MRB	SERDES Mode I/O Pin[1]	SERDES Mode I/O Cell[2]	FIFO Mode I/O Cell/Pin[3]	484 fpBGA
BK1_IO5	1	18N	0B	5	HSI0B_SINN	HSI0B_RXD3/TXD3	FIFO0B_DIN3/DOUT3	P17
BK1_IO6	1	19P	0B	6	HSI0_CSLOCK	HSI0B_RXD4/TXD4	FIFO0B_DIN4/DOUT4	U18
BK1_IO7	1	19N	0B	7	-	HSI0B_RXD5/TXD5	FIFO0B_DIN5/DOUT5	V19
BK1_IO8	1	20P	0B	8	-	HSI0B_RXD6/TXD6	FIFO0B_DIN6/DOUT6	V20
BK1_IO9	1	20N	0B	9	HSI0B_SYDT[5]	HSI0B_RXD7/TXD7	FIFO0B_DIN7/DOUT7	V21
BK1_IO10/ VREF1	1	21P	0B	10	HSI0B_SOUTP	HSI0B_RXD8/TXD8	FIFO0B_DIN8/DOUT8	R16
BK1_IO11	1	21N	0B	11	HSI0B_SOUTN	HSI0B_RXD9/TXD9	FIFO0B_DIN9/DOUT9	R17
GND	1	-	-	-	-	-	-	GND
BK1_IO12	1	22P	0B	12	HSI0B_CDRRSTb	HSI0B_RECCLK	FIFO0B_FIFORSTb	U19
BK1_IO13	1	22N	0B	13	FIFO0B_STRDb[6]	-	-	T19
BK1_IO14	1	23P	0B	14	-	-	-	U21
BK1_IO15	1	23N	0B	15	-	-	FIFO0B_EMPTY	U22
BK1_IO16	1	24P	1B	0	-	HSI1B_SYDT[5]	FIFO1B_FULL	R19
BK1_IO17	1	24N	1B	1	-	HSI1B_RXD0/TXD0	FIFO1B_DIN0/DOUT0	T20
BK1_IO18	1	25P	1B	2	Note 4	HSI1B_RXD1/TXD1	FIFO1B_DIN1/DOUT1	T21
BK1_IO19	1	25N	1B	3	-	HSI1B_RXD2/TXD2	FIFO1B_DIN2/DOUT2	T22
GND	1	-	-	-	-	-	-	GND
BK1_IO20	1	26P	1B	4	HSI1B_SOUTP	HSI1B_RXD3/TXD3	FIFO1B_DIN3/DOUT3	N16
BK1_IO21	1	26N	1B	5	HSI1B_SOUTN	HSI1B_RXD4/TXD4	FIFO1B_DIN4/DOUT4	N17
BK1_IO22	1	27P	1B	6	HSI1_CSLOCK	HSI1B_RXD5/TXD5	FIFO1B_DIN5/DOUT5	R20
BK1_IO23	1	27N	1B	7	HSI1B_SYDT[5]	HSI1B_RXD6/TXD6	FIFO1B_DIN6/DOUT6	R21
BK1_IO24	1	28P	1B	8	-	HSI1B_RXD7/TXD7	FIFO1B_DIN7/DOUT7	N19
BK1_IO25	1	28N	1B	9	-	HSI1B_RXD8/TXD8	FIFO1B_DIN8/DOUT8	P20
BK1_IO26	1	29P	1B	10	HSI1B_SINP	HSI1B_RXD9/TXD9	FIFO1B_DIN9/DOUT9	P18
BK1_IO27	1	29N	1B	11	HSI1B_SINN	HSI1B_RECCLK	-	N18
GND	1		-	-	-	-	-	GND
BK1_IO28	1	30P	1B	12	FIFO1B_STRDb[6]	-	-	R22
BK1_IO29	1	30N	1B	13	HSI1B_CDRRSTb	-	FIFO1B_FIFORSTb	P22
BK1_IO30	1	31P	1B	14	SS_CLKIN1P	-	-	M18
BK1_IO31/ CLK_OUT2	1	31N	1B	15	SS_CLKIN1N	-	FIFO1B_EMPTY	M17
GCLK/CE2	-	CLK2P	-	-	-	-	-	N20
SEL2	-	-	-	-	-	-	-	N21
SEL3	-	-	-	-	-	-	-	K21
GCLK/CE3	-	CLK2N	-	-	-	-	-	K20
BK2_IO0/ CLK_OUT3	2	32N	3A[7]	0	SS_CLKOUT1N	-	FIFO3A_FULL	K17
BK2_IO1	2	32P	3A[7]	1	SS_CLKOUT1P	-	-	K18
BK2_IO2	2	33N	3A[7]	2	-	HSI3A_SYDT[5]	-	L17
BK2_IO3	2	33P	3A[7]	3	-	HSI3A_RXD0/TXD0	FIFO3A_DIN0/DOUT0	L18
GND	2		-	-	-	-	-	GND
BK2_IO4	2	34N	3A[7]	4	HSI3A_SINN	HSI3A_RXD1/TXD1	FIFO3A_DIN1/DOUT1	J17
BK2_IO5	2	34P	3A[7]	5	HSI3A_SINP	HSI3A_RXD2/TXD2	FIFO3A_DIN2/DOUT2	J18
BK2_IO6	2	35N	3A[7]	6	HSI3_CSLOCK	HSI3A_RXD3/TXD3	FIFO3A_DIN3/DOUT3	J22
BK2_IO7	2	35P	3A[7]	7	Note 4	HSI3A_RXD4/TXD4	FIFO3A_DIN4/DOUT4	J20
BK2_IO8	2	36N	3A[7]	8	CAL	HSI3A_RXD5/TXD5	FIFO3A_DIN5/DOUT5	H22
BK2_IO9	2	36P	3A[7]	9	-	HSI3A_RXD6/TXD6	FIFO3A_DIN6/DOUT6	H21

ispGDX2-256 Logic Signal Connections (Continued)

Signal Name	sysIO Bank	LVDS Pair/Polarity	GDX Block	MRB	SERDES Mode I/O Pin[1]	SERDES Mode I/O Cell[2]	FIFO Mode I/O Cell/Pin[3]	484 fpBGA
BK2_IO10	2	37N	3A[7]	10	HSI3A_SOUTN	HSI3A_RXD7/TXD7	FIFO3A_DIN7/DOUT7	K16
BK2_IO11	2	37P	3A[7]	11	HSI3A_SOUTP	HSI3A_RXD8/TXD8	FIFO3A_DIN8/DOUT8	J16
GND	2	-	-	-	-	-	-	GND
BK2_IO12	2	38N	3A[7]	12	HSI3A_SYDT[5]	HSI3A_RXD9/TXD9	FIFO3A_DIN9/DOUT9	J19
BK2_IO13	2	38P	3A[7]	13	HSI3A_CDRRSTb	HSI3A_RECCLK	FIFO3A_FIFORSTb	H20
BK2_IO14	2	39N	3A[7]	14	FIFO3A_STRDb[6]	-	-	G21
BK2_IO15	2	39P	3A[7]	15	-	-	FIFO3A_EMPTY	G20
BK2_IO16	2	40N	2A	0	-	-	FIFO2A_FULL	G22
BK2_IO17	2	40P	2A	1	-	HSI2A_SYDT[5]	-	F22
BK2_IO18	2	41N	2A	2	-	HSI2A_RXD0/TXD0	FIFO2A_DIN0/DOUT0	F20
BK2_IO19	2	41P	2A	3	Note 4	HSI2A_RXD1/TXD1	FIFO2A_DIN1/DOUT1	F21
GND	2	-	-	-	-	-	-	GND
BK2_IO20/ PLL_FB3	2	42N	2A	4	HSI2A_SOUTN	HSI2A_RXD2/TXD2	FIFO2A_DIN2/DOUT2	H18
BK2_IO21/ VREF2	2	42P	2A	5	HSI2A_SOUTP	HSI2A_RXD3/TXD3	FIFO2A_DIN3/DOUT3	G17
BK2_IO22	2	43N	2A	6	HSI2_CSLOCK	HSI2A_RXD4/TXD4	FIFO2A_DIN4/DOUT4	E21
BK2_IO23	2	43P	2A	7	-	HSI2A_RXD5/TXD5	FIFO2A_DIN5/DOUT5	F19
BK2_IO24	2	44N	2A	8	-	HSI2A_RXD6/TXD6	FIFO2A_DIN6/DOUT6	E22
BK2_IO25	2	44P	2A	9	HSI2A_SYDT[5]	HSI2A_RXD7/TXD7	FIFO2A_DIN7/DOUT7	D22
BK2_IO26	2	45N	2A	10	HSI2A_SINN	HSI2A_RXD8/TXD8	FIFO2A_DIN8/DOUT8	H17
BK2_IO27	2	45P	2A	11	HSI2A_SINP	HSI2A_RXD9/TXD9	FIFO2A_DIN9/DOUT9	H16
BK2_IO28	2	46N	2A	12	HSI2A_CDRRSTb	HSI2A_RECCLK	FIFO2A_FIFORSTb	E19
BK2_IO29	2	46P	2A	13	FIFO2A_STRDb[6]	-	-	F18
BK2_IO30	2	47N	2A	14	-	-	-	D20
BK2_IO31	2	47P	2A	15	-	-	FIFO2A_EMPTY	D21
GND	2	-	-	-	-	-	-	GND
TCK	-	-	-	-	-	-	-	B19
GOE2	-	-	-	-	-	-	-	C19
BK3_IO0	3	48P	3B	0	-	HSI3B_SYDT[5]	FIFO3B_FULL	E17
BK3_IO1	3	48N	3B	1	-	HSI3B_RXD0/TXD0	FIFO3B_DIN0/DOUT0	D18
BK3_IO2	3	49P	3B	2	Note 4	HSI3B_RXD1/TXD1	FIFO3B_DIN1/DOUT1	A19
BK3_IO3	3	49N	3B	3	-	HSI3B_RXD2/TXD2	FIFO3B_DIN2/DOUT2	A18
GND	3	-	-	-	-	-	-	GND
BK3_IO4	3	50P	3B	4	HSI3B_SINP	HSI3B_RXD3/TXD3	FIFO3B_DIN3/DOUT3	G15
BK3_IO5	3	50N	3B	5	HSI3B_SINN	HSI3B_RXD4/TXD4	FIFO3B_DIN4/DOUT4	G14
BK3_IO6	3	51P	3B	6	-	HSI3B_RXD5/TXD5	FIFO3B_DIN5/DOUT5	D17
BK3_IO7	3	51N	3B	7	HSI3B_SYDT[5]	HSI3B_RXD6/TXD6	FIFO3B_DIN6/DOUT6	D16
BK3_IO8	3	52P	3B	8	-	HSI3B_RXD7/TXD7	FIFO3B_DIN7/DOUT7	C18
BK3_IO9	3	52N	3B	9	-	HSI3B_RXD8/TXD8	FIFO3B_DIN8/DOUT8	B18
BK3_IO10/ VREF3	3	53P	3B	10	HSI3B_SOUTP	HSI3B_RXD9/TXD9	FIFO3B_DIN9/DOUT9	F15
BK3_IO11	3	53N	3B	11	HSI3B_SOUTN	HSI3B_RECCLK	-	F14
GND	3	-	-	-	-	-	-	GND
BK3_IO12	3	54P	3B	12	FIFO3B_STRDb[6]	-	-	B17
BK3_IO13	3	54N	3B	13	HSI3B_CDRRSTb	HSI3B_RECCLK	FIFO3B_FIFORSTb	A17
BK3_IO14/ PLL_RST3	3	55P	3B	14	-	-	-	A16

ispGDX2-256 Logic Signal Connections (Continued)

Signal Name	sysIO Bank	LVDS Pair/Polarity	GDX Block	MRB	SERDES Mode I/O Pin[1]	SERDES Mode I/O Cell[2]	FIFO Mode I/O Cell/Pin[3]	484 fpBGA
BK3_IO15	3	55N	3B	15	-	-	FIFO3B_EMPTY	C16
BK3_IO16	3	56P	2B	0	-	HSI2B_RXD0/TXD0	FIFO2B_DIN0/DOUT0	D15
BK3_IO17	3	56N	2B	1	Note 4	HSI2B_RXD1/TXD1	FIFO2B_DIN1/DOUT1	D14
BK3_IO18	3	57P	2B	2	-	HSI2B_RXD2/TXD2	FIFO2B_DIN2/DOUT2	B16
BK3_IO19	3	57N	2B	3	-	HSI2B_RXD3/TXD3	FIFO2B_DIN3/DOUT3	C15
GND	3	-	-	-	-	-	-	GND
BK3_IO20	3	58P	2B	4	HSI2B_SOUTP	HSI2B_RXD4/TXD4	FIFO2B_DIN4/DOUT4	G13
BK3_IO21	3	58N	2B	5	HSI2B_SOUTN	HSI2B_RXD5/TXD5	FIFO2B_DIN5/DOUT5	G12
BK3_IO22	3	59P	2B	6	-	HSI2B_RXD6/TXD6	FIFO2B_DIN6/DOUT6	B15
BK3_IO23	3	59N	2B	7	FIFO2B_STRDb[6]	HSI2B_RXD7/TXD7	FIFO2B_DIN7 /DOUT7	A15
BK3_IO24	3	60P	2B	8	-	HSI2B_RXD8/TXD8	FIFO2B_DIN8/DOUT8	C14
BK3_IO25	3	60N	2B	9	HSI2B_SYDT[5]	HSI2B_RXD9/TXD9	FIFO2B_DIN9/DOUT9	A14
BK3_IO26	3	61P	2B	10	HSI2B_SINP	HSI2B_RECCLK	-	F13
BK3_IO27	3	61N	2B	11	HSI2B_SINN	-	-	F12
GND	3	-	-	-	-	-	-	GND
BK3_IO28	3	62P	2B	12	-	HSI2B_SYDT[5]	FIFO2B_FULL	D13
BK3_IO29	3	62N	2B	13	HSI2B_CDRRSTb	-	FIFO2B_FIFORSTb	C13
BK3_IO30/ PLL_LOCK3	3	63P	2B	14	-	-	-	B13
BK3_IO31	3	63N	2B	15	-	-	FIFO2B_ EMPTY	A13
RESETb	-		-	-	-	-	-	D12
BK4_IO0	4	64N	4A	0	-	-	FIFO4A_EMPTY	A10
BK4_IO1/ PLL_LOCK0	4	64P	4A	1	-	-	-	B10
BK4_IO2	4	65N	4A	2	HSI4A_CDRRSTb	-	FIFO4A_FIFORSTb	E11
BK4_IO3	4	65P	4A	3	-	HSI4A_SYDT[5]	FIFO4A_FULL	E10
GND	4				-	-	-	GND
BK4_IO4	4	66N	4A	4	HSI4A_SINN	-	-	F11
BK4_IO5	4	66P	4A	5	HSI4A_SINP	HSI4A_RECCLK	-	F10
BK4_IO6	4	67N	4A	6	HSI4A_SYDT[5]	HSI4A_RXD9/TXD9	FIFO4A_DIN9/DOUT9	C10
BK4_IO7	4	67P	4A	7	-	HSI4A_RXD8/TXD8	FIFO4A_DIN8/DOUT8	C9
BK4_IO8	4	68N	4A	8	FIFO4A_STRDb[6]	HSI4A_RXD7/TXD7	FIFO4A_DIN7 /DOUT7	D10
BK4_IO9/ PLL_FB0	4	68P	4A	9	-	HSI4A_RXD6/TXD6	FIFO4A_DIN6/DOUT6	D9
BK4_IO10	4	69N	4A	10	HSI4A_SOUTN	HSI4A_RXD5/TXD5	FIFO4A_DIN5/DOUT5	G11
BK4_IO11	4	69P	4A	11	HSI4A_SOUTP	HSI4A_RXD4/TXD4	FIFO4A_DIN4/DOUT4	G10
GND	4			-	-	-	-	GND
BK4_IO12	4	70N	4A	12	-	HSI4A_RXD3/TXD3	FIFO4A_DIN3/DOUT3	A9
BK4_IO13	4	70P	4A	13	-	HSI4A_RXD2/TXD2	FIFO4A_DIN2/DOUT2	C8
BK4_IO14	4	71N	4A	14	Note 4	HSI4A_RXD1/TXD1	FIFO4A_DIN1/DOUT1	B8
BK4_IO15	4	71P	4A	15	-	HSI4A_RXD0/TXD0	FIFO4A_DIN0/DOUT0	A8
BK4_IO16	4	72N	5A	0	-	-	FIFO5A_EMPTY	B7
BK4_IO17/ PLL_RST0	4	72P	5A	1	-	-	-	C7
BK4_IO18	4	73N	5A	2	HSI5A_CDRRSTb	-	FIFO5A_FIFORSTb	A7
BK4_IO19	4	73P	5A	3	FIFO5A_STRDb[6]	-	-	B6
GND	4	-	-	-	-	-	-	GND
BK4_IO20	4	74N	5A	4	HSI5A_SOUTN	HSI5A_RECCLK	-	F9

ispGDX2-256 Logic Signal Connections (Continued)

Signal Name	sysIO Bank	LVDS Pair/Polarity	GDX Block	MRB	SERDES Mode I/O Pin[1]	SERDES Mode I/O Cell[2]	FIFO Mode I/O Cell/Pin[3]	484 fpBGA
BK4_IO21/ VREF4	4	74P	5A	5	HSI5A_SOUTP	HSI5A_RXD9/TXD9	FIFO5A_DIN9/DOUT9	F8
BK4_IO22	4	75N	5A	6	-	HSI5A_RXD8/TXD8	FIFO5A_DIN8/DOUT8	D7
BK4_IO23	4	75P	5A	7	-	HSI5A_RXD7/TXD7	FIFO5A_DIN7/DOUT7	D6
BK4_IO24	4	76N	5A	8	HSI5A_SYDT[5]	HSI5A_RXD6/TXD6	FIFO5A_DIN6/DOUT6	A6
BK4_IO25	4	76P	5A	9	-	HSI5A_RXD5/TXD5	FIFO5A_DIN5/DOUT5	A5
BK4_IO26	4	77N	5A	10	HSI5A_SINN	HSI5A_RXD4/TXD4	FIFO5A_DIN4/DOUT4	G9
BK4_IO27	4	77P	5A	11	HSI5A_SINP	HSI5A_RXD3/TXD3	FIFO5A_DIN3/DOUT3	G8
BK4_IO28	4	78N	5A	12	-	HSI5A_RXD2/TXD2	FIFO5A_DIN2/DOUT2	C5
BK4_IO29	4	78P	5A	13	Note 4	HSI5A_RXD1/TXD1	FIFO5A_DIN1/DOUT1	B5
BK4_IO30	4	79N	5A	14	-	HSI5A_RXD0/TXD0	FIFO5A_DIN0/DOUT0	D5
BK4_IO31	4	79P	5A	15	-	HSI5A_SYDT[5]	FIFO5A_FULL	C4
GND	4		-	-	-	-	-	GND
GOE1	-			-	-	-	-	B4
TMS	-		-	-	-	-	-	A4
GND	5		-	-	-	-	-	GND
BK5_IO0	5	80P	4B	0	-	-	FIFO4B_EMPTY	D2
BK5_IO1	5	80N	4B	1	-	-	-	D3
BK5_IO2	5	81P	4B	2	FIFO4B_STRDb[6]	-	-	F5
BK5_IO3	5	81N	4B	3	HSI4B_CDRRSTb	HSI4B_RECCLK	FIFO4B_FIFORSTb	E4
BK5_IO4	5	82P	4B	4	HSI4B_SINP	HSI4B_RXD9/TXD9	FIFO4B_DIN9/DOUT9	J7
BK5_IO5	5	82N	4B	5	HSI4B_SINN	HSI4B_RXD8/TXD8	FIFO4B_DIN8/DOUT8	J6
BK5_IO6	5	83P	4B	6	HSI4B_SYDT[5]	HSI4B_RXD7/TXD7	FIFO4B_DIN7/DOUT7	D1
BK5_IO7	5	83N	4B	7	-	HSI4B_RXD6/TXD6	FIFO4B_DIN6/DOUT6	E1
BK5_IO8	5	84P	4B	8	-	HSI4B_RXD5/TXD5	FIFO4B_DIN5/DOUT5	F4
BK5_IO9	5	84N	4B	9	HSI4_CSLOCK	HSI4_RXD4/TXD4	FIFO4B_DIN4/DOUT4	E3
BK5_IO10/ VREF5	5	85P	4B	10	HSI4B_SOUTP	HSI4B_RXD3/TXD3	FIFO4B_DIN3/DOUT3	H7
BK5_IO11	5	85N	4B	11	HSI4B_SOUTN	HSI4B_RXD2/TXD2	FIFO4B_DIN2/DOUT2	H6
GND	5	-	-	-	-	-	-	GND
BK5_IO12	5	86P	4B	12	Note 4	HSI4B_RXD1/TXD1	FIFO4B_DIN1/DOUT1	E2
BK5_IO13	5	86N	4B	13	-	HSI4B_RXD0/TXD0	FIFO4B_DIN0/DOUT0	F2
BK5_IO14	5	87P	4B	14	-	HSI4B_SYDT[5]	-	G4
BK5_IO15	5	87N	4B	15	-	-	FIFO4B_FULL	H5
BK5_IO16	5	88P	5B	0	-	-	FIFO5B_EMPTY	F1
BK5_IO17	5	88N	5B	1	FIFO5B_STRDb[6]	-	-	G1
BK5_IO18	5	89P	5B	2	HSI5B_CDRRSTb	HSI5B_RECCLK	FIFO5B_FIFORSTb	G3
BK5_IO19	5	89N	5B	3	HSI5B_SYDT[5]	HSI5B_RXD9/TXD9	FIFO5B_DIN9/DOUT9	G2
GND	5	-	-	-	-	-	-	GND
BK5_IO20	5	90P	5B	4	HSI5B_SOUTP	HSI5B_RXD8/TXD8	FIFO5B_DIN8/DOUT8	K7
BK5_IO21	5	90N	5B	5	HSI5B_SOUTN	HSI5B_RXD7/TXD7	FIFO5B_DIN7/DOUT7	K6
BK5_IO22	5	91P	5B	6	-	HSI5B_RXD6/TXD6	FIFO5B_DIN6/DOUT6	H4
BK5_IO23	5	91N	5B	7	-	HSI5B_RXD5/TXD5	FIFO5B_DIN5/DOUT5	H3
BK5_IO24	5	92P	5B	8	Note 4	HSI5B_RXD4/TXD4	FIFO5B_DIN4/DOUT4	H1
BK5_IO25	5	92N	5B	9	HSI5_CSLOCK	HSI5B_RXD3/TXD3	FIFO5B_DIN3/DOUT3	H2
BK5_IO26	5	93P	5B	10	HSI5B_SINP	HSI5B_RXD2/TXD2	FIFO5B_DIN2/DOUT2	J5
BK5_IO27	5	93N	5B	11	HSI5B_SINN	HSI5B_RXD1/TXD1	FIFO5B_DIN1/DOUT1	K5

ispGDX2-256 Logic Signal Connections (Continued)

Signal Name	sysIO Bank	LVDS Pair/Polarity	GDX Block	MRB	SERDES Mode I/O Pin[1]	SERDES Mode I/O Cell[2]	FIFO Mode I/O Cell/Pin[3]	484 fpBGA
GND	5	-	-	-	-	-	-	GND
BK5_IO28	5	94P	5B	12	-	HSI5B_RXD0/TXD0	FIFO5B_DIN0/DOUT0	J4
BK5_IO29	5	94N	5B	13	-	HSI5B_SYDT[5]	-	J3
BK5_IO30	5	95P	5B	14	SS_CLKIN0P	-	-	L6
BK5_IO31/ CLK_OUT0	5	95N	5B	15	SS_CLKIN0N	-	FIFO5B_FULL	L5
GCLK/CE0	-	CLK0P	-	-	-	-	-	L4
SEL0	-	-	-	-	-	-	-	K3
SEL1	-	-	-	-	-	-	-	K2
GCLK/CE1	-	CLK0N	-	-	-	-	-	N1
BK6_IO0/ CLK_OUT1	6	96N	7A	0	SS_CLKOUT0N	-	FIFO7A_EMPTY	N6
BK6_IO1	6	96P	7A	1	SS_CLKOUT0P	-	-	N5
BK6_IO2	6	97N	7A	2	HSI7A_CDRRST	-	FIFO7A_FIFORSTb	M5
BK6_IO3	6	97P	7A	3	FIFO7A_STRDb[6]	-	-	M6
GND	6	-	-	-	-	-	-	GND
BK6_IO4	6	98N	7A	4	HSI7A_SINN	HSI7A_RECCLK	-	P6
BK6_IO5	6	98P	7A	5	HSI7A_SINP	HSI7A_RXD9/TXD9	FIFO7A_DIN9/DOUT9	P5
BK6_IO6	6	99N	7A	6	-	HSI7A_RXD8/TXD8	FIFO7A_DIN8/DOUT8	N3
BK6_IO7	6	99P	7A	7	-	HSI7A_RXD7/TXD7	FIFO7A_DIN7/DOUT7	N2
BK6_IO8	6	100N	7A	8	HSI7A_SYDT[5]	HSI7A_RXD6/TXD6	FIFO7A_DIN6/DOUT6	P3
BK6_IO9	6	100P	7A	9	HSI7_CSLOCK	HSI7A_RXD5/TXD5	FIFO7A_DIN5/DOUT5	P1
BK6_IO10	6	101N	7A	10	HSI7A_SOUTN	HSI7A_RXD4/TXD4	FIFO7A_DIN4/DOUT4	N7
BK6_IO11	6	101P	7A	11	HSI7A_SOUTP	HSI7A_RXD3/TXD3	FIFO7A_DIN3/DOUT3	P7
GND	6	-	-	-	-	-	-	GND
BK6_IO12	6	102N	7A	12	-	HSI7A_RXD2/TXD2	FIFO7A_DIN2/DOUT2	R3
BK6_IO13	6	102P	7A	13	Note 4	HSI7A_RXD1/TXD1	FIFO7A_DIN1/DOUT1	R2
BK6_IO14	6	103N	7A	14	-	HSI7A_RXD0/TXD0	FIFO7A_DIN0/DOUT0	R1
BK6_IO15	6	103P	7A	15	-	HSI7A_SYDT[5]	FIFO7A_ FULL	T1
BK6_IO16	6	104N	6A	0	-	-	FIFO6A_EMPTY	T2
BK6_IO17	6	104P	6A	1	-	-	-	T3
BK6_IO18	6	105N	6A	2	FIFO6A_STRDb[6]	-	-	U1
BK6_IO19	6	105P	6A	3	HSI6A_CDRRSTb	HSI6_RECCLK	FIFO6A_FIFORSTb	U2
GND	6	-	-	-	-	-	-	GND
BK6_IO20/ PLL_FB1	6	106N	6A	4	HSI6A_SOUTN	HSI6A_RXD9/TXD9	FIFO6A_DIN9/DOUT9	R5
BK6_IO21/ VREF6	6	106P	6A	5	HSI6A_SOUTP	HSI6A_RXD8/TXD8	FIFO6A_DIN8/DOUT8	T6
BK6_IO22	6	107N	6A	6	HSI6A_SYDT[5]	HSI6A_RXD7/TXD7	FIFO6A_DIN7/DOUT7	U4
BK6_IO23	6	107P	6A	7	-	HSI6A_RXD6/TXD6	FIFO6A_DIN6/DOUT6	V4
BK6_IO24	6	108N	6A	8	-	HSI6A_RXD5/TXD5	FIFO6A_DIN5/DOUT5	V3
BK6_IO25	6	108P	6A	9	HSI6_CSLOCK	HSI6A_RXD4/TXD4	FIFO6A_DIN4/DOUT4	V2
BK6_IO26	6	109N	6A	10	HSI6A_SINN	HSI6A_RXD3/TXD3	FIFO6A_DIN3/DOUT3	R6
BK6_IO27	6	109P	6A	11	HSI6A_SINP	HSI6A_RXD2/TXD2	FIFO6A_DIN2/DOUT2	R7
BK6_IO28	6	110N	6A	12	Note 4	HSI6A_RXD1/TXD1	FIFO6A_DIN1/DOUT1	W1
BK6_IO29	6	110P	6A	13	-	HSI6A_RXD0/TXD0	FIFO6A_DIN0/DOUT0	V1
BK6_IO30	6	111N	6A	14	-	HSI6A_SYDT[5]	-	W2
BK6_IO31	6	111P	6A	15	-	-	FIFO6A_ FULL	W3

ispGDX2-256 Logic Signal Connections (Continued)

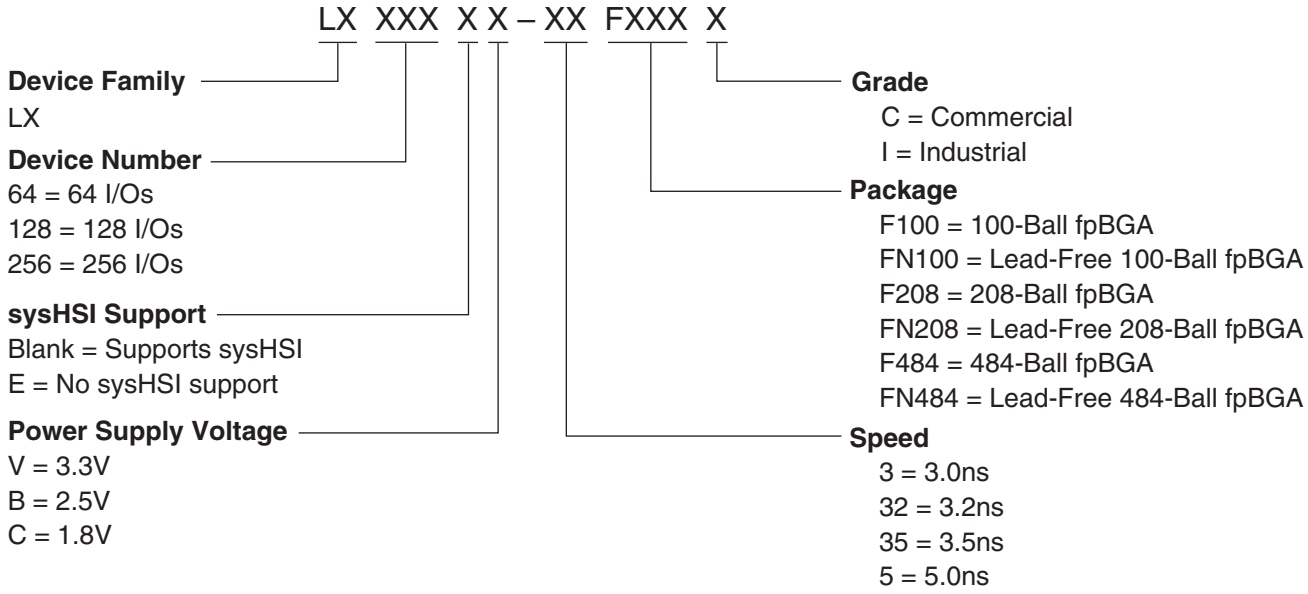
Signal Name	sysIO Bank	LVDS Pair/Polarity	GDX Block	MRB	SERDES Mode I/O Pin[1]	SERDES Mode I/O Cell[2]	FIFO Mode I/O Cell/Pin[3]	484 fpBGA
GND	6	-	-	-	-	-	-	GND
TDI	-	-	-	-	-	-	-	AA4
GOE0	-	-	-	-	-	-	-	Y4
GND	7	-	-	-	-	-	-	GND
BK7_IO0	7	112P	7B	0	-	-	FIFO7B_ EMPTY	AB4
BK7_IO1	7	112N	7B	1	FIFO7B_STRDb[6]	-	-	AB5
BK7_IO2	7	113P	7B	2	HSI7B_CDRRSTb	HSI7B_RECCLK	FIFO7B_FIFORSTb	V6
BK7_IO3	7	113N	7B	3	HSI7B_SYDT[5]	HSI7B_RXD9/TXD9	FIFO7B_DIN9/DOUT9	W5
BK7_IO4	7	114P	7B	4	HSI7B_SINP	HSI7B_RXD8/TXD8	FIFO7B_DIN8/DOUT8	T8
BK7_IO5	7	114N	7B	5	HSI7B_SINN	HSI7B_RXD7/TXD7	FIFO7B_DIN7/DOUT7	T9
BK7_IO6	7	115P	7B	6	-	HSI7B_RXD6/TXD6	FIFO7B_DIN6/DOUT6	W6
BK7_IO7	7	115N	7B	7	-	HSI7B_RXD5/TXD5	FIFO7B_DIN5/DOUT5	Y5
BK7_IO8	7	116P	7B	8	Note 4	HSI7B_RXD4/TXD4	FIFO7B_DIN4/DOUT4	AA5
BK7_IO9	7	116N	7B	9	-	HSI7B_RXD3/TXD3	FIFO7B_DIN3/DOUT3	AA6
BK7_IO10/ VREF7	7	117P	7B	10	HSI7B_SOUTP	HSI7B_RXD2/TXD2	FIFO7B_DIN2/DOUT2	U8
BK7_IO11	7	117N	7B	11	HSI7B_SOUTN	HSI7B_RXD1/TXD1	FIFO7B_DIN1/DOUT1	U9
GND	7	-	-	-	-	-	-	GND
BK7_IO12	7	118P	7B	12	-	HSI7B_RXD0/TXD0	FIFO7B_DIN0/DOUT0	W7
BK7_IO13	7	118N	7B	13	-	HSI7B_SYDT[5]	-	W8
BK7_IO14/ PLL_RST1	7	119P	7B	14	-	-	-	AB6
BK7_IO15	7	119N	7B	15	-	-	FIFO7B_FULL	AB7
BK7_IO16	7	120P	6B	0	FIFO6B_STRDb[6]	-	-	Y7
BK7_IO17	7	120N	6B	1	HSI6B_CDRRSTb	HSI6B_RECCLK	FIFO6B_FIFORSTb	AA7
BK7_IO18	7	121P	6B	2	HSI6B_SYDT[5]	HSI6B_RXD9/TXD9	FIFO6B_DIN9/DOUT9	W9
BK7_IO19	7	121N	6B	3	-	HSI6B_RXD8/TXD8	FIFO6B_DIN8/DOUT8	Y8
GND	7	-	-	-	-	-	-	GND
BK7_IO20	7	122P	6B	4	HSI6B_SOUTP	HSI6B_RXD7/TXD7	FIFO6B_DIN7/DOUT7	T10
BK7_IO21	7	122N	6B	5	HSI6B_SOUTN	HSI6B_RXD6/TXD6	FIFO6B_DIN6/DOUT6	T11
BK7_IO22	7	123P	6B	6	-	HSI6B_RXD5/TXD5	FIFO6B_DIN5/DOUT5	AA8
BK7_IO23	7	123N	6B	7	-	HSI6B_RXD4/TXD4	FIFO6B_DIN4/DOUT4	AB8
BK7_IO24	7	124P	6B	8	Note 4	HSI6B_RXD3/TXD3	FIFO6B_DIN3/DOUT3	W10
BK7_IO25	7	124N	6B	9	-	HSI6B_RXD2/TXD2	FIFO6B_DIN2/DOUT2	Y9
BK7_IO26	7	125P	6B	10	HSI6B_SINP	HSI6B_RXD1/TXD1	FIFO6B_DIN1/DOUT1	U10
BK7_IO27	7	125N	6B	11	HSI6B_SINN	HSI6B_RXD0/TXD0	FIFO6B_DIN0/DOUT0	U11
GND	7	-	-	-	-	-	-	GND
BK7_IO28	7	126P	6B	12	-	HSI6B_SYDT[5]	FIFO6B_ EMPTY	W11
BK7_IO29/ PLL_LOCK1	7	126N	6B	13	-	-	-	Y10
BK7_IO30	7	127P	6B	14	-	-	-	AA10
BK7_IO31	7	127N	6B	15	-	-	FIFO6B_FULL	AB9

ispGDX2-256 Logic Signal Connections (Continued)

Signal Name	sysIO Bank	LVDS Pair/Polarity	GDX Block	MRB	SERDES Mode I/O Pin[1]	SERDES Mode I/O Cell[2]	FIFO Mode I/O Cell/Pin[3]	484 fpBGA
TOE	-	-	-	-	-	-	-	AB10

1. The signals in this column route to/from the assigned pins of the associated I/O cell.
2. The signals in this column use the I/O cell. If a receiver signal is present in the I/O cell, the associated pin is available for output only. When transmit data (TXD) is present in the cell, the associated pin is available for input only.
3. The DOUT outputs are routed to GRP through the input register of the cell and the DIN inputs are routed direct from the associated pins in FIFO only mode. In SERDES with FIFO mode, the FULL and EMPTY flags are routed to the associated pins through the output MUX and the pins.
4. If the Source Synchronous Receiver is used in the HSI Block, this pin is unavailable for another use and must be left unconnected.
5. The SYDT signal has two routing options. If direct output through the dedicated pin is used, the I/O cell (the whole HSI Block) is not available for transmitter. The SYDT in the I/O Cell column is routed to the GRP through the input register of the cell and frees the I/O cell for transmitter.
6. FIFO_STRDb flag output is used in SERDES with FIFO Mode only.
7. sysHSI Source Synchronous Receive Mode is not available for channel 3A.

Part Number Description



Ordering Information

Conventional Packaging

Commercial

Family	Part Number	I/Os	Voltage	t_{PD}	Package	Pins	Grade
LX64V	LX64V-3F100C	64	3.3	3	fpBGA	100	C
	LX64V-5F100C	64	3.3	5	fpBGA	100	C
LX128V	LX128V-32F208C	128	3.3	3.2	fpBGA	208	C
	LX128V-5F208C	128	3.3	5	fpBGA	208	C
LX256V	LX256V-35F484C	256	3.3	3.5	fpBGA	484	C
	LX256V-5F484C	256	3.3	5	fpBGA	484	C
LX64B	LX64B-3F100C	64	2.5	3	fpBGA	100	C
	LX64B-5F100C	64	2.5	5	fpBGA	100	C
LX128B	LX128B-32F208C	128	2.5	3.2	fpBGA	208	C
	LX128B-5F208C	128	2.5	5	fpBGA	208	C
LX256B	LX256B-35F484C	256	2.5	3.5	fpBGA	484	C
	LX256B-5F484C	256	2.5	5	fpBGA	484	C
LX64C	LX64C-3F100C	64	1.8	3	fpBGA	100	C
	LX64C-5F100C	64	1.8	5	fpBGA	100	C
LX128C	LX128C-32F208C	128	1.8	3.2	fpBGA	208	C
	LX128C-5F208C	128	1.8	5	fpBGA	208	C
LX256C	LX256C-35F484C	256	1.8	3.5	fpBGA	484	C
	LX256C-5F484C	256	1.8	5	fpBGA	484	C

"E-Series" Commercial

Family	Part Number	I/Os	Voltage	t_{PD}	Package	Pins	Grade
LX64EV	LX64EV-3F100C	64	3.3	3	fpBGA	100	C
	LX64EV-5F100C	64	3.3	5	fpBGA	100	C
LX128EV	LX128EV-32F208C	128	3.3	3.2	fpBGA	208	C
	LX128EV-5F208C	128	3.3	5	fpBGA	208	C
LX256EV	LX256EV-35F484C	256	3.3	3.5	fpBGA	484	C
	LX256EV-5F484C	256	3.3	5	fpBGA	484	C
LX64EB	LX64EB-3F100C	64	2.5	3	fpBGA	100	C
	LX64EB-5F100C	64	2.5	5	fpBGA	100	C
LX128EB	LX128EB-32F208C	128	2.5	3.2	fpBGA	208	C
	LX128EB-5F208C	128	2.5	5	fpBGA	208	C
LX256EB	LX256EB-35F484C	256	2.5	3.5	fpBGA	484	C
	LX256EB-5F484C	256	2.5	5	fpBGA	484	C
LX64EC	LX64EC-3F100C	64	1.8	3	fpBGA	100	C
	LX64EC-5F100C	64	1.8	5	fpBGA	100	C
LX128EC	LX128EC-32F208C	128	1.8	3.2	fpBGA	208	C
	LX128EC-5F208C	128	1.8	5	fpBGA	208	C

"E-Series" Industrial

Family	Part Number	I/Os	Voltage	t_{PD}	Package	Pins	Grade
LX64EV	LX64EV-5F100I	64	3.3	5	fpBGA	100	I
LX64EB	LX64EB-5F100I	64	2.5	5	fpBGA	100	I
LX64EC	LX64EC-5F100I	64	1.8	5	fpBGA	100	I
LX128EV	LX128EV-5F208I	128	3.3	5	fpBGA	208	I
LX128EB	LX128EB-5F208I	128	2.5	5	fpBGA	208	I
LX128EC	LX128EC-5F208I	128	1.8	5	fpBGA	208	I
LX256EV	LX256EV-5F484I	256	3.3	5	fpBGA	484	I
LX256EB	LX256EB-5F484I	256	2.5	5	fpBGA	484	I
LX256EC	LX256EC-5F484I	256	1.8	5	fpBGA	484	I

Lead-Free Packaging

Commercial

Family	Part Number	I/Os	Voltage	t_{PD}	Package	Pins	Grade
LX64V	LX64V-3FN100C	64	3.3	3.0	Lead-free fpBGA	100	C
	LX64V-5FN100C	64	3.3	5.0	Lead-free fpBGA	100	C
LX64B	LX64B-3FN100C	64	2.5	3.0	Lead-free fpBGA	100	C
	LX64B-5FN100C	64	2.5	5.0	Lead-free fpBGA	100	C
LX64C	LX64C-3FN100C	64	1.8	3.0	Lead-free fpBGA	100	C
	LX64C-5FN100C	64	1.8	5.0	Lead-free fpBGA	100	C
LX128V	LX128V-32FN208C	128	3.3	3.2	Lead-free fpBGA	208	C
	LX128V-5FN208C	128	3.3	5.0	Lead-free fpBGA	208	C
LX128B	LX128B-32FN208C	128	2.5	3.2	Lead-free fpBGA	208	C
	LX128B-5FN208C	128	2.5	5.0	Lead-free fpBGA	208	C
LX128C	LX128C-32FN208C	128	1.8	3.2	Lead-free fpBGA	208	C
	LX128C-5FN208C	128	1.8	5.0	Lead-free fpBGA	208	C
LX256V	LX256V-35FN484C	256	3.3	3.5	Lead-free fpBGA	484	C
	LX256V-5FN484C	256	3.3	5.0	Lead-free fpBGA	484	C
LX256B	LX256B-35FN484C	256	2.5	3.5	Lead-free fpBGA	484	C
	LX256B-5FN484C	256	2.5	5.0	Lead-free fpBGA	484	C
LX256C	LX256C-35FN484C	256	1.8	3.5	Lead-free fpBGA	484	C
	LX256C-5FN484C	256	1.8	5.0	Lead-free fpBGA	484	C

"E-Series" Commercial

Family	Part Number	I/Os	Voltage	t_{PD}	Package	Pins	Grade
LX64EV	LX64EV-3FN100C	64	3.3	3.0	Lead-free fpBGA	100	C
	LX64EV-5FN100C	64	3.3	5.0	Lead-free fpBGA	100	C
LX64EB	LX64EB-3FN100C	64	2.5	3.0	Lead-free fpBGA	100	C
	LX64EB-5FN100C	64	2.5	5.0	Lead-free fpBGA	100	C
LX64EC	LX64EC-3FN100C	64	1.8	3.0	Lead-free fpBGA	100	C
	LX64EC-5FN100C	64	1.8	5.0	Lead-free fpBGA	100	C
LX128EV	LX128EV-32FN208C	128	3.3	3.2	Lead-free fpBGA	208	C
	LX128EV-5FN208C	128	3.3	5.0	Lead-free fpBGA	208	C
LX128EB	LX128EB-32FN208C	128	2.5	3.2	Lead-free fpBGA	208	C
	LX128EB-5FN208C	128	2.5	5.0	Lead-free fpBGA	208	C
LX128EC	LX128EC-32FN208C	128	1.8	3.2	Lead-free fpBGA	208	C
	LX128EC-5FN208C	128	1.8	5.0	Lead-free fpBGA	208	C
LX256EV	LX256EV-35FN484C	256	3.3	3.5	Lead-free fpBGA	484	C
	LX256EV-5FN484C	256	3.3	5.0	Lead-free fpBGA	484	C
LX256EB	LX256EB-35FN484C	256	2.5	3.5	Lead-free fpBGA	484	C
	LX256EB-5FN484C	256	2.5	5.0	Lead-free fpBGA	484	C
LX256EC	LX256EC-35FN484C	256	1.8	3.5	Lead-free fpBGA	484	C
	LX256EC-5FN484C	256	1.8	5.0	Lead-free fpBGA	484	C

"E-Series" Industrial

Family	Part Number	I/Os	Voltage	t_{PD}	Package	Pins	Grade
LX64EV	LX64EV-5FN100I	64	3.3	5.0	Lead-free fpBGA	100	I
LX64EB	LX64EB-5FN100I	64	2.5	5.0	Lead-free fpBGA	100	I
LX64EC	LX64EC-5FN100I	64	1.8	5.0	Lead-free fpBGA	100	I
LX128EV	LX128EV-5FN208I	128	3.3	5.0	Lead-free fpBGA	208	I
LX128EB	LX128EB-5FN208I	128	2.5	5.0	Lead-free fpBGA	208	I
LX128EC	LX128EC-5FN208I	128	1.8	5.0	Lead-free fpBGA	208	I
LX256EV	LX256EV-5FN484I	256	3.3	5.0	Lead-free fpBGA	484	I
LX256EB	LX256EB-5FN484I	256	2.5	5.0	Lead-free fpBGA	484	I
LX256EC	LX256EC-5FN484I	256	1.8	5.0	Lead-free fpBGA	484	I

For Further Information

In addition to this data sheet, the following Lattice technical notes may be helpful when designing with the ispGDX2 Family:

- *sysIO Design and Usage Guidelines* (TN1000)
- s*ysCLOCK PLL Design and Usage Guidelines* (TN1003)
- *sysHSI Usage Guide* (TN1020)
- *Power Estimation in ispGDX2 Devices* (TN1021)