KAI-04022

2048 (H) x 2048 (V) Interline CCD Image Sensor

ON Semiconductor®

www.onsemi.com

Description

The KAI−04022 Image Sensor is a high-performance 4-million pixel sensor designed for a wide range of medical, scientific and machine vision applications. The 7.4 μm square pixels with microlenses provide high sensitivity and the large full well capacity results in high dynamic range. The two high-speed outputs and binning capabilities allow for 16−50 frames per second (fps) video rate for the progressively scanned images. The vertical overflow drain structure provides anti-blooming protection and enables electronic shuttering for precise exposure control. Other features include low dark current, negligible lag and low smear.

Table 1. GENERAL SPECIFICATIONS

Parameter	Typical Value
Architecture	Interline CCD, Progressive Scan
Total Number of Pixels	2112 (H) × 2072 (V)
Number of Effective Pixels	2056 (H) × 2062 (V)
Number of Active Pixels	2048 (H) × 2048 (V)
Pixel Size	7.4 μm (H) × 7.4 μm (V)
Active Image Size	15.15 mm (H) × 15.15 mm (V), 21.43 mm (Diagonal), 4/3″ Optical Format
Aspect Ratio	1:1
Number of Outputs	1 or 2
Charge Capacity	40,000 e^-
Output Sensitivity	33 μV/e^-
Peak Quantum Efficiency KAI−04022−ABA KAI−04022−FBA (BRG) KAI−04022−CBA (BRG)	 50% 44%, 42%, 36% 45%, 42%, 35%
Read Noise (f = 10 MHz)	9 e^-, rms
Dark Current	< 0.5 nA/cm^2
Dark Current Doubling Temp.	7°C
Dynamic Range	72 dB
Charge Transfer Efficiency	> 0.999999
Blooming Suppression	300X
Smear	−80 dB
Image Lag	< 10 e^-
Maximum Frame Rates	8 fps (Single Output) 16 fps (Single Output)
Package	34-pin, CERDIP
Cover Glass	AR Coated, 2-Side

NOTE: All Parameters are specified at T = 40°C unless otherwise noted.

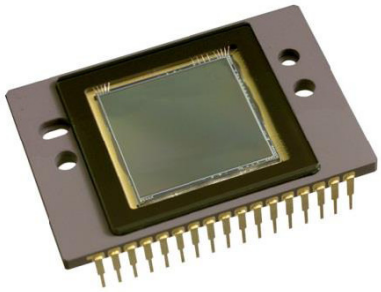


Figure 1. KAI−04022 Interline CCD Image Sensor

Features

- High Resolution
- High Sensitivity
- High Dynamic Range
- Low Noise Architecture
- High Frame Rate
- Binning Capability for Higher Frame Rate
- Electronic Shutter

Applications

- Intelligent Transportation Systems
- Machine Vision
- Scientific Imaging
- Surveillance

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ORDERING INFORMATION

Table 2. ORDERING INFORMATION − KAI−04022 IMAGE SENSOR

Part Number	Description	Marking Code
KAI−04022−AAA−CR−BA	Monochrome, No Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass with AR Coating (2 Sides), Standard Grade	KAI−04022−AAA Serial Number
KAI−04022−AAA−CR−AE	Monochrome, No Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass with AR Coating (2 Sides), Engineering Grade	
KAI−04022−ABA−CD−BA	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass with AR Coating (2 Sides), Standard Grade	KAI−04022−ABA Serial Number
KAI−04022−ABA−CD−AE	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass with AR Coating (2 Sides), Engineering Grade	
KAI−04022−ABA−CR−BA	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass with AR Coating (2 Sides), Standard Grade	
KAI−04022−ABA−CR−AE	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass with AR Coating (2 Sides), Engineering Grade	
KAI−04022−FBA−CD−BA	Color (Bayer RGB), Telecentric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass with AR Coating (2 Sides), Standard Grade	KAI−04022−FBA Serial Number
KAI−04022−FBA−CD−AE	Color (Bayer RGB), Telecentric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass with AR Coating (2 Sides), Engineering Grade	
KAI−04022−FBA−CR−BA	Color (Bayer RGB), Telecentric Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass with AR Coating (2 Sides), Standard Grade	
KAI−04022−FBA−CR−AE	Color (Bayer RGB), Telecentric Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass with AR Coating (2 Sides), Engineering Grade	
KAI−04022−CBA−CD−BA*	Color (Bayer RGB), Telecentric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass with AR Coating (2 Sides), Standard Grade	KAI−04022−CBA Serial Number
KAI−04022−CBA−CD−AE*	Color (Bayer RGB), Telecentric Microlens, CERDIP Package (sidebrazed), Clear Cover Glass with AR Coating (2 Sides), Engineering Grade	
KAI−04022−CBA−CR−BA*	Color (Bayer RGB), Telecentric Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass with AR Coating (2 Sides), Standard Grade	
KAI−04022−CBA−CR−AE*	Color (Bayer RGB), Telecentric Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass with AR Coating (2 Sides), Engineering Grade	

*Not recommended for new designs.

See the ON Semiconductor *Device Nomenclature* document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

DEVICE DESCRIPTION

Architecture

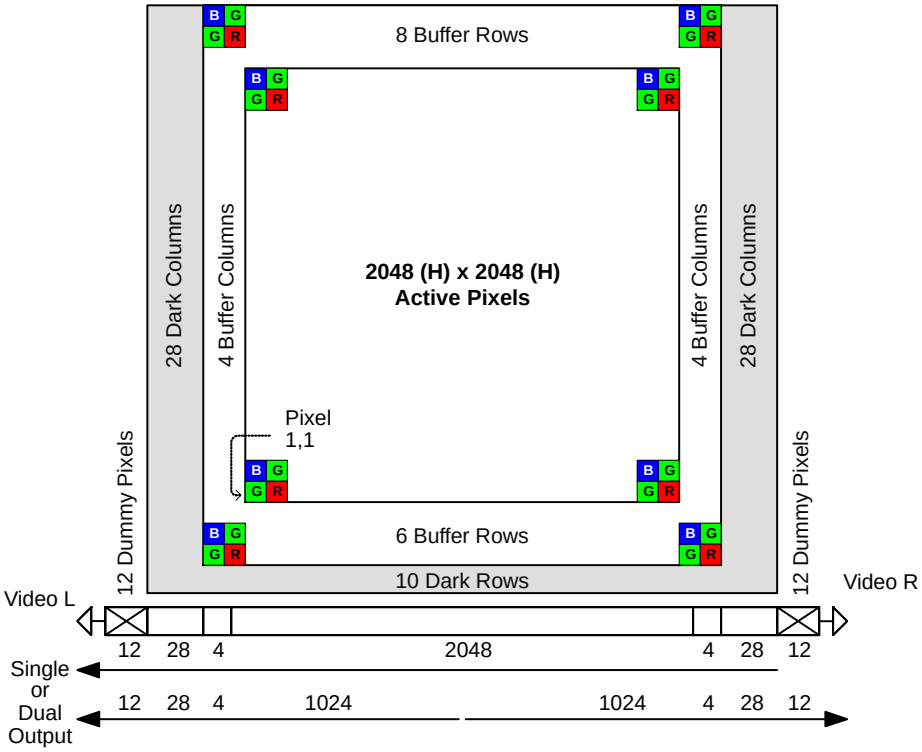


Figure 2. Sensor Architecture

There are 10 light shielded rows followed 2,062 photoactive rows. The first 6 and the last 8 photoactive rows are buffer rows giving a total of 2,048 lines of image data.

In the single output mode all pixels are clocked out of the Video L output in the lower left corner of the sensor. The first 12 empty pixels of each line do not receive charge from the vertical shift register. The next 28 pixels receive charge from the left light-shielded edge followed by 2,056 photo-sensitive pixels and finally 28 more light shielded pixels from the right edge of the sensor. The first and last 4 photosensitive pixels are buffer pixels giving a total of 2,048 pixels of image data.

In the dual output mode the clocking of the right half of the horizontal CCD is reversed. The left half of the image is clocked out Video L and the right half of the image is clocked out Video R. Each row consists of 12 empty pixels followed by 28 light shielded pixels followed by 1,028 photosensitive pixels. When reconstructing the image, data from Video R will have to be reversed in a line buffer and appended to the Video L data.

There are no dark reference rows at the top and 10 dark rows at the bottom of the image sensor. The 10 dark rows are not entirely dark and so should not be used for a dark reference level. Use the 28 dark columns on the left or right side of the image sensor as a dark reference.

Of the 28 dark columns, the first and last dark columns should not be used for determining the zero signal level. Some light does leak into the first and last dark columns. Only use the center 26 columns of the 28 column dark reference.

Pixel

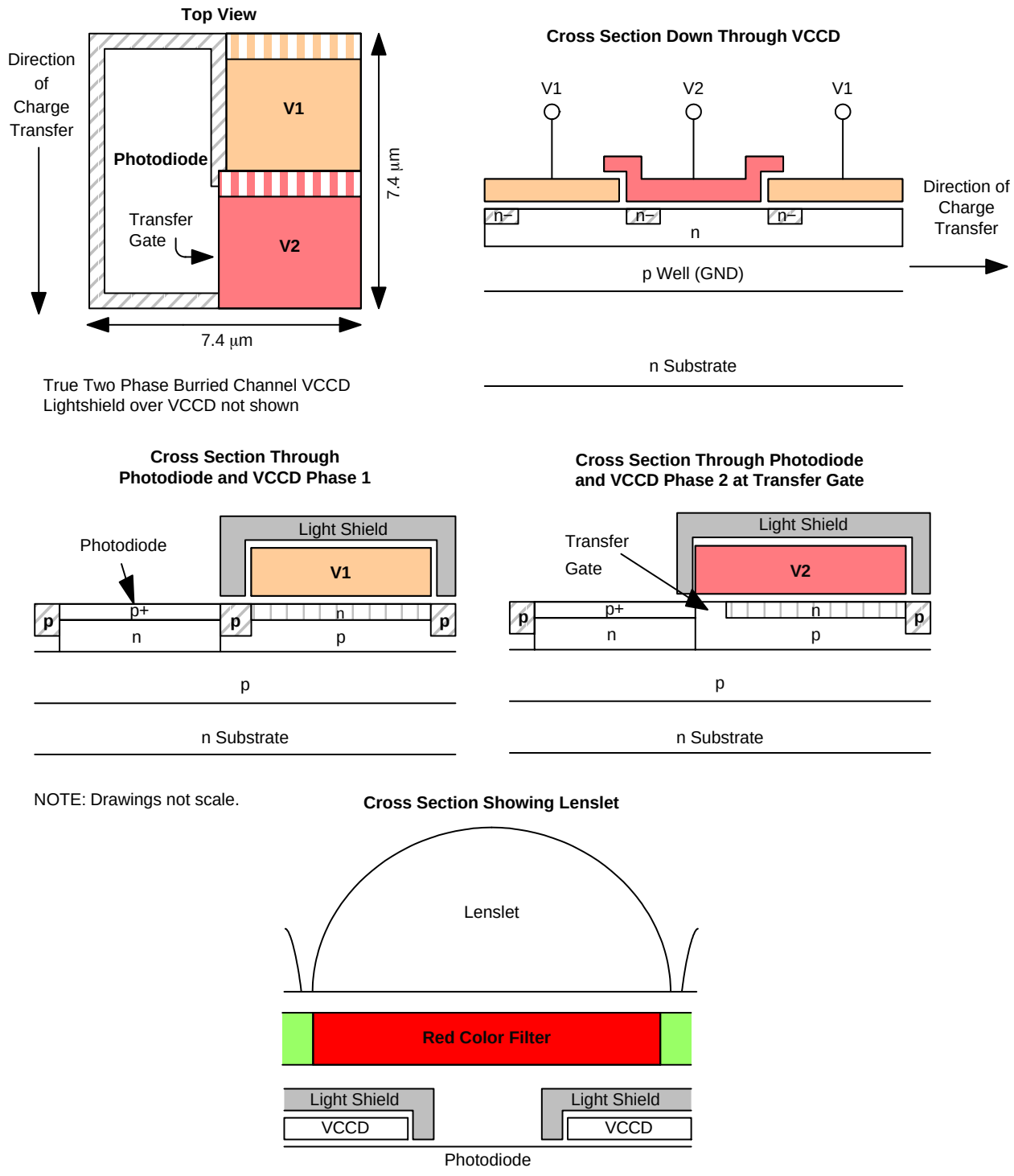


Figure 3. Pixel Architecture

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the individual silicon photodiodes. These photoelectrons are collected locally by the formation of potential wells at each photosite. Below photodiode saturation, the number of photoelectrons collected at each pixel is linearly dependent upon light level and exposure time and non-linearly dependent on wavelength. When the photodiodes charge capacity is reached, excess electrons are discharged into the substrate to prevent blooming.

Vertical to Horizontal Transfer

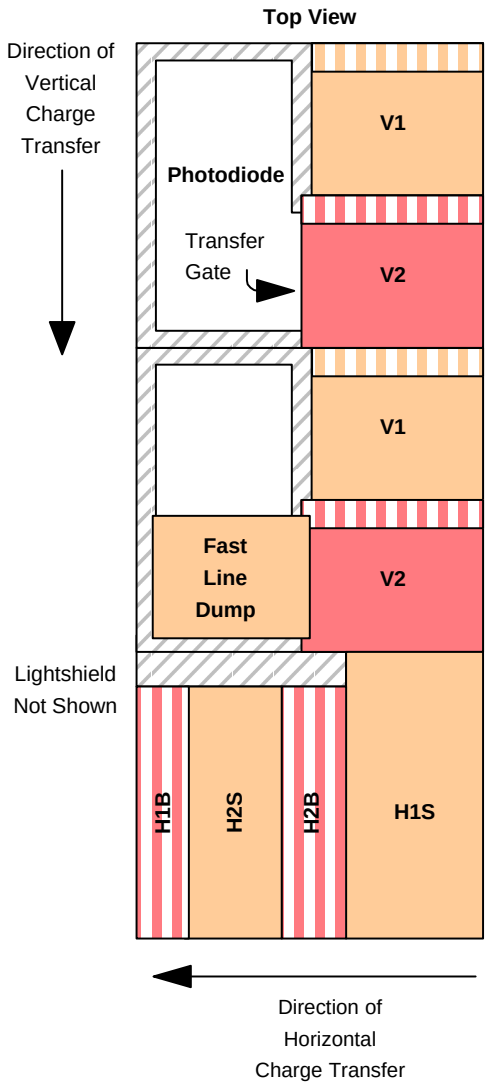


Figure 4. Vertical to Horizontal Transfer Architecture

When the V1 and V2 timing inputs are pulsed, charge in every pixel of the VCCD is shifted one row towards the HCCD. The last row next to the HCCD is shifted into the HCCD. When the VCCD is shifted, the timing signals to the HCCD must be stopped. H1 must be stopped in the high state and H2 must be stopped in the low state. The HCCD clocking may begin t_{HD} μs after the falling edge of the V1 and V2 pulse.

Charge is transferred from the last vertical CCD phase into the H1S horizontal CCD phase. Refer to Figure 36 for an example of timing that accomplishes the vertical to horizontal transfer of charge.

If the fast line dump is held at the high level (FDH) during a vertical to horizontal transfer, then the entire line is removed and not transferred into the horizontal register.

Horizontal Register to Floating Diffusion

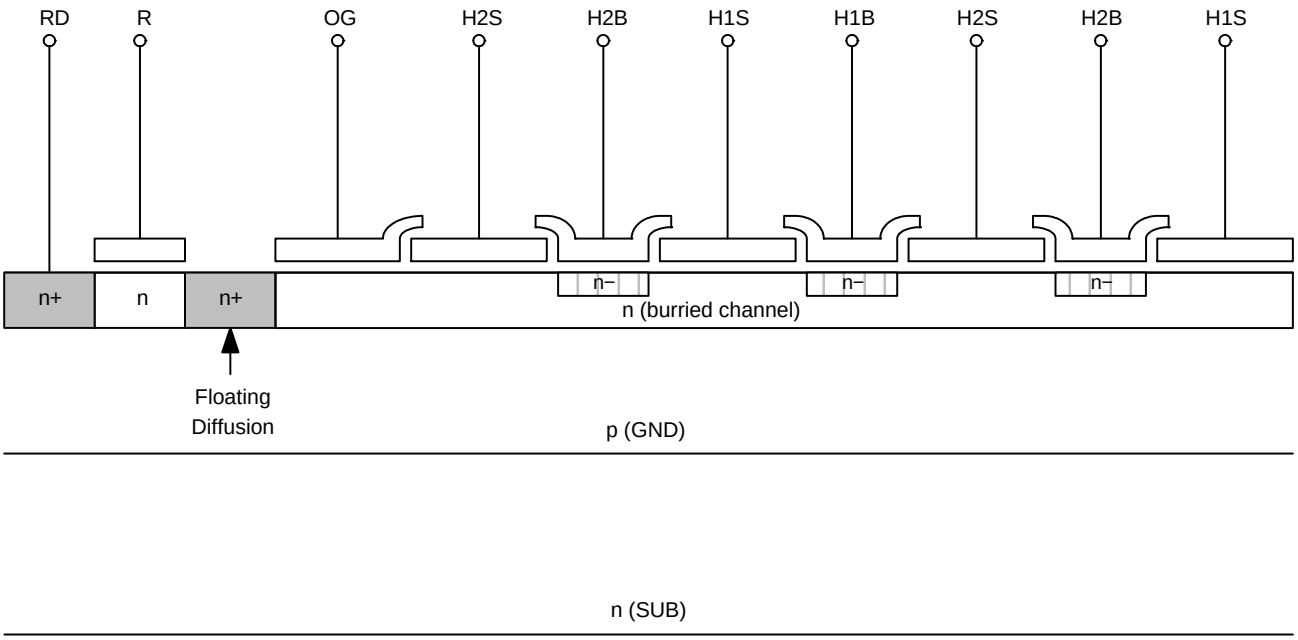


Figure 5. Horizontal Register to Floating Diffusion Architecture

The HCCD has a total of 2,124 pixels. The 2,112 vertical shift registers (columns) are shifted into the center 2,112 pixels of the HCCD. There are 12 pixels at both ends of the HCCD, which receive no charge from a vertical shift register. The first 12 clock cycles of the HCCD will be empty pixels (containing no electrons). The next 28 clock cycles will contain only electrons generated by dark current in the VCCD and photodiodes. The next 2,056 clock cycles will contain photo-electrons (image data). Finally, the last 28 clock cycles will contain only electrons generated by dark current in the VCCD and photodiodes. Of the 28 dark columns, the first and last dark columns should not be used for determining the zero signal level. Some light does leak into the first and last dark columns. Only use the center 26 columns of the 28 column dark reference.

When the HCCD is shifting valid image data, the timing inputs to the electronic shutter (SUB), VCCD (V1, V2), and fast line dump (FD) should be not be pulsed. This prevents unwanted noise from being introduced. The HCCD is a type of charge coupled device known as a pseudo-two phase CCD. This type of CCD has the ability to shift charge in two directions. This allows the entire image to be shifted out to the video L output, or to the video R output (left/right image reversal). The HCCD is split into two equal halves of 1,068 pixels each. When operating the sensor in single output mode the two halves of the HCCD are shifted in the same direction. When operating the sensor in dual output mode the two halves of the HCCD are shifted in opposite directions. The direction of charge transfer in each half is controlled by the H1BL, H2BL, H1BR, and H2BR timing inputs.

Horizontal Register Split

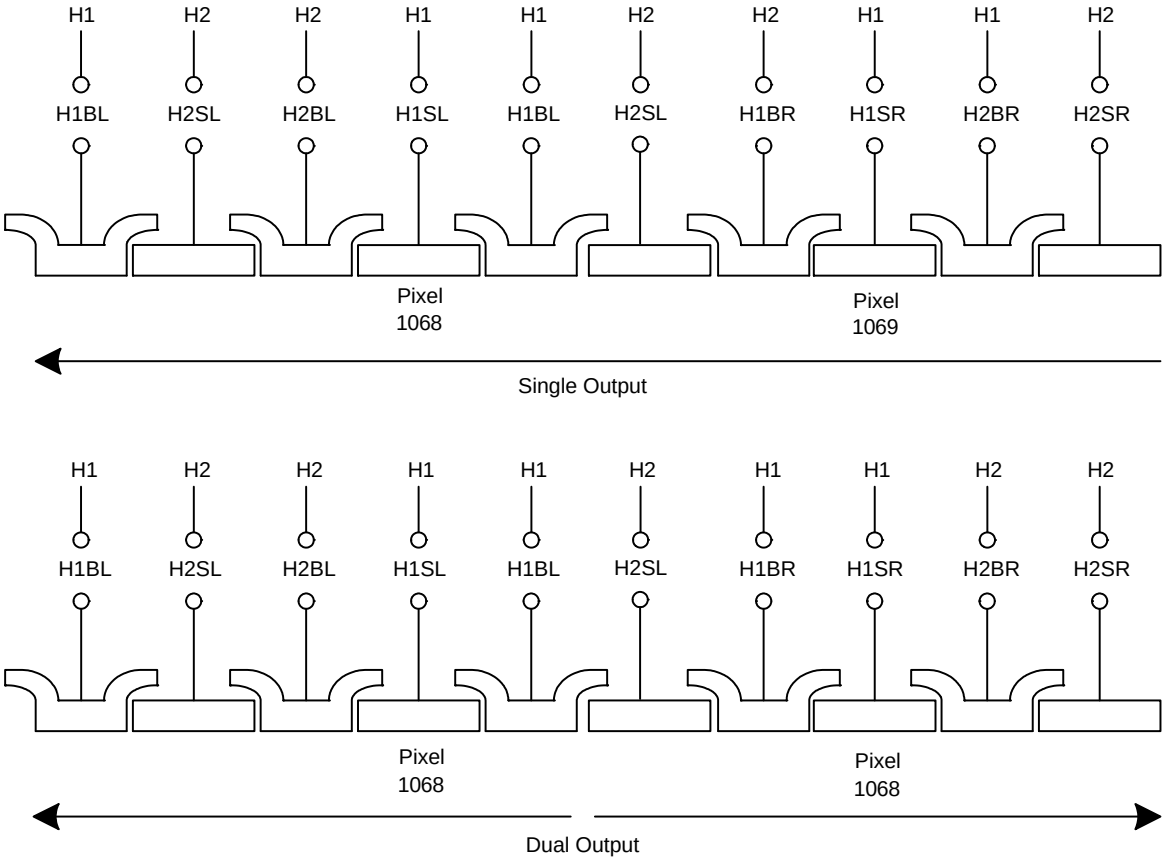


Figure 6. Horizontal Register

Single Output Operation

When operating the sensor in single output mode all pixels of the image sensor will be shifted out the Video L output (pin 12). To conserve power and lower heat generation the output amplifier for Video R may be turned off by connecting VDDR (pin 24) and VOUTR (pin 23) to GND (0 V).

The H1 timing from the timing diagrams should be applied to H1SL, H1BL, H1SR, H2BR, and the H2 timing should be applied to H2SL, H2BL, H2SR, and H1BR. In other words, the clock driver generating the H1 timing should be connected to pins 16, 15, 19, and 21. The clock driver generating the H2 timing should be connected to pins 17, 14, 18, and 20. The horizontal CCD should be clocked for 12 empty pixels plus 28 light shielded pixels plus 2,056 photoactive pixels plus 28 light shielded pixels for a total of 2,124 pixels.

Dual Output Operation

In dual output mode the connections to the H1BR and H2BR pins are swapped from the single output mode to change the direction of charge transfer of the right side horizontal shift register. In dual output mode both VDDL and VDDR (pins 11, 24) should be connected to 15 V. The H1 timing from the timing diagrams should be applied to H1SL, H1BL, H1SR, H1BR, and the H2 timing should be applied to H2SL, H2BL, H2SR, and H2BR. The clock driver generating the H1 timing should be connected to pins 16, 15, 19, and 20. The clock driver generating the H2 timing should be connected to pins 17, 14, 18, and 21. The horizontal CCD should be clocked for 12 empty pixels plus 28 light shielded pixels plus 1,028 photoactive pixels for a total of 1,068 pixels. If the camera is to have the option of dual or single output mode, the clock driver signals sent to H1BR and H2BR may be swapped by using a relay. Another alternative is to have two extra clock drivers for H1BR and H2BR and invert the signals in the timing logic generator. If two extra clock drivers are used, care must be taken to ensure the rising and falling edges of the H1BR and H2BR clocks occur at the same time (within 3 ns) as the other HCCD clocks.

Output

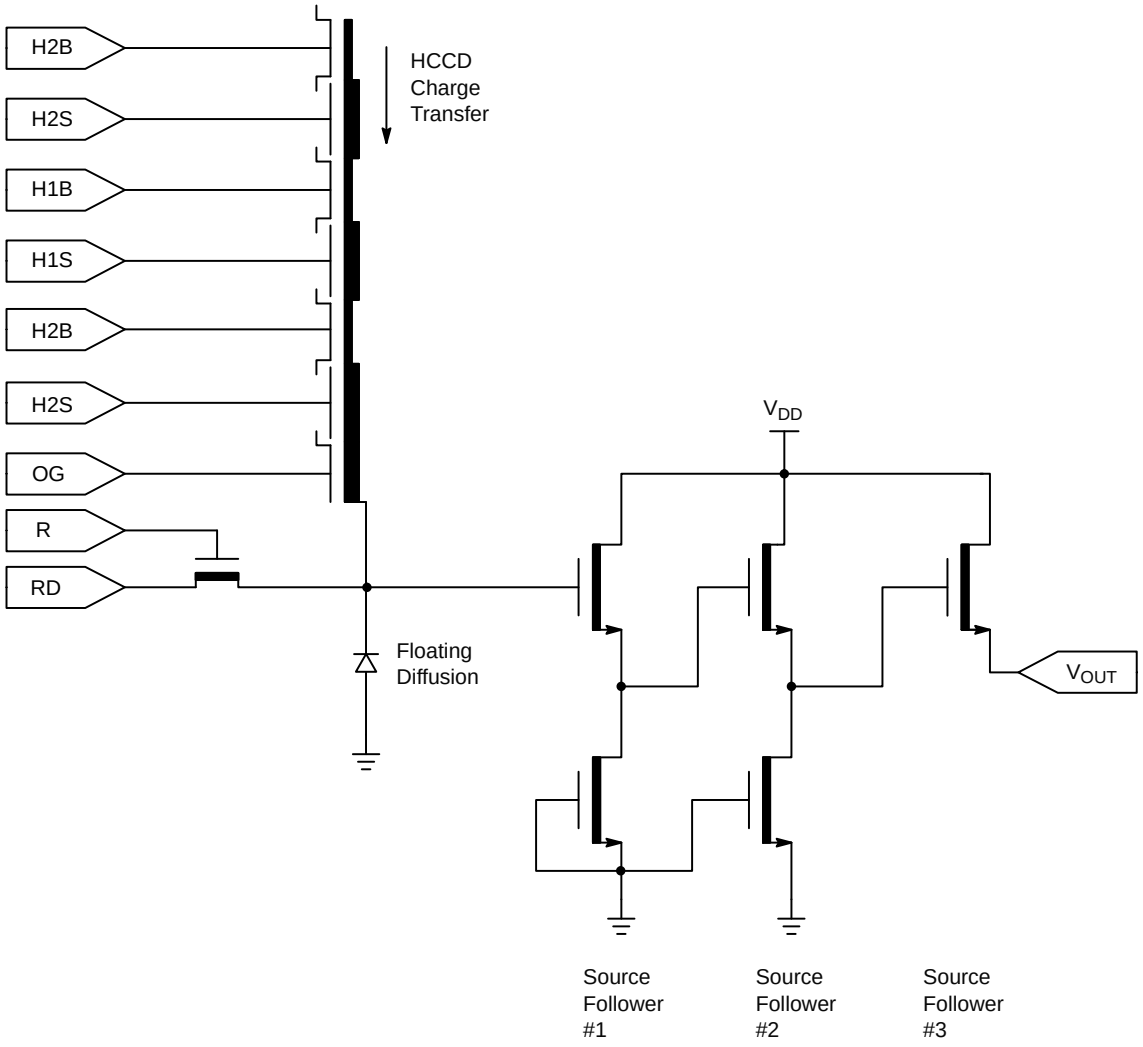


Figure 7. Output Architecture

Charge packets contained in the horizontal register are dumped pixel by pixel onto the floating diffusion (FD) output node whose potential varies linearly with the quantity of charge in each packet. The amount of potential charge is determined by the expression $\Delta V_{FD} = \Delta Q / C_{FD}$. A three-stage source-follower amplifier is used to buffer this signal voltage off chip with slightly less than unity gain. The translation from the charge domain to the voltage domain is quantified by the output sensitivity or charge to voltage conversion in terms of microvolts per electron ($\mu V/e^-$). After the signal has been sampled off chip, the reset clock (R) removes the charge from the floating diffusion and resets its potential to the reset drain voltage (RD).

When the image sensor is operated in the binned or summed interlaced modes there will be more than 20,000 electrons in the output signal. The image sensor is designed with a 31 μV/e charge to voltage conversion on the output. This means a full signal of 20,000 electrons will produce a 640 mV change on the output amplifier. The output amplifier was designed to handle an output swing of 640 mV at a pixel rate of 40 MHz. If 40,000 electron charge packets are generated in the binned or summed interlaced modes then the output amplifier output will have to swing 1,280 mV. The output amplifier does not have enough bandwidth (slew rate) to handle 1,280 mV at 40 MHz. Hence, the pixel rate will have to be reduced to 20 MHz if the full dynamic range of 40,000 electrons is desired.

The charge handling capacity of the output amplifier is also set by the reset clock voltage levels. The reset clock driver circuit is very simple, if an amplitude of 5 V is used. But the 5 V amplitude restricts the output amplifier charge capacity to 20,000 electrons. If the full dynamic range of 40,000 electrons is desired then the reset clock amplitude will have to be increased to 7 V.

If you only want a maximum signal of 20,000 electrons in binned or summed interlaced modes, then a 40 MHz pixel rate with a 5 V reset clock may be used. The output of the amplifier will be unpredictable above 20,000 electrons so be sure to set the maximum input signal level of your analog to digital converter to the equivalent of 20,000 electrons (640 mV).

The following table summarizes the previous explanation on the output amplifier's operation. Certain trade-offs can be made based on application needs such as Dynamic Range or Pixel frequency.

Table 3. OUTPUT AMPLIFIER'S OPERATION

Pixel Frequency (MHz)	Reset Clock Amplitude (V)	Output Gate (V)	Saturation Signal (mV)	Saturation Signal (ke^-)	Notes
40	5	−2	640	20	
20	5	−2	640	20	
20	7	−3	1280	40	
20	7	−3	2560	80	1

1. 80,000 electrons achievable in summed interlaced or binning modes.

ESD Protection

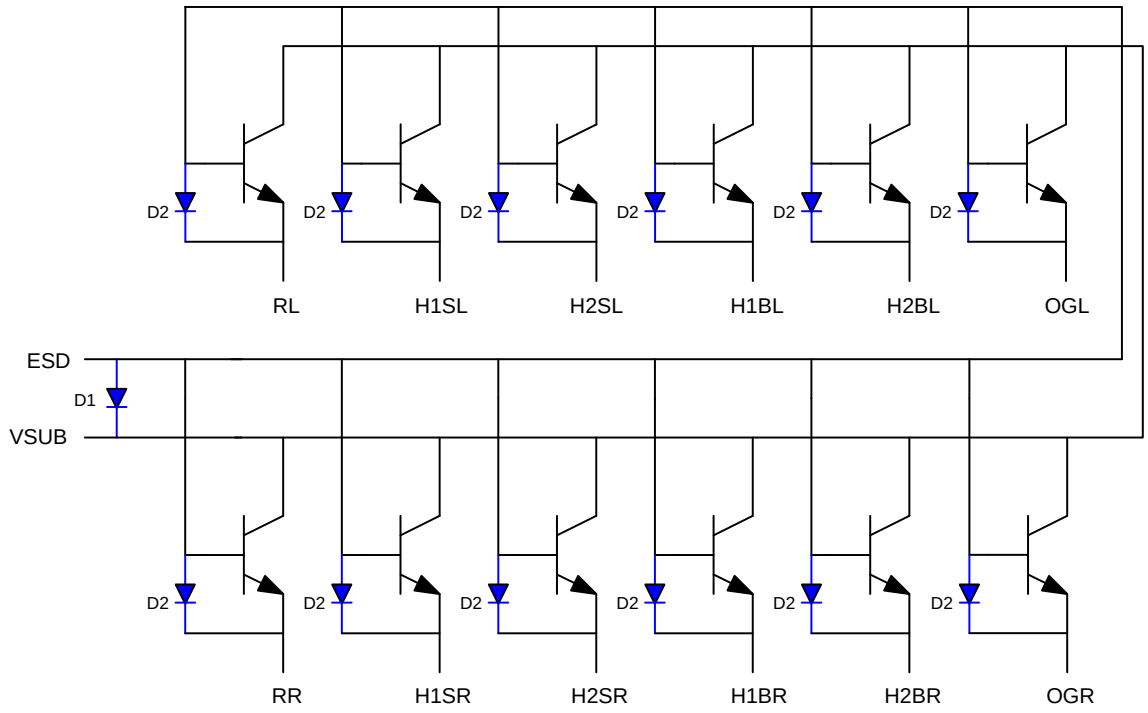


Figure 8. ESD Protection

The ESD protection on the KAI−04022 is implemented using bipolar transistors. The substrate (VSUB) forms the common collector of all the ESD protection transistors. The ESD pin is the common base of all the ESD protection transistors. Each protected pin is connected to a separate emitter as shown in Figure 8.

The ESD circuit turns on if the base-emitter junction voltage exceeds 17 V. Care must be taken while operating the image sensor, especially during the power on sequence, to not forward bias the base-emitter or base-collector junctions. If it is possible for the camera power up sequence to forward bias these junctions then diodes D1 and D2 should be added to protect the image sensor. Put one diode D1 between the ESD and VSUB pins. Put one diode D2 on each pin that may forward bias the base-emitter junction. The diodes will prevent large currents from flowing through the image sensor. Note that external diodes D1 and D2 are optional and are only needed if it is possible to forward bias any of the junctions.

Note that diodes D1 and D2 are added external to the KAI−04022.

Pin Description and Physical Orientation

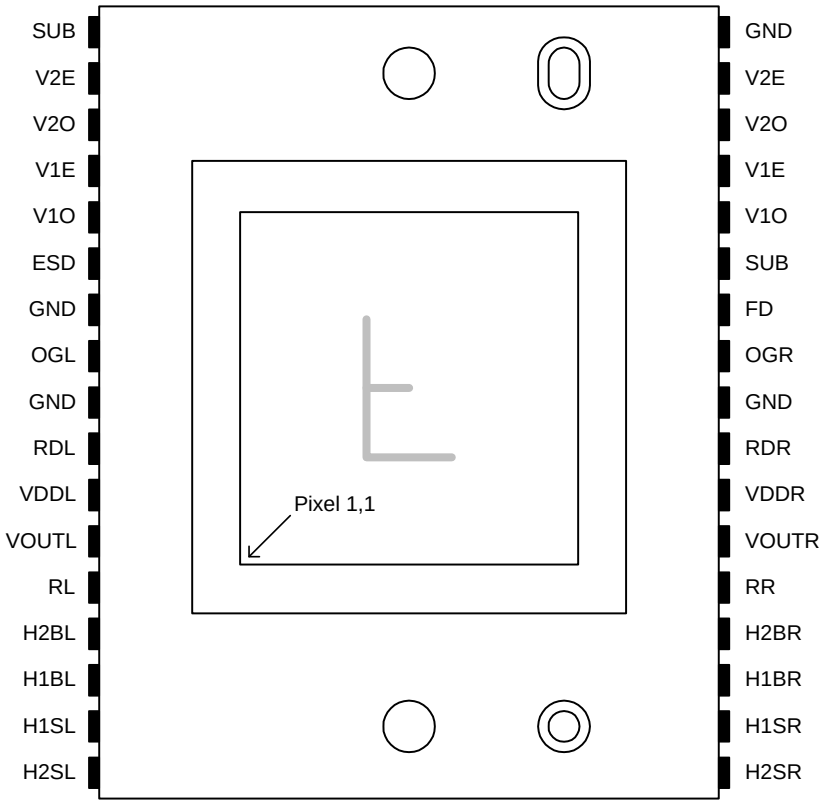


Figure 9. Package Pin Description− Top View

Table 4. PIN DESCRIPTION

Pin	Name	Description
1	SUB	Substrate
2	V2E	Vertical Clock, Phase 2, Even
3	V2O	Vertical Clock, Phase 2, Odd
4	V1E	Vertical Clock, Phase 1, Even
5	V1O	Vertical Clock, Phase 1, Odd
6	ESD	ESD
7	GND	Ground
8	OGL	Output Gate, Left
9	GND	Ground
10	RDL	Reset Drain, Left
11	VDDL	VDD, Left
12	VOUTL	Video Output, Left
13	RL	Reset Gate, Left
14	H2BL	H2 Barrier, Left
15	H1BL	H1 Barrier, Left
16	H1SL	H1 Storage, Left
17	H2SL	H2 Storage, Left

Pin	Name	Description
18	H2SR	H2 Storage, Right
19	H1SR	H1 Storage, Right
20	H1BR	H1 Barrier, Right
21	H2BR	H2 Barrier, Right
22	RR	Reset Gate, Right
23	VOUTR	Video Output. Right
24	VDDR	VDD, Right
25	RDR	Reset Drain, Right
26	GND	Ground
27	OGR	Output Gate. Right
28	FD	Fast Line Dump Gate
29	SUB	Substrate
30	V1O	Vertical Clock, Phase 1, Odd
31	V1E	Vertical Clock, Phase 1, Even
32	V2O	Vertical Clock, Phase 2, Odd
33	V2E	Vertical Clock, Phase 2, Even
34	GND	Ground

NOTE: The pins are on a 0.070″ spacing.

IMAGING PERFORMANCE

Table 5. TYPICAL OPERATIONAL CONDITIONS

(Unless otherwise noted, the Imaging Performance Specifications are measured using the following conditions.)

Description	Condition
Frame Time (Note 1)	538 ms
Horizontal Clock Frequency	10 MHz
Light Source (Notes 2, 3)	Continuous Red, Green and Blue LED Illumination Centered at 450, 530 and 650 nm
Operation	Nominal Operating Voltages and Timing

1. Electronic shutter is not used. Integration time equals frame time.
2. LEDs used: Blue: Nichia NLPB500, Green: Nichia NSPG500S and Red: HP HLMP−8115.
3. For monochrome sensor, only green LED used.

Specifications

Table 6. PERFORMANCE SPECIFICATIONS

Description	Symbol	Min.	Nom.	Max.	Unit	Sample Plan	Temperature Tested at (°C)
ALL CONFIGURATIONS							
Dark Center Non-Uniformity		N/A	N/A	2	mV rms	Die	27, 40
Dark Global Non-Uniformity		N/A	N/A	5.0	m Vpp	Die	27, 40
Global Non-Uniformity (Note 1)		N/A	2.5	5.0	% rms	Die	27, 40
Global Peak to Peak Non-Uniformity (Note 1)	PRNU	N/A	10	20	% pp	Die	27, 40
Center Non-Uniformity (Note 1)		N/A	1.0	2.0	% rms	Die	27, 40
Maximum Photoresponse Non-Linearity (Notes 2, 3)	NL	N/A	2	−	%	Design	
Maximum Gain Difference Between Outputs (Notes 2, 3)	ΔG	N/A	10	−	%	Design	
Max. Signal Error due to Non-Linearity Dif. (Notes 2, 3)	ΔNL	N/A	1	−	%	Design	
Horizontal CCD Charge Capacity	H_{Ne}	−	100	−	ke^-	Design	
Vertical CCD Charge Capacity	V_{Ne}	50	60	−	ke^-	Die	
Photodiode Charge Capacity	P_{Ne}	38	40	−	ke^-	Die	
Horizontal CCD Charge Transfer Efficiency	HCTE	0.99999	−	N/A		Design	
Vertical CCD Charge Transfer Efficiency	VCTE	0.99999	−	N/A		Design	
Photodiode Dark Current	I_{PD}	N/A	40	350	$e^-/p/s$	Die	
Photodiode Dark Current	I_{PD}	N/A	0.01	0.1	nA/cm^2	Die	
Vertical CCD Dark Current	I_{VD}	N/A	400	1711	$e^-/p/s$	Die	
Vertical CCD Dark Current	I_{VD}	N/A	0.12	0.5	nA/cm^2	Die	
Image Lag	Lag	N/A	< 10	50	e^-	Design	
Anti-Blooming Factor	X_{AB}	100	300	N/A			
Vertical Smear	Smr	N/A	−80	−75	dB		
Read Noise (Note 4)	n_{e-T}	−	9	−	e^- rms	Design	
Dynamic Range (Notes 4, 5)	DR	−	72	−	dB	Design	
Output Amplifier DC Offset	V_{ODC}	4	8.5	14	V	Die	
Output Amplifier Bandwidth	f_{-3dB}	−	140	−	MHz	Design	

Table 6. PERFORMANCE SPECIFICATIONS (continued)

Description	Symbol	Min.	Nom.	Max.	Unit	Sample Plan	Temperature Tested at (°C)
ALL CONFIGURATIONS							
Output Amplifier Impedance	R_{OUT}	100	130	200	Ω	Die	
Output Amplifier Sensitivity	ΔV/ΔN	−	31	−	μV/e⁻	Design	
KAI−04022−ABA CONFIGURATION							
Peak Quantum Efficiency	QE_{MAX}	−	55	−	%	Design	
Peak Quantum Efficiency Wavelength	λQE	−	470	−	nm	Design	
KAI−04022−FBA GEN2 COLOR CONFIGURATIONS							
Peak Quantum Efficiency Red Green Blue	QE_{MAX}	 − − −	 36 42 44	 − − −	%	Design	
Peak Quantum Efficiency Wavelength Red Green Blue	λQE	 − − −	 605 530 455	 − − −	nm	Design	
KAI−04022−CBA GEN1 COLOR CONFIGURATIONS (Note 6)							
Peak Quantum Efficiency Red Green Blue	QE_{MAX}	 − − −	 35 42 45	 − − −	%	Design	
Peak Quantum Efficiency Wavelength Red Green Blue	λQE	 − − −	 620 540 470	 − − −	nm	Design	

NOTE: N/A = Not Applicable.

1. Per color.
2. Value is over the range of 10% to 90% of photodiode saturation.
3. Value is for the sensor operated without binning.
4. At 10 MHz.
5. Uses 20LOG (P_{Ne} / n_{e-T}).
6. This color filter set configuration (Gen1) is not recommended for new designs.

TYPICAL PERFORMANCE CURVES

Quantum Efficiency

Monochrome with Microlens

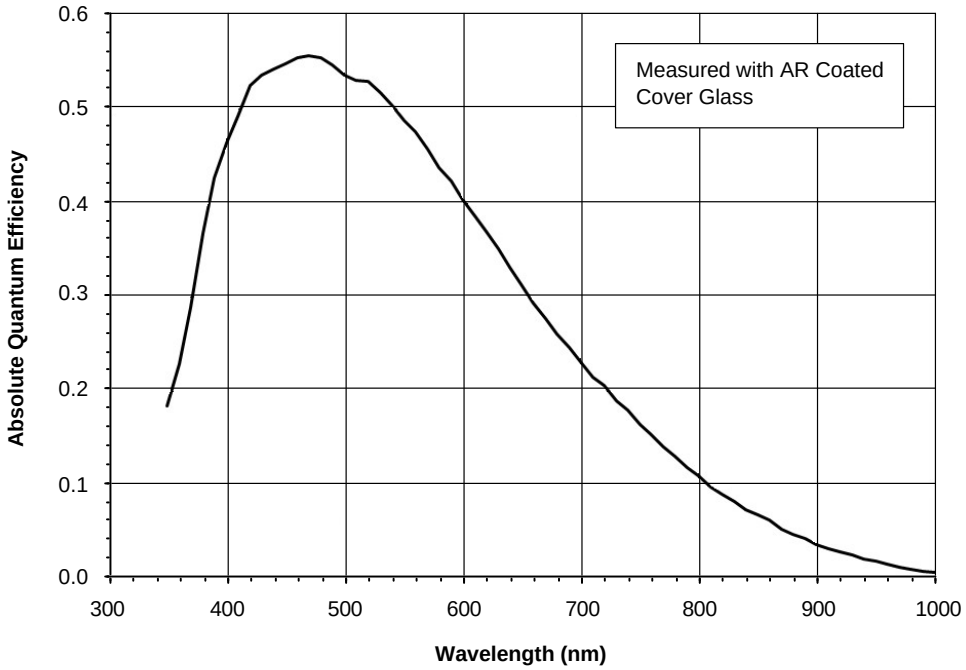


Figure 10. Monochrome with Microlens Quantum Efficiency

Monochrome without Microlens

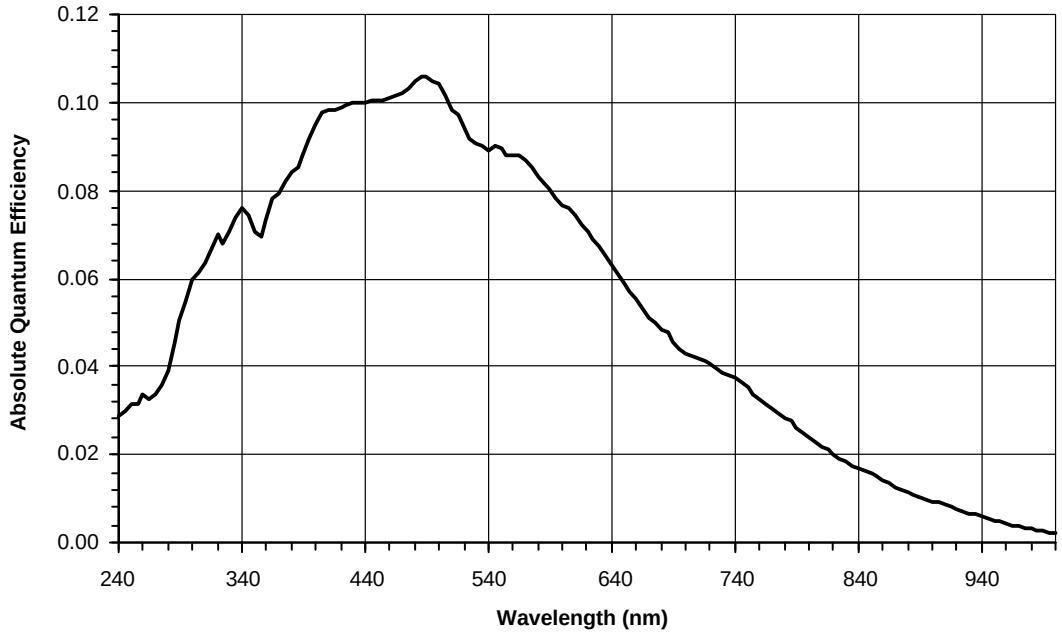


Figure 11. Monochrome without Microlens Quantum Efficiency

Color (Bayer RGB) with Microlens

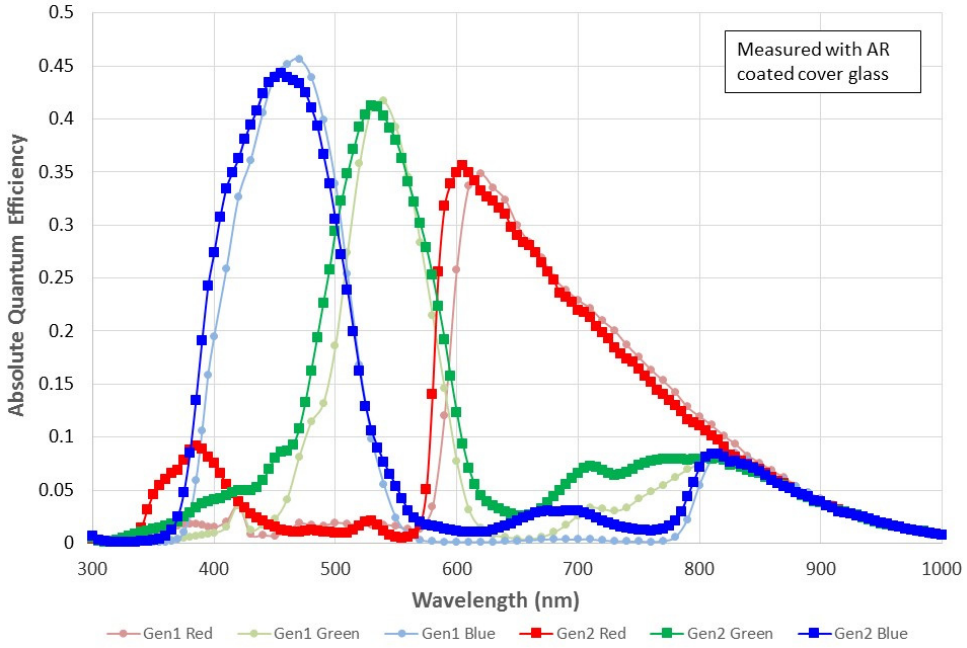


Figure 12. Color Quantum Efficiency

Angular Quantum Efficiency

For the curves marked “Horizontal”, the incident light angle is varied in a plane parallel to the HCCD.
For the curves marked “Vertical”, the incident light angle is varied in a plane parallel to the VCCD.

Monochrome with Microlens

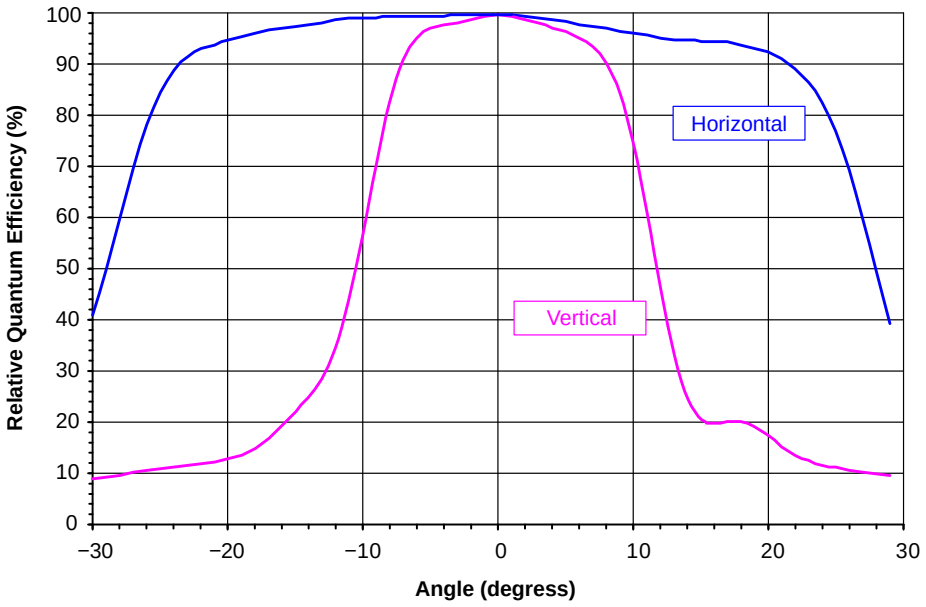


Figure 13. Monochrome with Microlens Angular Quantum Efficiency

Dark Current vs. Temperature

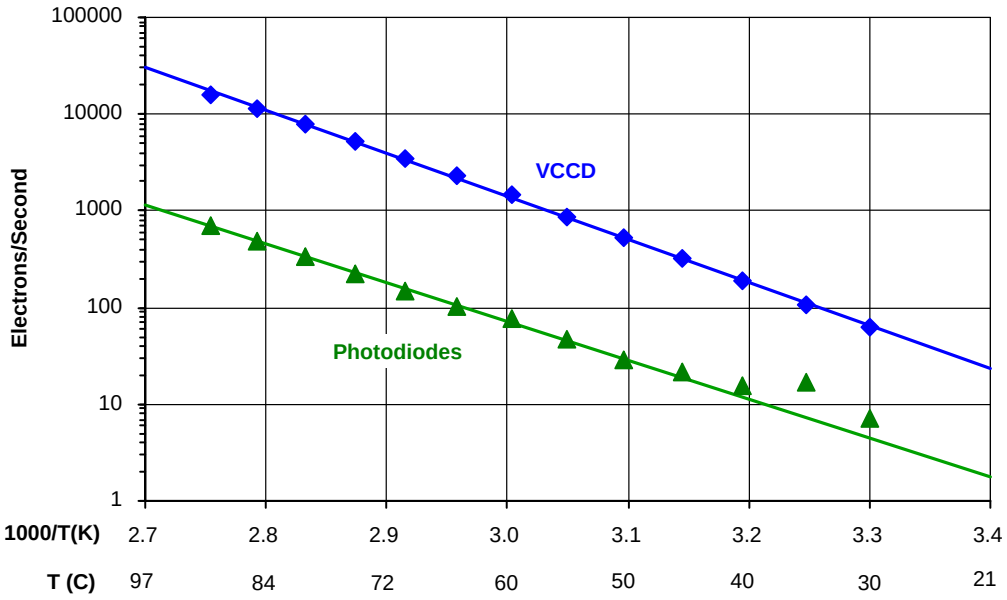


Figure 14. Dark Current vs. Temperature

Power-Estimated

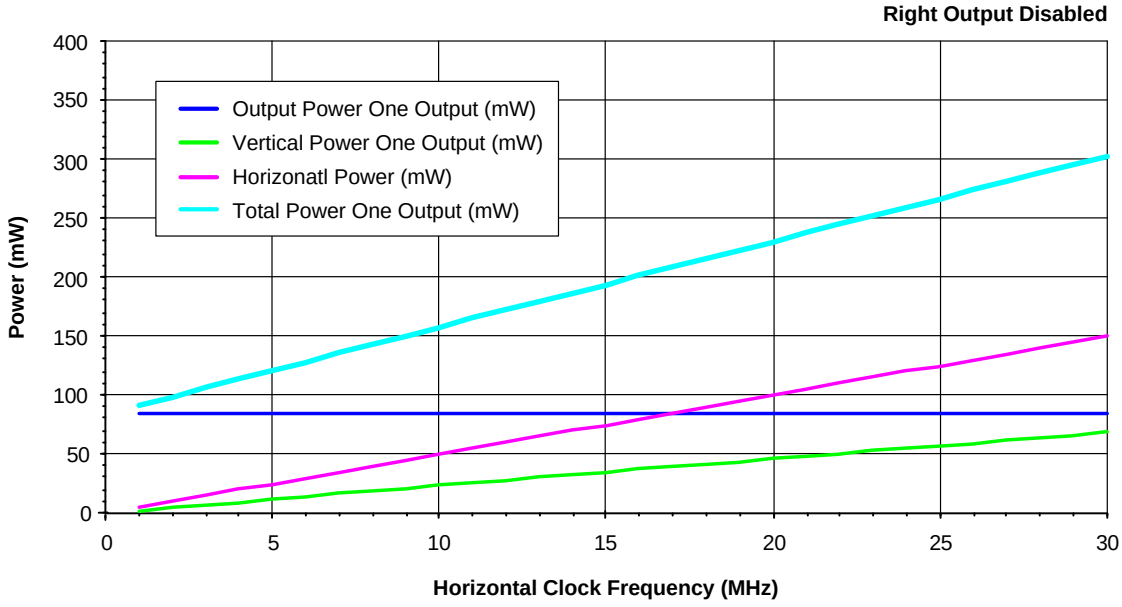


Figure 15. Power

Frame Rates

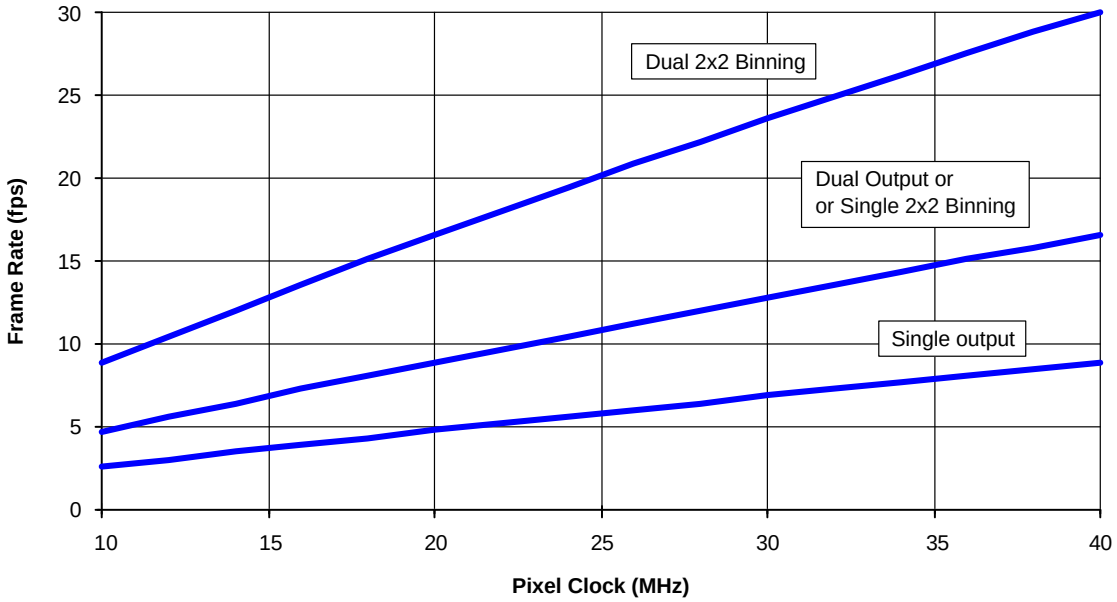


Figure 16. Frame Rates

DEFECT DEFINITIONS

Table 7. DEFECT DEFINITIONS

Description	Definition	Maximum	Temperature(s) Tested at (°C)
Major Dark Field Defective Pixel (Note 1)	Defect ≥ 148 mV	40	27, 40
Major Bright Field Defective Pixel (Note 1)	Defect ≥ 10%	40	27, 40
Minor Dark Field Defective Pixel	Defect ≥ 76 mV	400	27, 40
Dead Pixel (Note 1)	Defect ≥ 80%	5	27, 40
Saturated Pixel (Note 1)	Defect ≥ 340 mV	10	27, 40
Cluster Defect (Note 1)	A group of 2 to 10 contiguous major defective pixels, but no more than 2 adjacent defects horizontally	8	27, 40
Column Defect (Note 1)	A group of more than 10 contiguous major defective pixels along a single column	0	27, 40

1. There will be at least two non-defective pixels separating any two major defective pixels.

Defect Map

The defect map supplied with each sensor is based upon testing at an ambient (27°C) temperature. Minor point defects are not included in the defect map. All defective pixels are reference to pixel 1,1 in the defect maps.

TEST DEFINITIONS

Test Regions of Interest

Active Area ROI: Pixel (1, 1) to Pixel (2048, 2048)
Center 100 by 100 ROI: Pixel (974, 974) to Pixel (1073, 1073)

Only the active pixels are used for performance and defect tests.

Overclocking

The test system timing is configured such that the sensor is overclocked in both the vertical and horizontal directions. See Figure 17 for a pictorial representation of the regions.

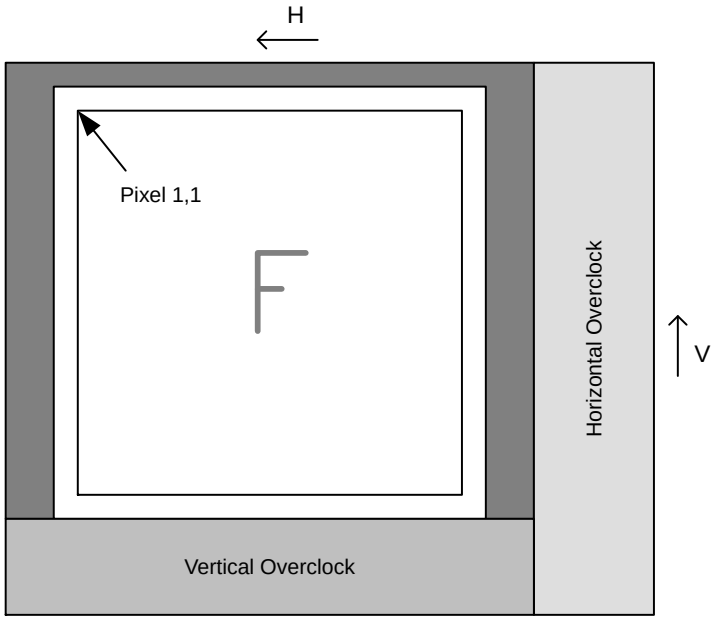


Figure 17. Overclock Regions of Interest

Tests

Dark Field Center Non-Uniformity

This test is performed under dark field conditions. Only the center 100 by 100 pixels of the sensor are used for this test − pixel (974, 974) to pixel (1073, 1073).

$$\text{Dark Field Center Non−Uniformity} = \text{Standard Deviation of Center 100 by 100 Pixels}$$

Units : mV rms

Dark Field Global Non-Uniformity

This test is performed under dark field conditions. The sensor is partitioned into 256 sub regions of interest, each of which is 128 by 128 pixels in size. The average signal level of each of the 256 sub regions of interest is calculated. The signal level of each of the sub regions of interest is calculated using the following formula:

$$\text{Signal of ROI[i]} = (\text{ROI Average in ADU} - \text{Horizontal Overclock Average in ADU}) \cdot \text{mV per Count}$$

Units : mVpp (millivolts Peak to Peak)

Where i = 1 to 256. During this calculation on the 256 sub regions of interest, the maximum and minimum signal levels are found. The dark field global non-uniformity is then calculated as the maximum signal found minus the minimum signal level found.

Global Non-Uniformity

This test is performed with the imager illuminated to a level such that the output is at 70% of saturation (approximately 868 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 1,240 mV. Global non-uniformity is defined as:

$$\text{Global Non−Uniformity} = 100 \cdot \left(\frac{\text{Active Area Standard Deviation}}{\text{Active Area Signal}}\right)$$

Units : % rms
Active Area Signal = Active Area Average − H. Column Average

Global Peak to Peak Non-Uniformity

This test is performed with the imager illuminated to a level such that the output is at 70% of saturation (approximately 868 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 1,240 mV. The sensor is partitioned into 256 sub regions of interest, each of which is 128 by 128 pixels in size. The average signal level of each of the 256 sub regions of interest (ROI) is calculated. The signal level of each of the sub regions of interest is calculated using the following formula:

$$A[i] = (\text{ROI Average} - \text{Horizontal Overclock Average})$$

Where i = 1 to 256. During this calculation on the 256 sub regions of interest, the maximum and minimum average signal levels are found. The global peak to peak non−uniformity is then calculated as:

$$\text{Global Non−Uniformity} = 100 \cdot \frac{\text{A[i] Max. Signal} - \text{A[i] Min. Signal}}{\text{Active Area Signal}}$$

Units : % pp

Active Area Signal = Active Area Average − H. Column Average

Center Non-Uniformity

This test is performed with the imager illuminated to a level such that the output is at 70% of saturation (approximately 868 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 1,240 mV. Defects are excluded for the calculation of this test. This test is performed on the center 100 by 100 pixels (See Test Regions of Interest) of the sensor. Center non-uniformity is defined as:

$$\text{Center ROI Non−Uniformity} = 100 \cdot \frac{\text{Center ROI Standard Deviation}}{\text{Center ROI Signal}}$$

Units : % rms

Center ROI Signal = Center ROI Average −H. Colum Average

Dark Field Defect Test

This test is performed under dark field conditions. The sensor is partitioned into 256 sub regions of interest, each of which is 128 by 128 pixels in size. In each region of interest, the median value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the defect threshold specified in “Defect Definitions” section.

Bright Field Defect Test

This test is performed with the imager illuminated to a level such that the output is at 70% of saturation (approximately 28,000 electrons). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 40,000 electrons. The average signal level of all active pixels is found. The bright and dark thresholds are set as:

$$\text{Dark Defect Threshold} = \text{Active Area Signal} \cdot \text{Threshold}$$

$$\text{Bright Defect Threshold} = \text{Active Area Signal} \cdot \text{Threshold}$$

The sensor is then partitioned into 256 sub regions of interest, each of which is 128 by 128 pixels in size. In each region of interest, the average value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the bright threshold specified or if it is less than or equal to the median value of that region of interest minus the dark threshold specified.

Example for major bright field defective pixels:

- Average value of all active pixels is found to be 868 mV (28,000 electrons)
- Dark defect threshold: 868 mV · 15% = 130.2 mV
- Bright defect threshold: 868 mV · 15% = 130.2 mV
- Region of interest #1 selected. This region of interest is pixels 1,1 to pixels 128,128
  - Median of this region of interest is found to be 868 mV.
  - Any pixel in this region of interest that is ≥ (868 + 130.2 mV) 998.2 mV in intensity will be marked defective.
  - Any pixel in this region of interest that is ≤ (868 − 130.2 mV) 737.8 mV in intensity will be marked defective.
- All remaining 255 sub-regions of interest are analyzed for defective pixels in the same manner

OPERATION

Absolute Maximum Ratings

Absolute maximum rating is defined as a level or condition that should not be exceeded at any time per the description. If the level or the condition is exceeded, the device will be degraded and may be damaged.

Table 8. ABSOLUTE MAXIMUM RATINGS

Description	Symbol	Minimum	Maximum	Unit
Operating Temperature (Note 1)	T_{OP}	−50	70	°C
Humidity (Note 2)	RH	5	90	%
Output Bias Current (Note 3)	I_{OUT}	0.0	10	mA
Off-Chip Load (Note 4)	C_L	−	10	pF

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Noise performance will degrade at higher temperatures.
2. T = 25°C. Excessive humidity will degrade MTTF.
3. Each output. See Figure 18. Note that the current bias affects the amplifier bandwidth.
4. With total output load capacitance of C_L = 10 pF between the outputs and AC ground.

Table 9. MAXIMUM VOLTAGE RATINGS BETWEEN PINS

Description	Minimum	Maximum	Unit
RL, RR, H1S, H2S, H1BL, H2BL, H1BR, H2BR, OGR, OGL to ESD	0	17	V
Pin to Pin with ESD Protection (Note 1)	−17	17	V
VDDL, VDDR to GND	0	25	V

1. Pins with ESD protection are: RL, RR, H1S, H2S, H1BL, H2BL, H1BR, H2BR, OGL, and OGR.

Table 10. DC BIAS OPERATING CONDITIONS

Description	Symbol	Minimum	Nominal	Maximum	Unit	Maximum DC Current
Output Gate (Notes 4, 5)	OG	−3.0	−2.0	−1.5	V	1 μA
Reset Drain (Note 4)	RD	11.5	12.0	12.5	V	1 μA
Output Amplifier Supply (Note 3)	V_{DD}	14.5	15.0	15.5	V	1 mA
Ground	GND	0.0	0.0	0.0	V	
Substrate (Notes 1, 7)	VSUB	8.0	V_{AB}	17.0	V	
ESD Protection (Note 2)	ESD	−9.5	−9.0	−8.0	V	
Output Bias Current (Note 6)	I_{OUT}	0.0	5.0	10.0	mA	

1. The operating value of the substrate voltage, V_{AB}, will be marked on the shipping container for each device. The value V_{AB} is set such that the photodiode charge capacity is 40,000 electrons.
2. VESD must be equal to FDL and more negative than H1L, H2L and RL during sensors operation AND during camera power turn on.
3. One output, unloaded. The maximum DC current is for one output unloaded and is shown as I_{SS} in Figure 18. This is the maximum current that the first two stages of one output amplifier will draw. This value is with V_{OUT} disconnected.
4. May be changed in future versions.
5. Output gate voltage level must be set to –3 V for 40,000 – 80,000 electrons output in summed interlaced or binning modes.
6. One output.
7. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions.*

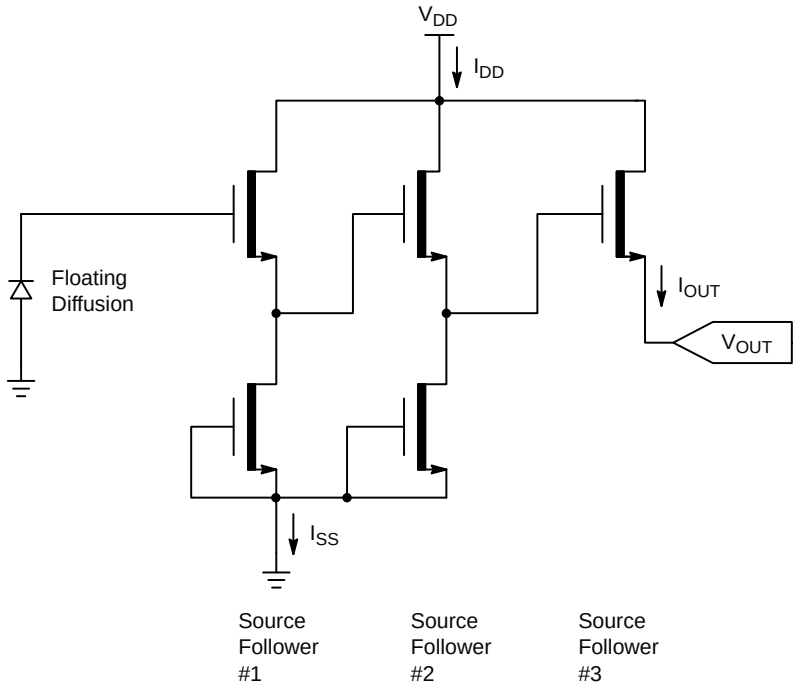


Figure 18. Output Architecture

AC Operating Conditions

Table 11. CLOCK LEVELS

Description	Symbol	Minimum	Nominal	Maximum	Unit
Vertical CCD Clock High	V2H	8.5	9.0	9.5	V
Vertical CCD Clocks Midlevel	V1M, V2M	−0.5	0.0	0.2	V
Vertical CCD Clocks Low	V1L, V2L	−9.5	−9.0	−8.5	V
Horizontal CCD Clocks High	H1H, H2H	0.0	0.5	1.0	V
Horizontal CCD Clocks Low	H1L, H2L	−5.0	−4.5	−4.0	V
Reset Clock Amplitude	RH	−	5.0	−	V
Reset Clock Low	RL	−3.5	−3.0	−2.5	V
Electronic Shutter Voltage (Note 2)	$V_{SHUTTER}$	44	48	52	V
Fast Dump High	FDH	4	5	5	V
Fast Dump Low (Note 1)	FDL	−9.5	−9.0	−8.0	V

1. Reset amplitude must be set to 7.0 V for 40,000 – 80,000 electrons output in summed interlaced or binning modes.
2. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions.*

Clock Line Capacitances

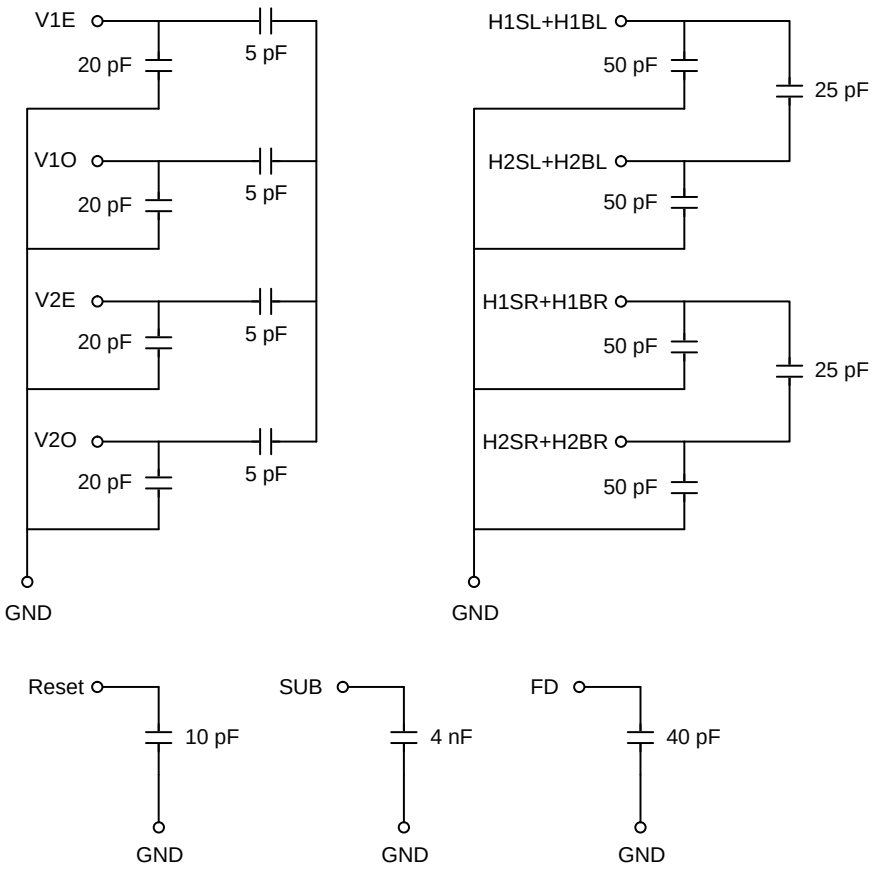


Figure 19. Clock Line Capacitances

TIMING

Table 12. TIMING REQUIREMENTS

Description	Symbol	Minimum	Nominal	Maximum	Unit
HCCD Delay	t_{HD}	1.3	1.5	10.0	μs
VCCD Transfer Time	t_{VCCD}	1.3	1.5	20.0	μs
Photodiode Transfer Time	t_{V3rd}	3.0	5.0	15.0	μs
VCCD Pedestal Time	t_{3P}	50.0	60.0	80.0	μs
VCCD Delay	t_{3D}	10.0	20.0	80.0	μs
Reset Pulse Time	t_R	2.5	5.0	−	ns
Shutter Pulse Time	t_S	3.0	4.0	10.0	μs
Shutter Pulse Delay	t_{SD}	1.0	1.5	10.0	μs
HCCD Clock Period (Note 1)	t_H	25.0	50.0	200.0	ns
VCCD Rise/Fall Time	t_{VR}	0.0	0.1	1.0	μs
Fast Dump Gate Delay	t_{FD}	0.5	−	−	μs
Vertical Clock Edge Alignment	t_{VE}	0.0	−	100	ns

1. For operation at the minimum HCCD clock period (40 MHz), the substrate voltage will need to be raised to limit the signal at the output to 20,000 electrons.

Timing Modes

Progressive Scan

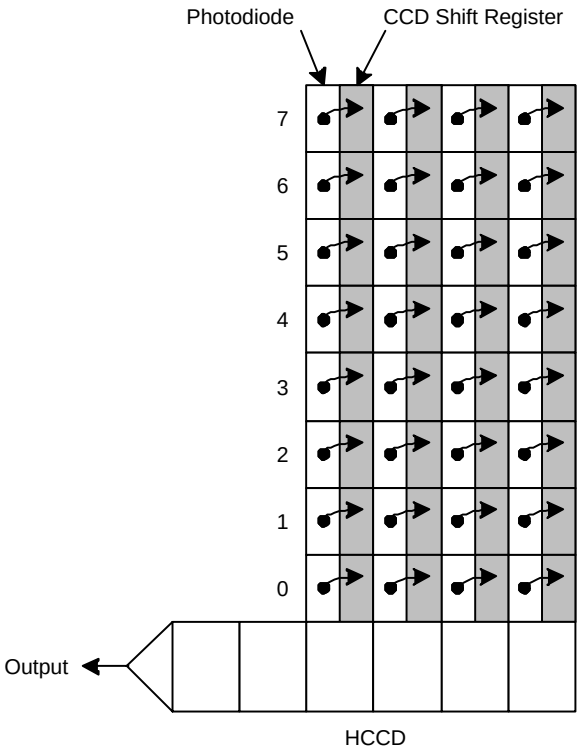


Figure 20. Progressive Scan Operation

In progressive scan read out every pixel in the image sensor is read out simultaneously. Each charge packet is transferred from the photodiode to the neighboring vertical CCD shift register simultaneously. The maximum useful signal output is limited by the photodiode charge capacity to 40,000 electrons.

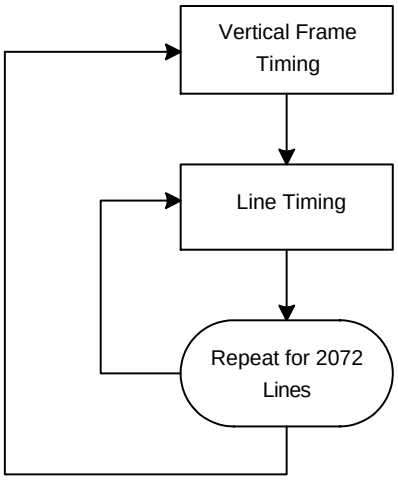


Figure 21. Progressive Scan Flow Chart

Summed Interlaced Scan

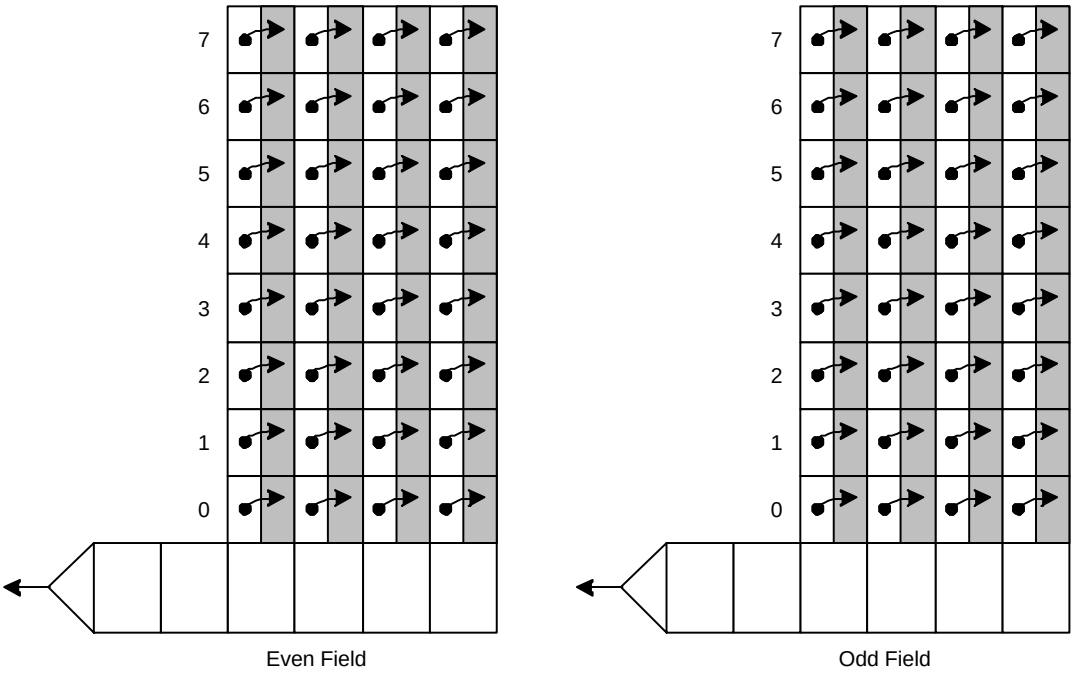


Figure 22. Summed Interlaced Scan Operation

In the summed interlaced scan read out mode, charge from two photodiodes is summed together inside the vertical CCD. The clocking of the VCCD is such that one pixel occupies the space equivalent to two pixels in the progressive scan mode. This allows the VCCD to hold twice as many electrons as in progressive scan mode. Now the maximum useful signal is limited by the charge capacity of two photodiodes at 80,000 electrons. If only one field is read out of the image sensor the apparent vertical resolution will be 1,024 rows instead of the 2,048 rows in progressive scan (equivalent to binning). To recover the full resolution of the image sensor two fields, even and odd, are read out. In the even field rows 0 + 1, 2 + 3, 4 + 5, … are summed together. In the odd field rows 1 + 2, 3 + 4, 5 + 6, … are summed together.

The modulation transfer function (MTF) of the summed interlaced scan mode is less in the vertical direction than the progressive scan. But the dynamic range is twice that of progressive scan. The vertical MTF is better than a simple binning operation. In this mode the VCCD needs to be clocked for only 1,037 rows to read out each field.

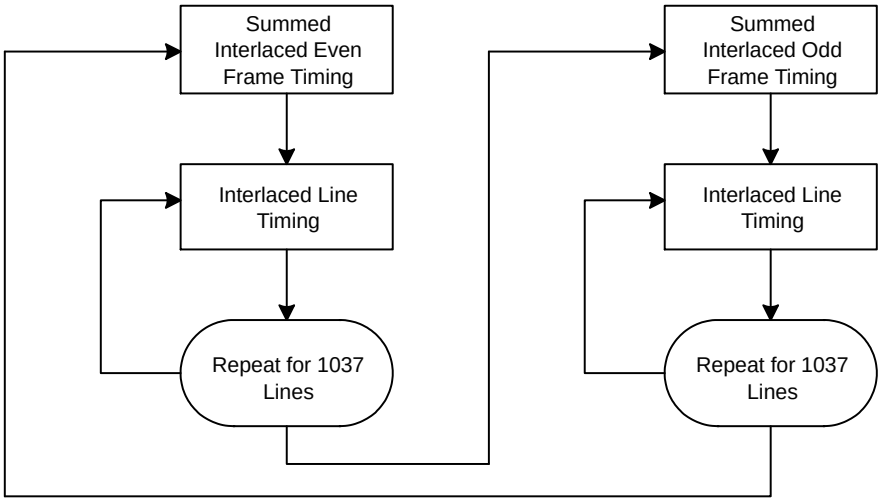


Figure 23. Summed Interlaced Scan Flow Chart

Non-Summed Interlaced Scan

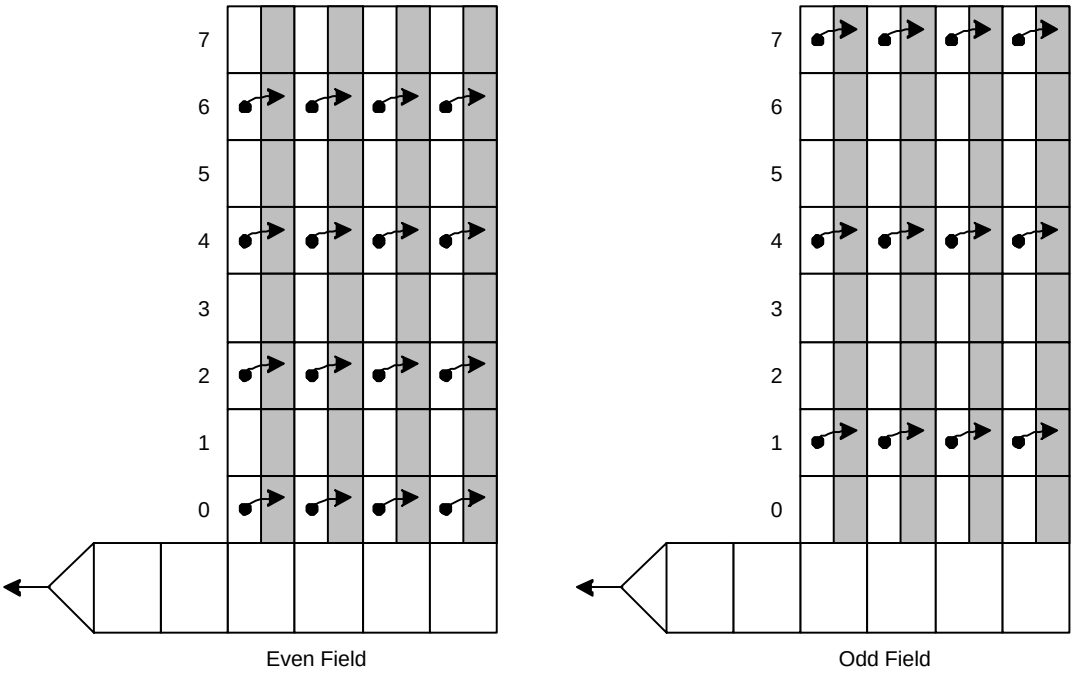


Figure 24. Non-Summed Interlaced Scan Operation

In the non-summed interlaced scan mode only half the photodiode are read out in each field. In the even field rows 0, 2, 4, … are transferred to the VCCD. In the odd field rows 1, 3, 5, … are transferred to the VCCD. When the charge packet is transferred from a photodiode is occupies the equivalent of two rows in progressive scan mode. This allows the VCCD to hold twice as much charge a progressive scan mode. However, since only one photodiode for each row is transferred to the VCCD the maximum usable signal is still only 40,000 electrons. The large extra capacity of the VCCD causes the anti-blooming protection to be increased dramatically compared to the progressive scan. The vertical MTF is the same between the non-summed interlaced scan and progressive scan. There will be motion related artifacts in the images read out in the interlaced modes because the two fields are acquired at different times.

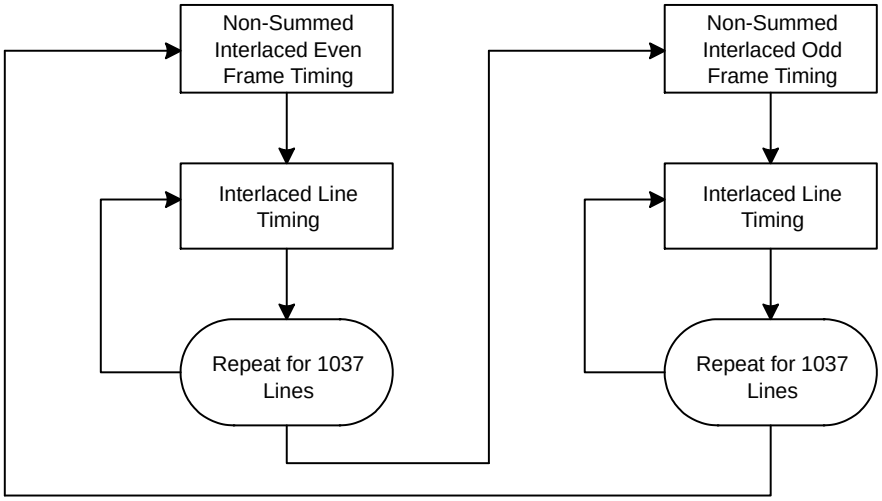


Figure 25. Non-Summed Interlaced Scan Flow Chart

Frame Timing

Frame Timing without Binning − Progressive Scan

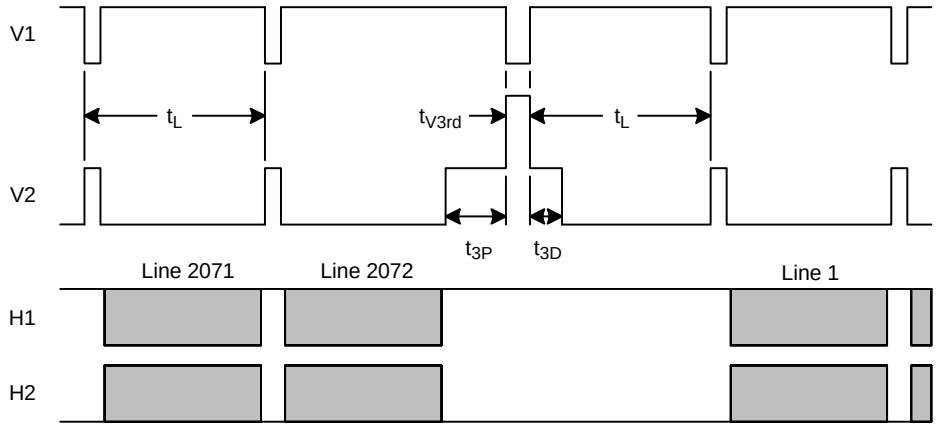


Figure 26. Frame Timing without Binning

Frame Timing for Vertical Binning by 2 − Progressive Scan

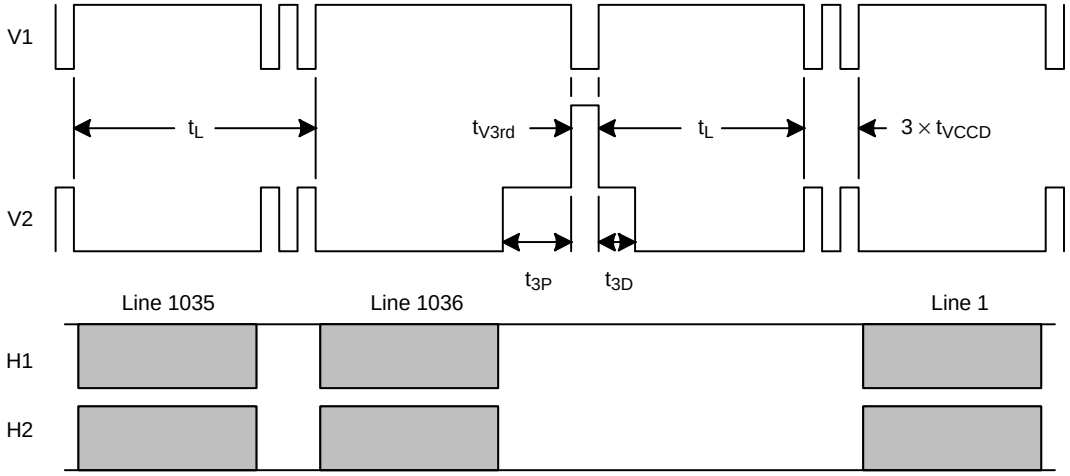


Figure 27. Frame Timing for Vertical Binning by 2

Frame Timing Non-Summed Interlaced Scan (Even)

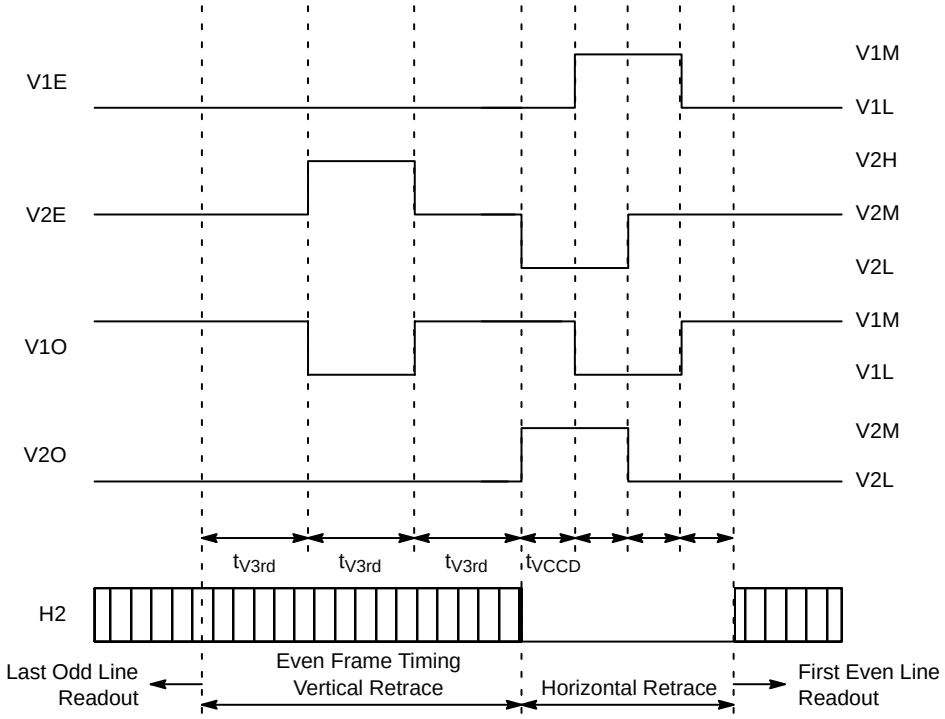


Figure 28. Non-Summed Interlaced Scan Even Frame Timing

Frame Timing Non-Summed Interlaced Scan (Odd)

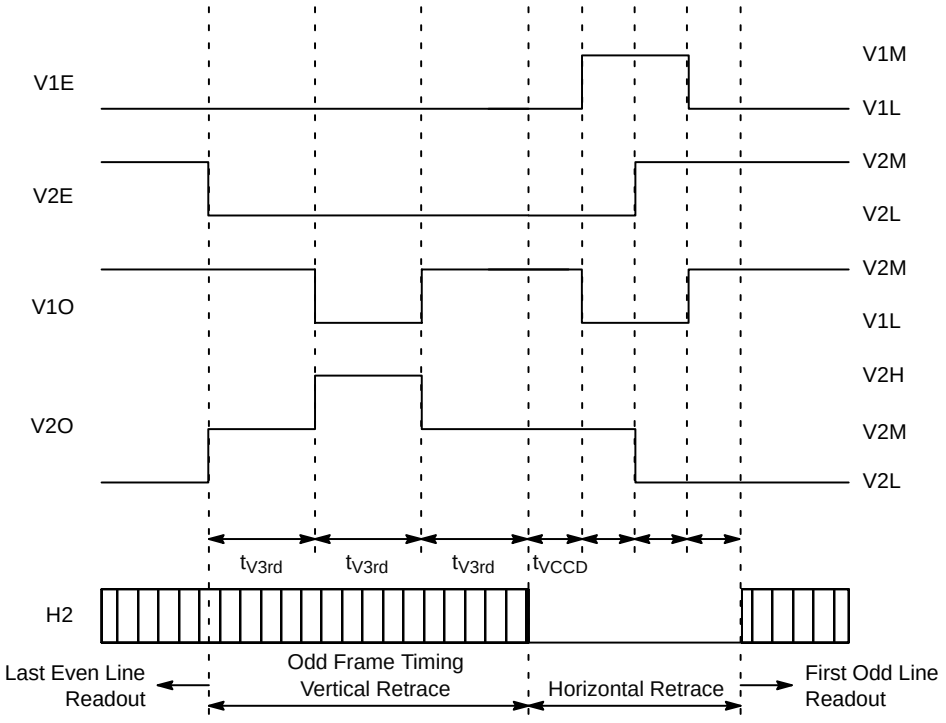


Figure 29. Non-Summed Interlaced Scan Odd Frame Timing

Frame Timing Summed Interlaced Scan (Even)

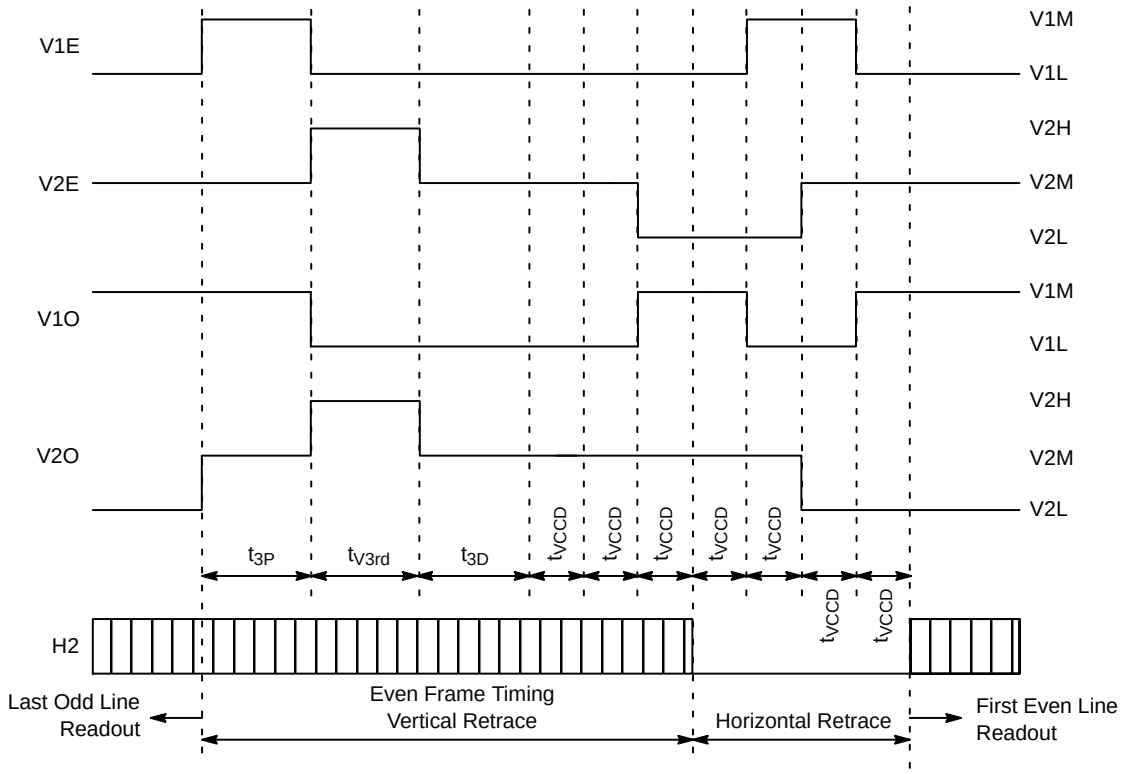


Figure 30. Summed Interlaced Scan Even Frame Timing

Frame Timing Summed Interlaced Scan (Odd)

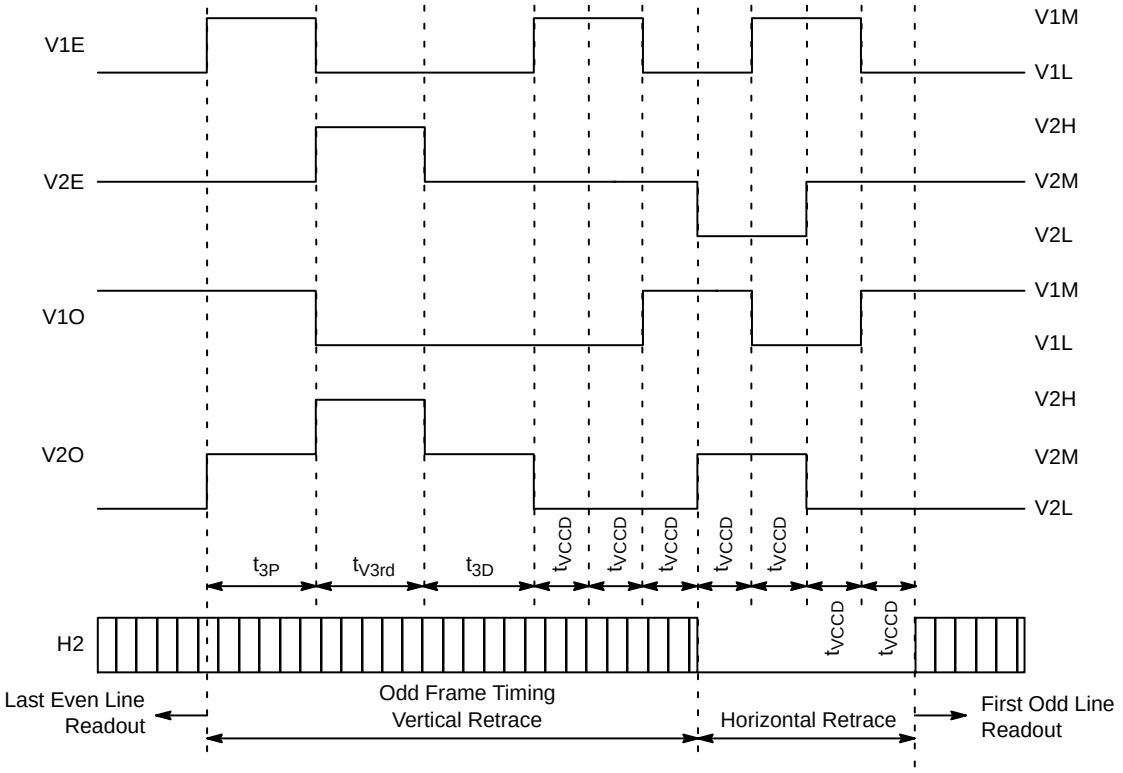


Figure 31. Summed Interlaced Scan Odd Frame Timing

Frame Timing Edge Alignment

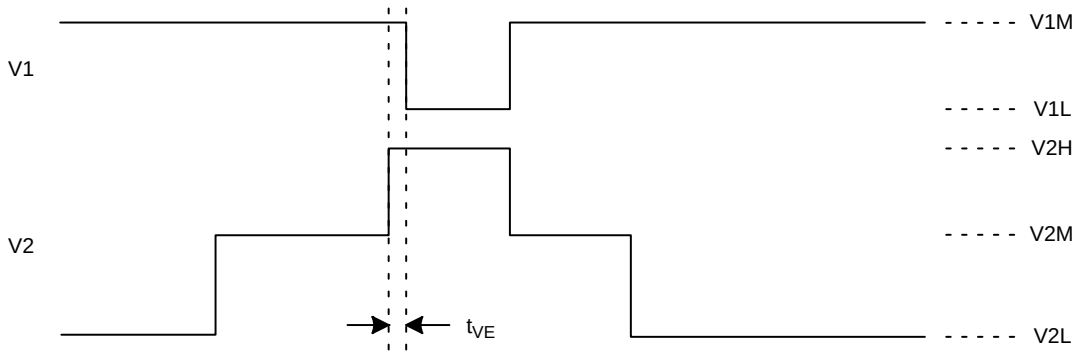


Figure 32. Frame Timing Edge Alignment

Line Timing

Line Timing Single Output − Progressive Scan

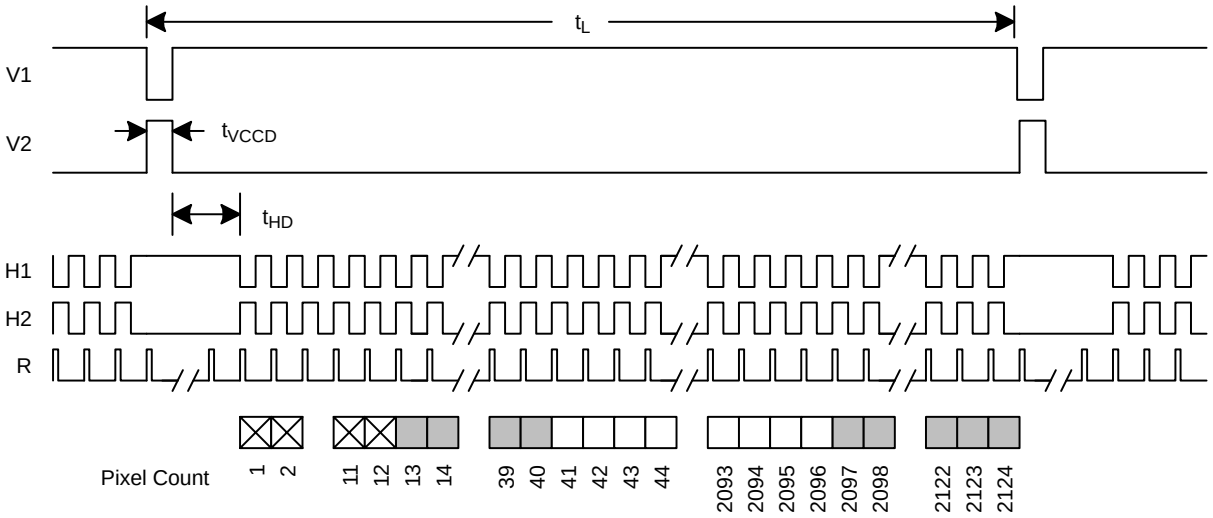


Figure 33. Line Timing Single Output

Line Timing Dual Output − Progressive Scan

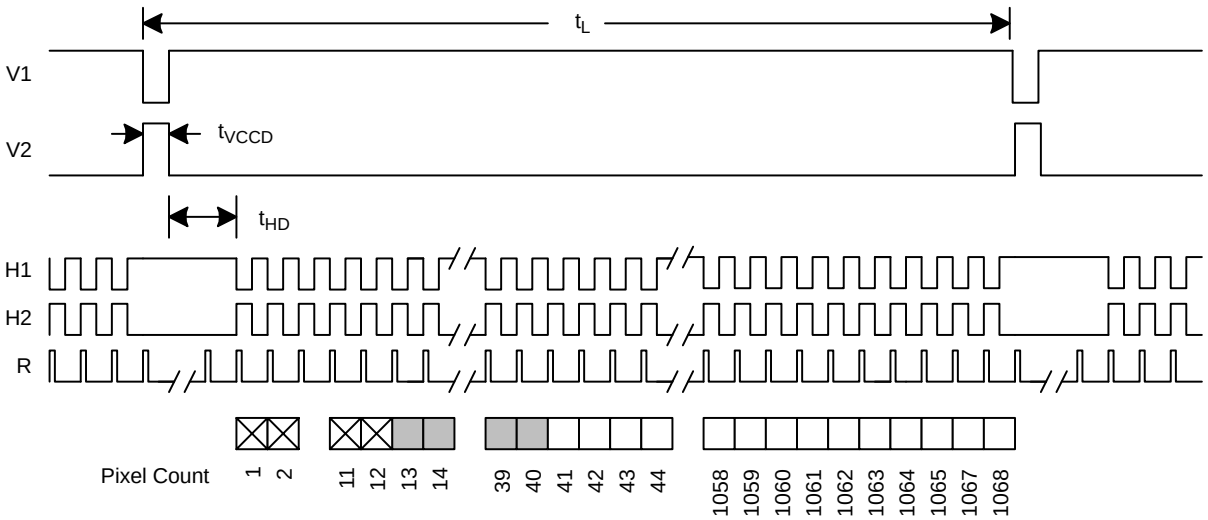


Figure 34. Line Timing Dual Output

Line Timing Vertical Binning by 2 − Progressive Scan

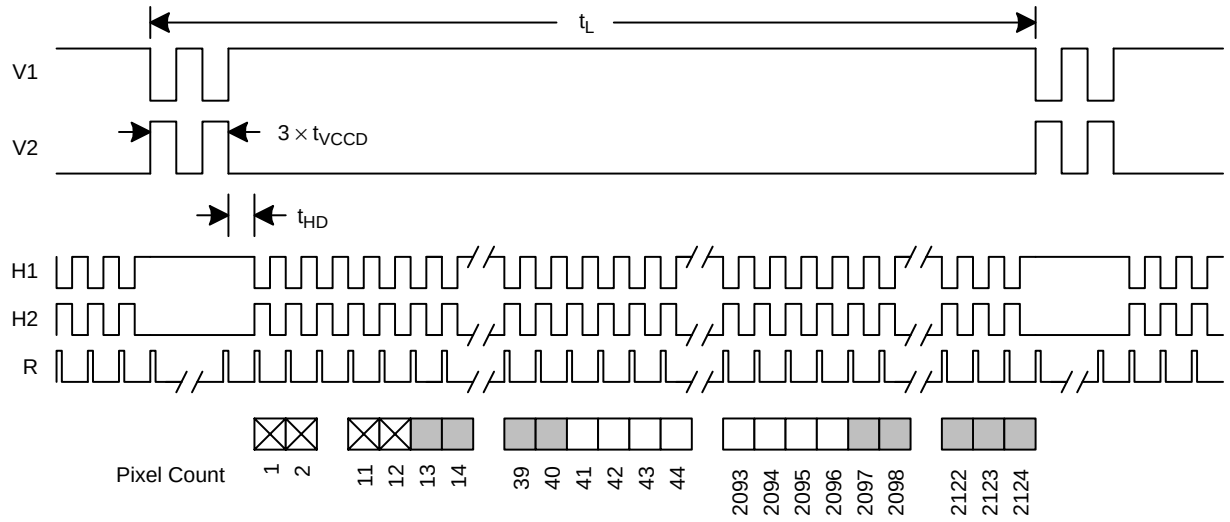


Figure 35. Line Timing Vertical Binning by 2

Line Timing Detail − Progressive Scan

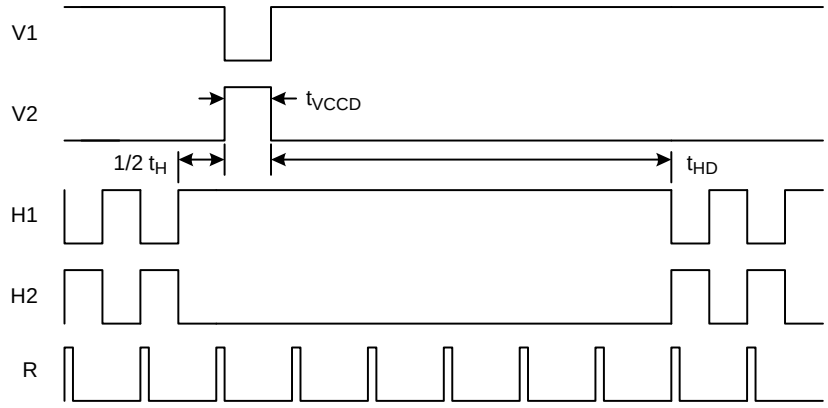


Figure 36. Line Timing Detail

Line Timing Binning by 2 Detail − Progressive Scan

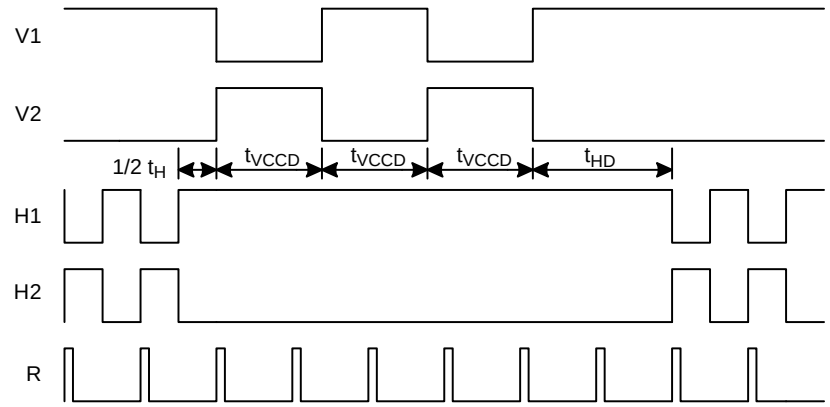


Figure 37. Line Timing by 2 Detail

Line Timing Binning Interlaced Modes

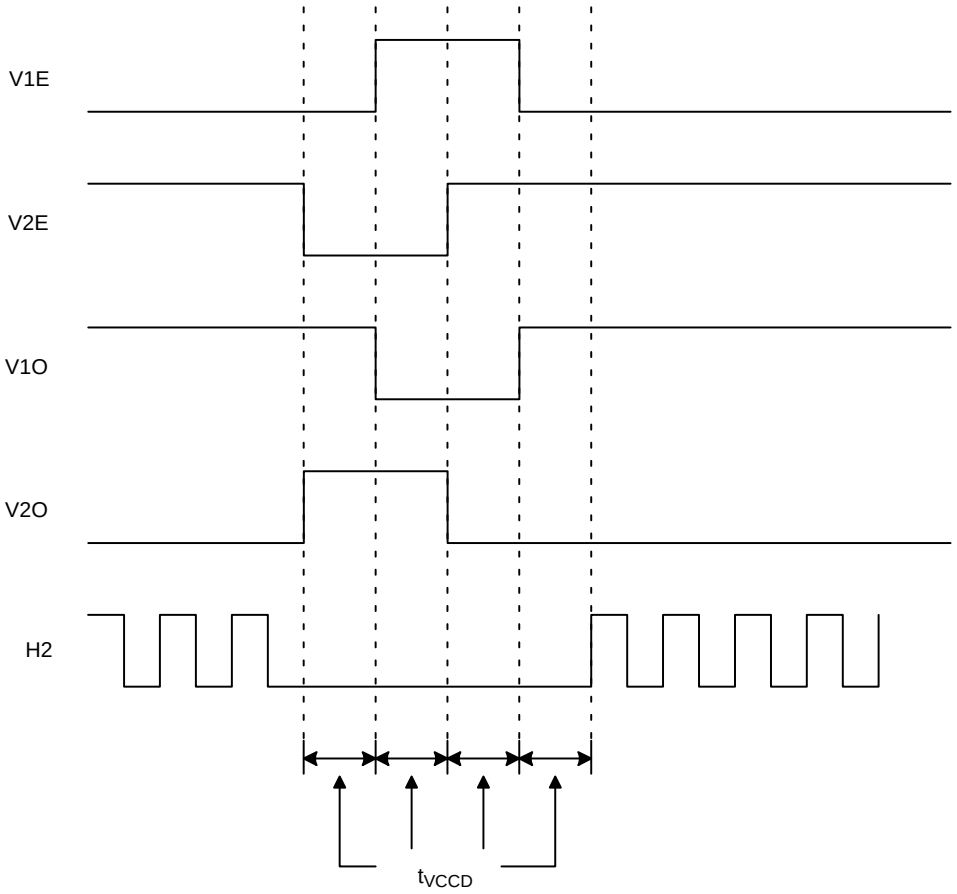


Figure 38. Line Timing Interlaced Modes

Line Timing Edge Alignment
Applies to all modes.

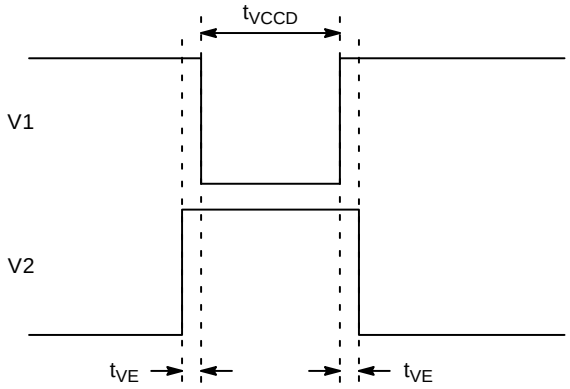


Figure 39. Line Timing Edge Alignment

Pixel Timing

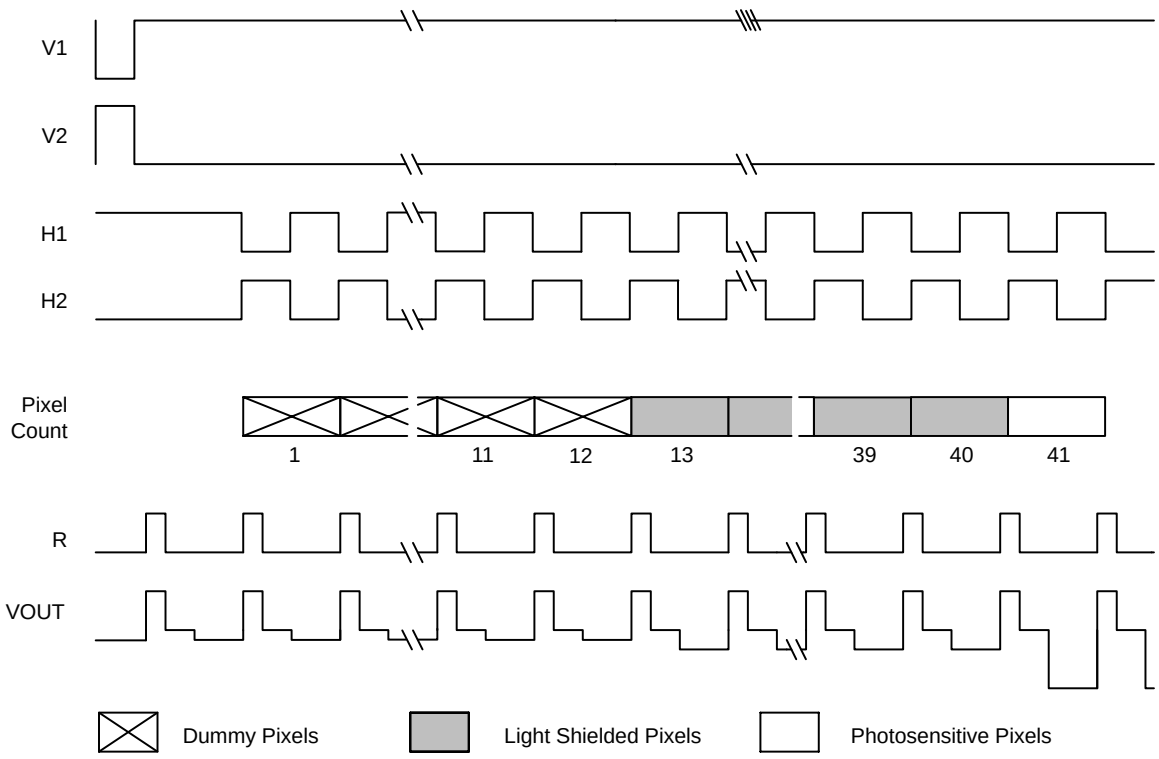


Figure 40. Pixel Timing

Pixel Timing Detail

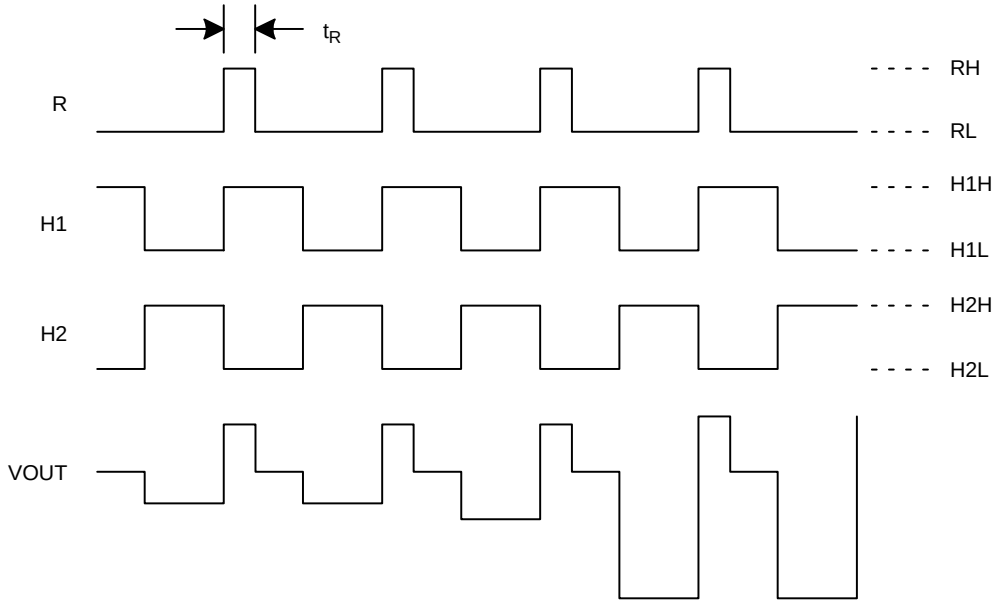


Figure 41. Pixel Timing Detail

Fast Line Dump Timing

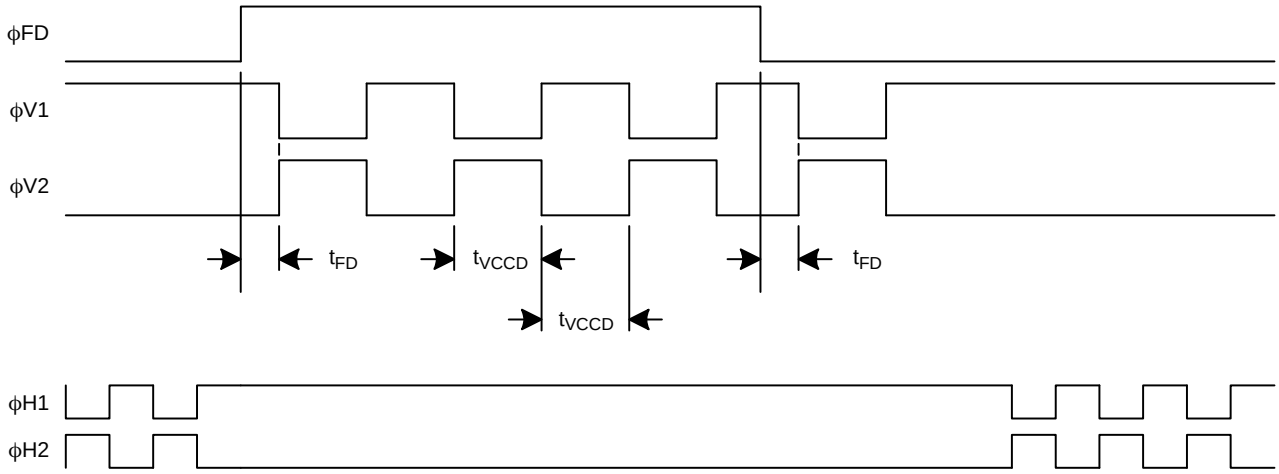


Figure 42. Fast Line Dump Timing

Electronic Shutter

Electronic Shutter Line Timing

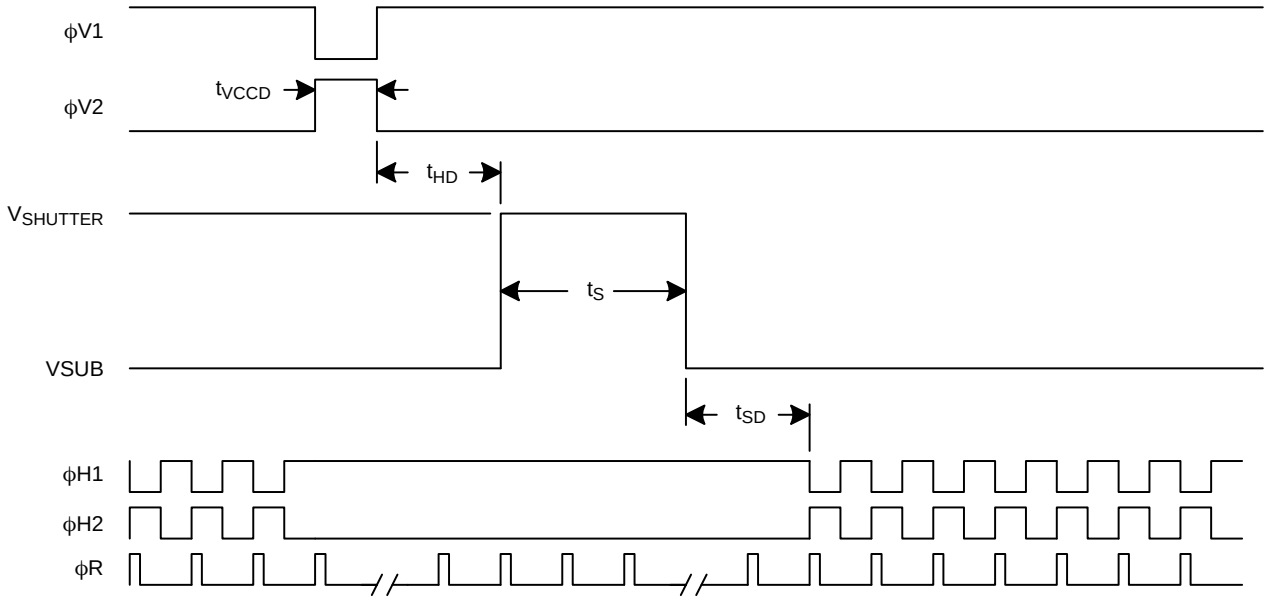


Figure 43. Electronic Shutter Line Timing

Electronic Shutter − Integration Time Definition

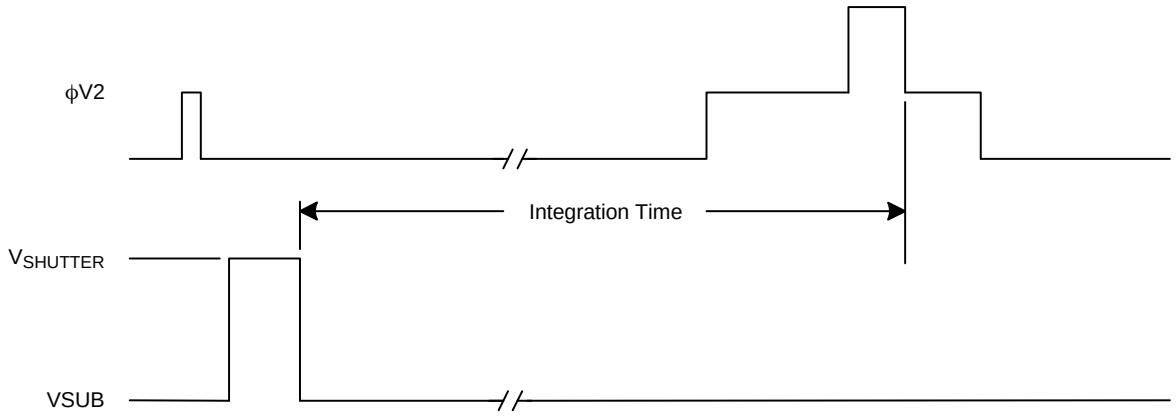


Figure 44. Integration Time Definition

Electronic Shutter − DC and AC Bias Definition

The figure below shows the DC bias (VSUB) and AC clock (VES) applied to the SUB pin. Both the DC bias and AC clock are referenced to ground.

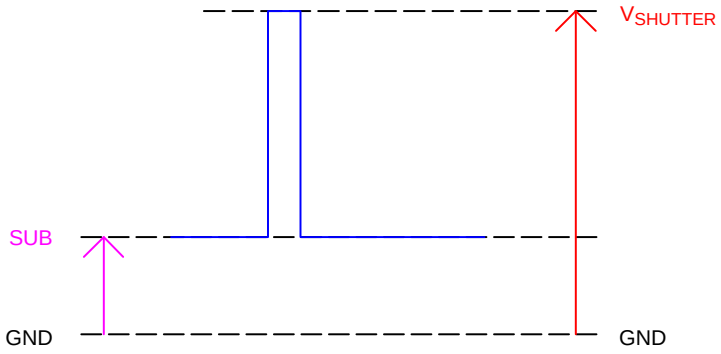


Figure 45. DC Bias and AC Clock Applied to the SUB Pin

Electronic Shutter Description

The voltage on the substrate (SUB) determines the charge capacity of the photodiodes. When SUB is 8 V the photodiodes will be at their maximum charge capacity. Increasing VSUB above 8 V decreases the charge capacity of the photodiodes until 48 V when the photodiodes have a charge capacity of zero electrons. Therefore, a short pulse on SUB, with a peak amplitude greater than 48 V, empties all photodiodes and provides the electronic shuttering action.

It may appear the optimal substrate voltage setting is 8 V to obtain the maximum charge capacity and dynamic range. While setting VSUB to 8 V will provide the maximum dynamic range, it will also provide the minimum anti-blooming protection.

The KAI−04022 VCCD has a charge capacity of 60,000 electrons (60 ke$^-$). If the SUB voltage is set such that the photodiode holds more than 60 ke$^-$, then when the charge is transferred from a full photodiode to VCCD, the VCCD will overflow. This overflow condition manifests itself in the image by making bright spots appear elongated in the vertical direction. The size increase of a bright spot is called blooming when the spot doubles in size. The blooming can be eliminated by increasing the voltage on SUB to lower the charge capacity of the photodiode. This ensures the VCCD charge capacity is greater than the photodiode capacity. There are cases where an extremely bright spot will still cause blooming in the VCCD. Normally, when the photodiode is full, any additional electrons generated by photons will spill out of the photodiode. The excess electrons are drained harmlessly out to the substrate. There is a maximum rate at which the electrons can be drained to the substrate. If that maximum rate is exceeded, (for example, by a very bright light source) then it is possible for the total amount of charge in the photodiode to exceed the VCCD capacity. This results in blooming. The amount of anti-blooming protection also decreases when the integration time is decreased. There is a compromise between photodiode dynamic range (controlled by VSUB) and the amount of anti-blooming protection. A low VSUB voltage provides the maximum dynamic range and minimum (or no) anti-blooming protection. A high VSUB voltage provides lower dynamic range and maximum anti-blooming protection. The optimal setting of VSUB is written on the container in which each KAI−04022 is shipped. The given VSUB voltage for each sensor is selected to provide anti-blooming protection for bright spots at least 100 times saturation, while maintaining at least 40 ke$^-$ of dynamic range.

The electronic shutter provides a method of precisely controlling the image exposure time without any mechanical components. If an integration time of t_{INT} is desired, then the substrate voltage of the sensor is pulsed to at least 40 V t_{INT} seconds before the photodiode to VCCD transfer pulse on V2. Use of the electronic shutter does not have to wait until the previously acquired image has been completely read out of the VCCD.

Large Signal Output

When the image sensor is operated in the binned or summed interlaced modes there will be more than 20,000 electrons in the output signal. The image sensor is designed with a 31 μV/e charge to voltage conversion on the output. This means a full signal of 20,000 electrons will produce a 640 mV change on the output amplifier. The output amplifier was designed to handle an output swing of 640 mV at a pixel rate of 40 MHz. If 40,000 electron charge packets are generated in the binned or summed interlaced modes then the output amplifier output will have to swing 1,280 mV. The output amplifier does not have enough bandwidth (slew rate) to handle 1,280 mV at 40 MHz. Hence, the pixel rate will have to be reduced to 20 MHz if the full dynamic range of 40,000 electrons is desired.

The charge handling capacity of the output amplifier is also set by the reset clock voltage levels. The reset clock driver circuit is very simple if an amplitude of 5 V is used. But the 5 V amplitude restricts the output amplifier charge capacity to 20,000 electrons. If the full dynamic range of 40,000 electrons is desired then the reset clock amplitude will have to be increased to 7 V.

If you only want a maximum signal of 20,000 electrons in binned or summed interlaced modes, then a 40 MHz pixel rate with a 5 V reset clock may be used. The output of the amplifier will be unpredictable above 20,000 electrons so be sure to set the maximum input signal level of your analog to digital converter to the equivalent of 20,000 electrons (640 mV).

REFERENCES

For information on ESD and cover glass care and cleanliness, please download the *Image Sensor Handling and Best Practices* Application Note (AN52561/D) from www.onsemi.com.

For information on environmental exposure, please download the *Using Interline CCD Image Sensors in High Intensity Lighting Conditions* Application Note (AND9183/D) from www.onsemi.com.

For information on soldering recommendations, please download the Soldering and Mounting Techniques Reference Manual (SOLDERRM/D) from www.onsemi.com.

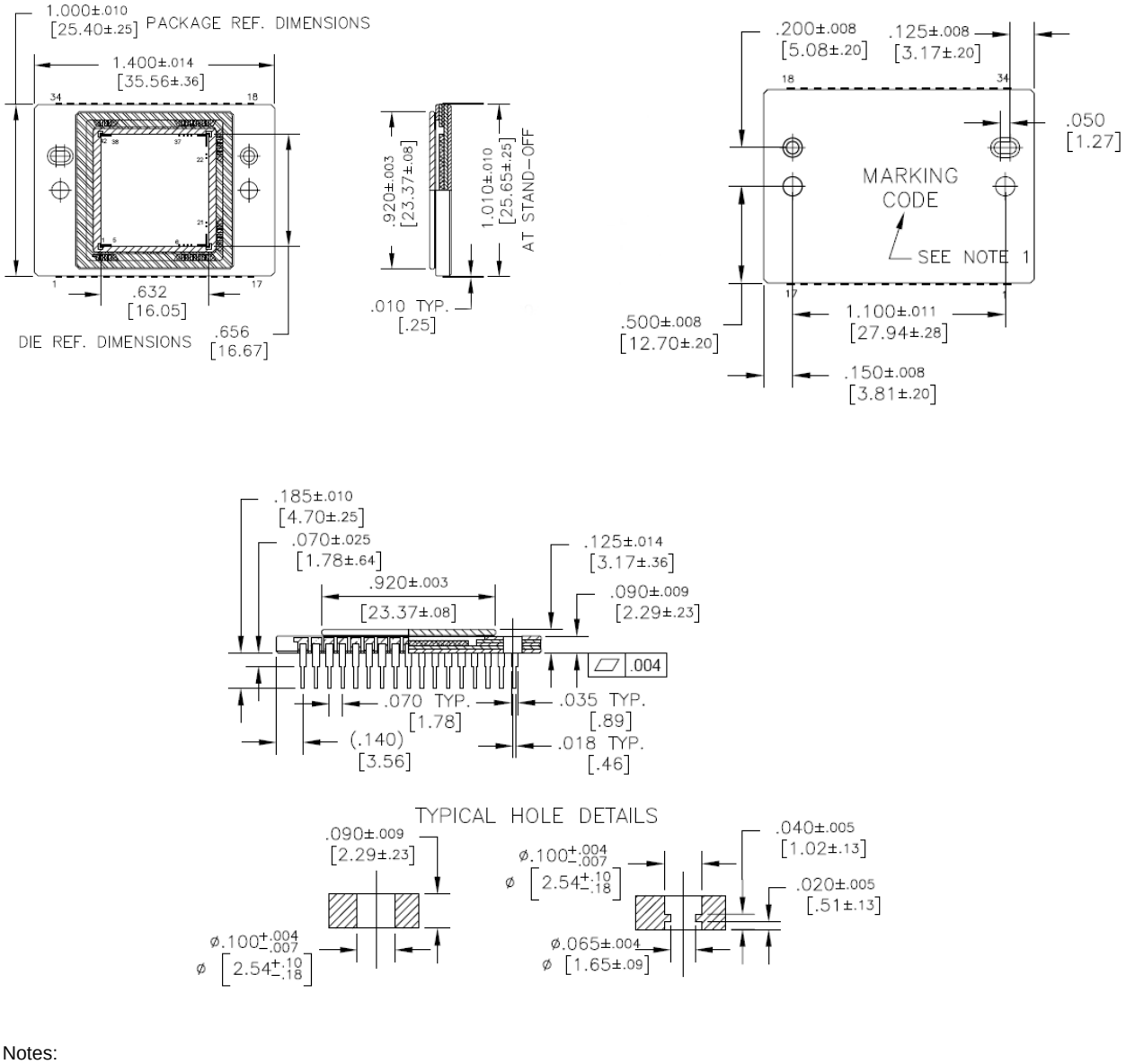
For quality and reliability information, please download the *Quality & Reliability* Handbook (HBD851/D) from www.onsemi.com.

For information on device numbering and ordering codes, please download the *Device Nomenclature* technical note (TND310/D) from www.onsemi.com.

For information on Standard terms and Conditions of Sale, please download Terms and Conditions from www.onsemi.com.

MECHANICAL INFORMATION

Completed Assembly



Notes:
1. See Ordering Information for marking code.
2. The Cover Glass is manually placed and aligned.

Figure 46. Completed Assembly

Die to Package Alignment

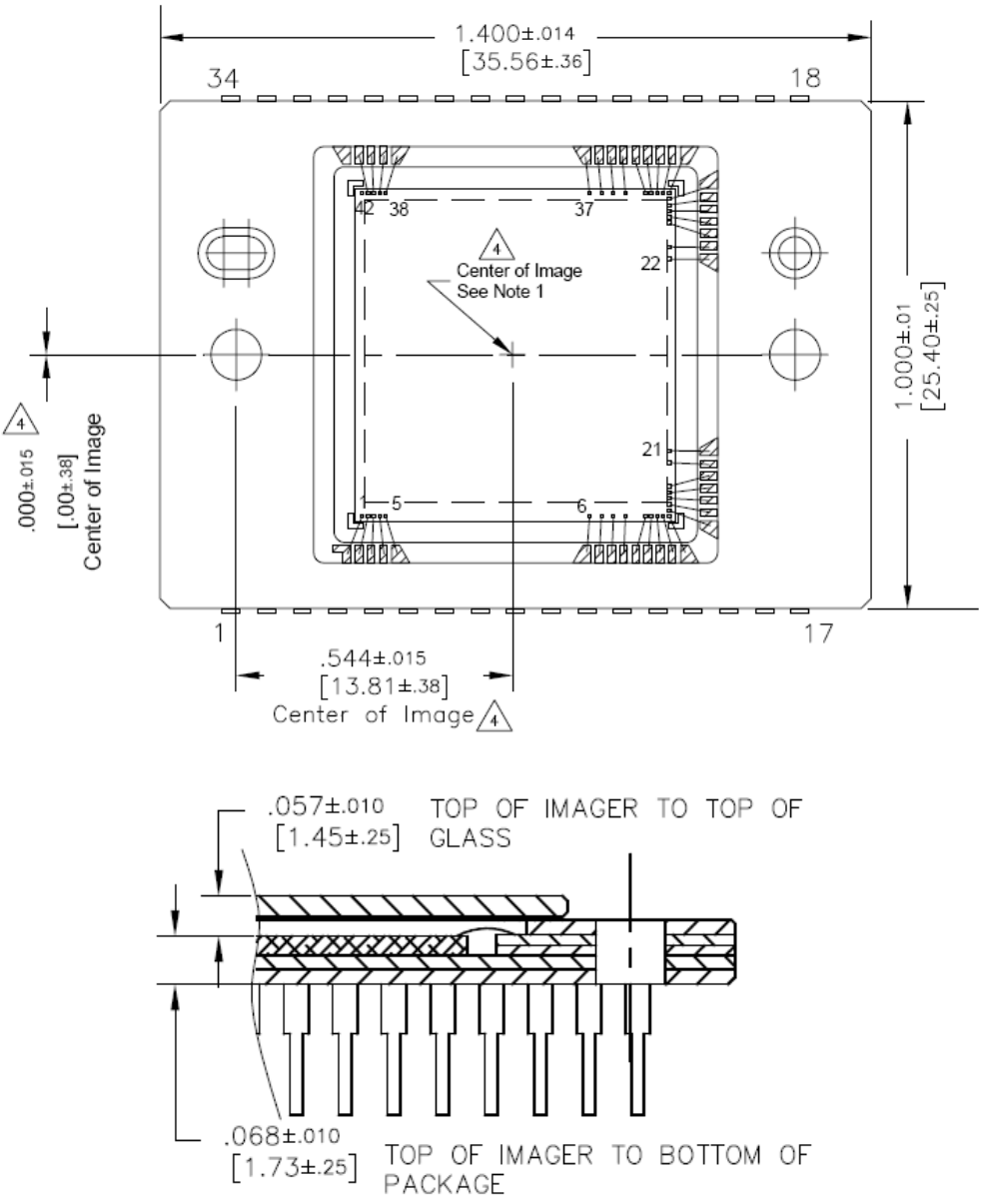
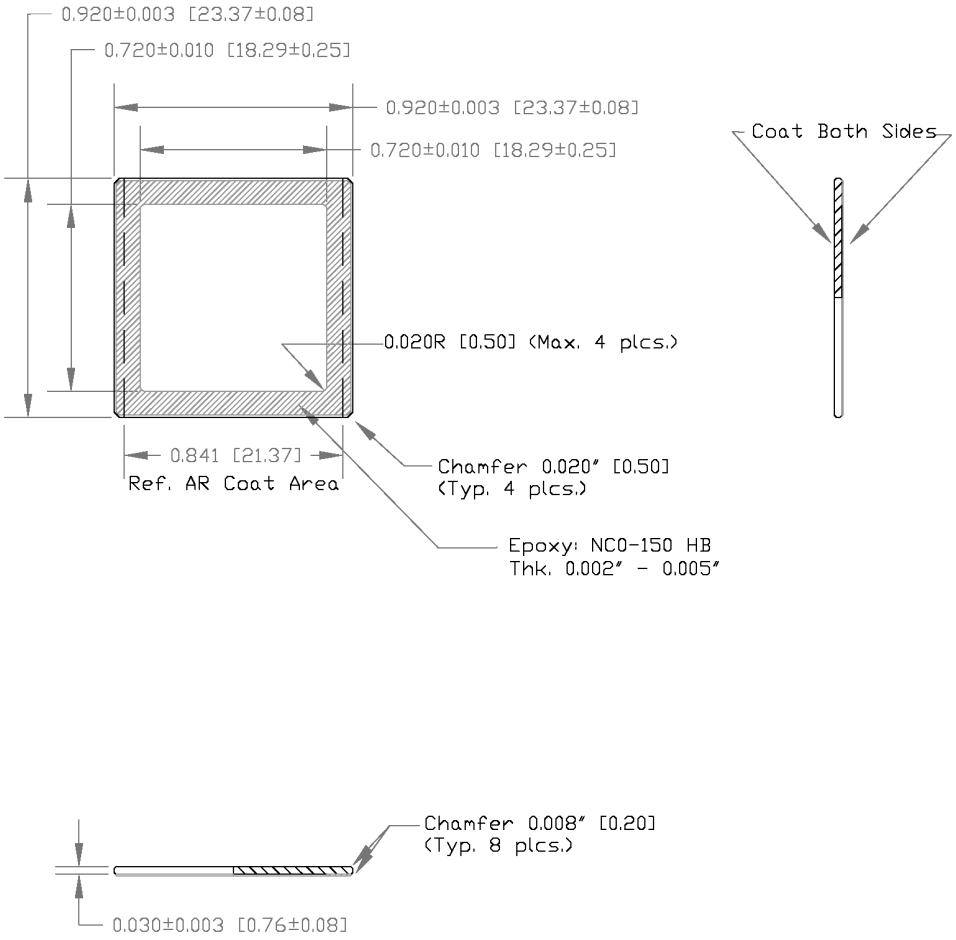


Figure 47. Die to Package Alignment

Glass



Notes:

1. Multi-layer anti-reflective coating on 2 sides:
   a. Double sided reflectance
   b. Range (nm):
      i. 420−435 nm < 2.0%
      ii. 435−630 nm < 0.8%
      iii. 630−680 nm < 2.0%
2. Dust, Scratch specification: 10 μm maximum.
3. Substrate − Schott D263T eco or equivalent.
4. Epoxy: NCO−150HB
   a. Thickness: 0.002−0.005″
5. Dimensions
   a. Units: Inch [mm]
6. Tolerance, unless otherwise specified:
   a. Ceramic: ±1% no less than 0.004″
   b. L/F: ±1% no more than 0.004″

Figure 48. Glass Drawing

Glass Transmission

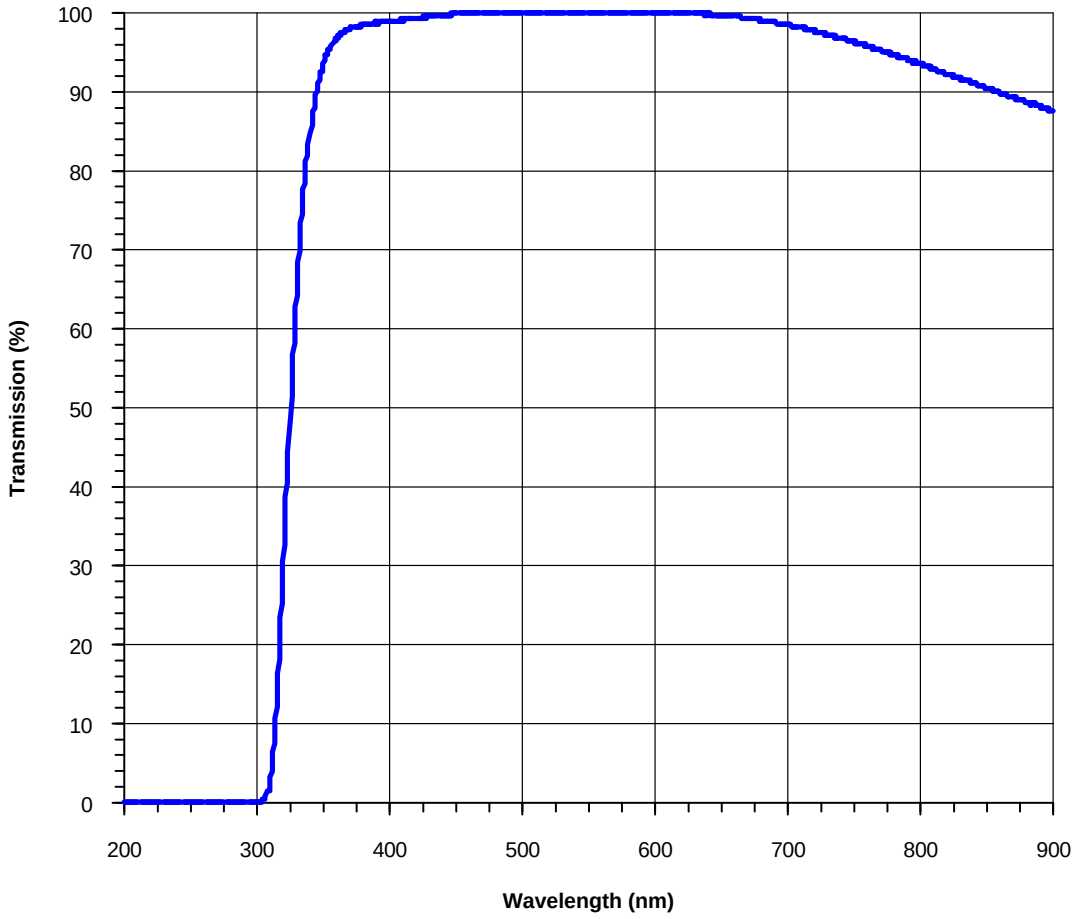


Figure 49. Glass Transmission

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