

## PROTECTION PRODUCTS

### Description

The LCDAxxC-8 has been specifically designed to protect sensitive components which are connected to data and transmission lines from over voltages caused by **ESD** (electrostatic discharge), **EFT** (electrical fast transients), and **lightning**.

The low capacitance array configuration of the LCDAxxC-8 allows the user to protect eight high-speed data or I/O lines. They may be used on systems operating from 5 to 15 Volts. The high surge capability (500W,  $t_p=8/20\mu s$ ) makes the LCDAxxC-8 suitable for telecommunications systems operating in harsh transient environments. The low inductance construction minimizes voltage overshoot during high current surges.

The features of the LCDAxxC-8 are ideal for protecting multi-protocol transceivers in WAN applications such as Frame Relay systems, routers, and switches.

### Features

- ◆ Transient protection for high-speed data lines to **IEC 61000-4-2 (ESD) 15kV (air), 8kV (contact)**  
**IEC 61000-4-4 (EFT) 40A (5/50ns)**  
**IEC 61000-4-5 (Lightning) 0.5kV, 12A (8/20 $\mu s$ )**
- ◆ Protects eight I/O lines
- ◆ Low capacitance for high-speed interfaces
- ◆ High surge capability
- ◆ Low clamping voltage
- ◆ Solid-state silicon avalanche technology

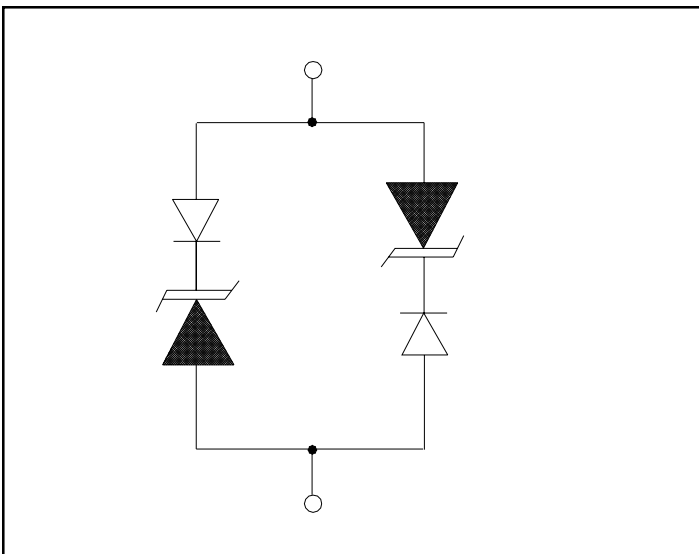
### Mechanical Characteristics

- ◆ JEDEC SO-16 package
- ◆ Molding compound flammability rating: UL 94V-0
- ◆ Marking : Part number, date code, logo
- ◆ Packaging : Tape and Reel per EIA 481

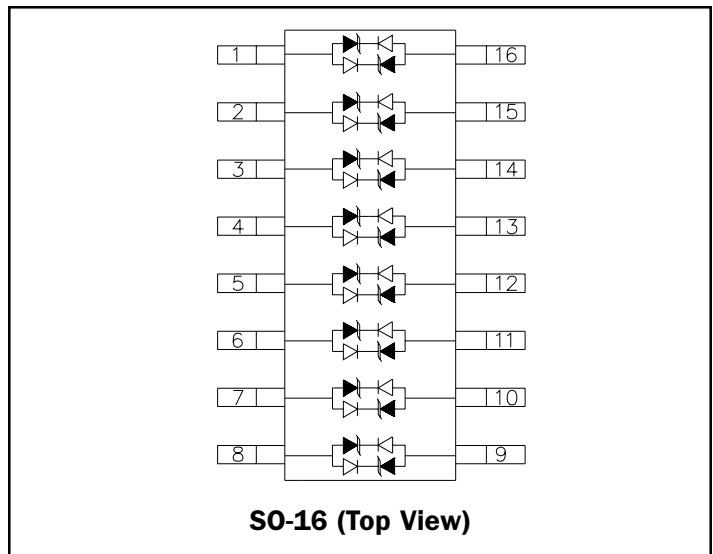
### Applications

- ◆ Multi-Mode Transceiver Protection
- ◆ WAN Equipment:
  - CSU/DSU
  - Multiplexers
  - Routers
  - ISP Equipment
  - Customer Premise Equipment
- ◆ Protection for any of the following interfaces:
  - RS-232 (V.28)
  - RS-422 (V.11, X.21)
  - RS-449 (V.11/V.10)

### Circuit Diagram



### Schematic & PIN Configuration



**PROTECTION PRODUCTS**
**Absolute Maximum Rating**

Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20μs)	$P_{pk}$	500	Watts
Peak Pulse Current (tp = 8/20μs)	$I_{pp}$	20	A
Lead Soldering Temperature	$T_L$	260 (10 sec.)	°C
Operating Temperature	$T_J$	-55 to +125	°C
Storage Temperature	$T_{STG}$	-55 to +150	°C

**Electrical Characteristics**

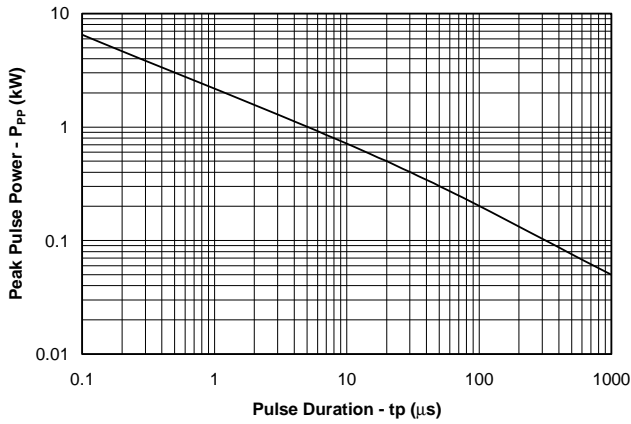
<b>LCDA12C-8</b>						
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	$V_{RWM}$				12	V
Reverse Breakdown Voltage	$V_{BR}$	$I_t = 1mA$	13.3			V
Reverse Leakage Current	$I_R$	$V_{RWM} = 12V, T=25^\circ C$			5	μA
Clamping Voltage	$V_C$	$I_{pp} = 5A, tp = 8/20\mu s$			19	V
Clamping Voltage	$V_C$	$I_{pp} = 20A, tp = 8/20\mu s$			26.6	V
Junction Capacitance	$C_J$	Between I/O pins & Gnd $V_R = 0V, f = 1MHz$		8	15	pF

<b>LCDA15C-8</b>						
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	$V_{RWM}$				15	V
Reverse Breakdown Voltage	$V_{BR}$	$I_t = 1mA$	16.7			V
Reverse Leakage Current	$I_R$	$V_{RWM} = 15V, T=25^\circ C$			5	μA
Clamping Voltage	$V_C$	$I_{pp} = 1A, tp = 8/20\mu s$			24	V
Clamping Voltage	$V_C$	$I_{pp} = 15A, tp = 8/20\mu s$			33	V
Junction Capacitance	$C_J$	Between I/O pins & Gnd $V_R = 0V, f = 1MHz$		8	15	pF

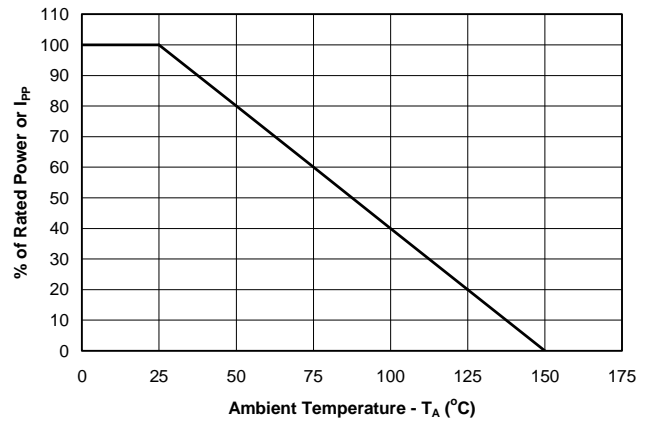
## PROTECTION PRODUCTS

### Typical Characteristics

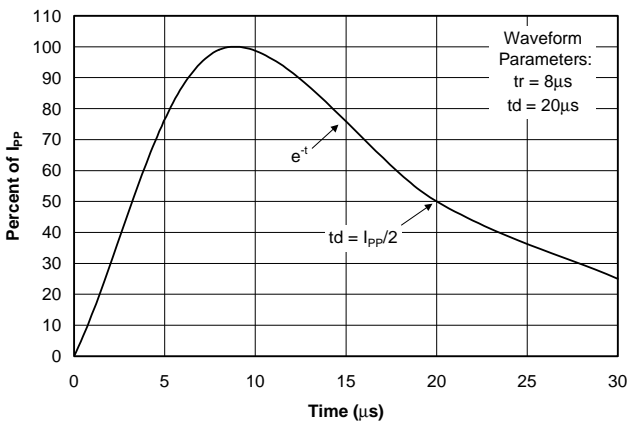
**Non-Repetitive Peak Pulse Power vs. Pulse Time**



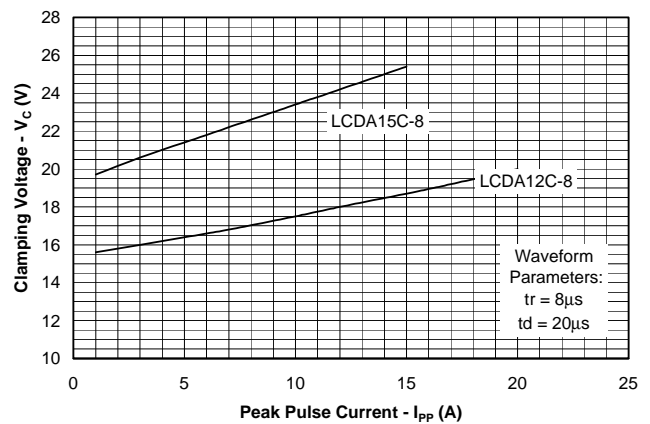
**Power Derating Curve**



**Pulse Waveform**



**Clamping Voltage vs. Peak Pulse Current**



## PROTECTION PRODUCTS

### Applications Information

#### Device Connection Options for Protection of Eight High-Speed Data Lines

The LCDAxxC-8 may be configured to protect up to eight I/O lines operating between 5 and 15V. It may be used to protect the most popular serial data interface standard lines making it ideal for use in equipment utilizing multi-mode transceivers. The LCDAxxC-8 is symmetrical so the data lines may be connected at pins 1-8 or 9-16. Pins 9-16 or 1-8 are connected to ground as shown. For best results, these pins should be connected directly to a ground plane on the board. The path length should be kept as short as possible to minimize parasitic inductance.

#### Multi-Mode Transceiver Protection

The LCDAxxC-8 may be used to protect multi-mode transceiver I/O lines with external connections. The LCDAxxC-8 adds a maximum loading capacitance of 15pF with a working voltage of 12V or 15V. This allows the transceiver to safely operate in all modes without clipping or degradation of the signal.

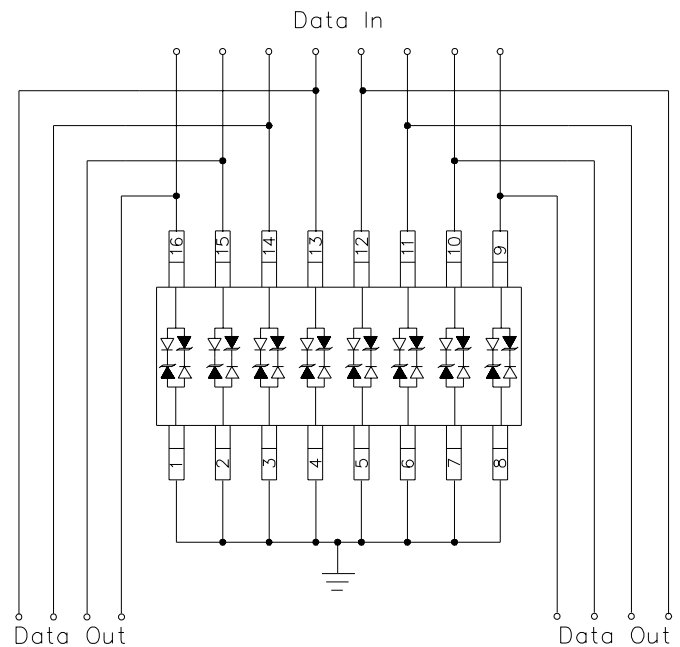
With proper design and layout, the transceiver port can be protected to >15kV (HBM per IEC 61000-4-2).

#### Circuit Board Layout Recommendations for Suppression of ESD.

Good circuit board layout is critical for the suppression of fast rise-time transients such as ESD. The following guidelines are recommended:

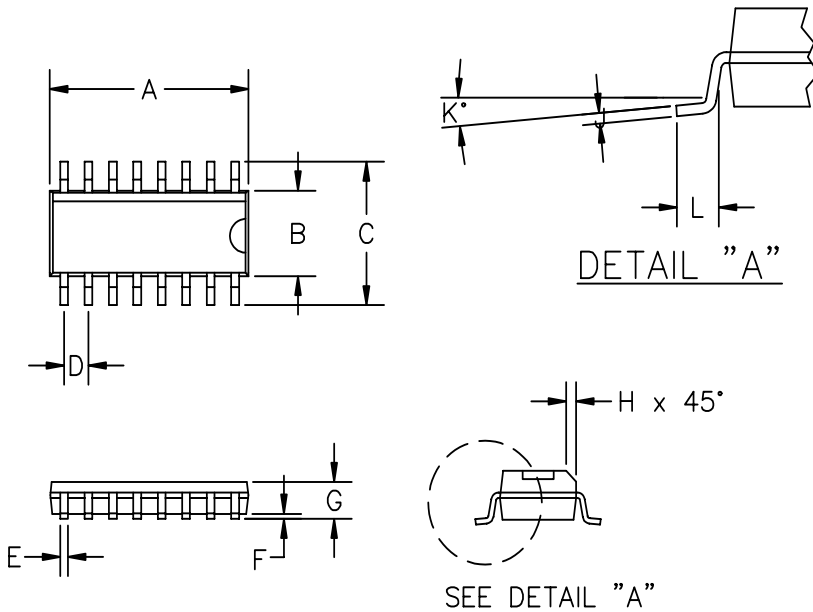
- Place the LCDAxxC-8 near the input terminals or connectors to restrict transient coupling.
- Minimize the path length between the LCDAxxC-8 and the protected line.
- Minimize all conductive loops including power and ground loops.
- The ESD transient return path to ground should be kept as short as possible.
- Never run critical signals near board edges.
- Use ground planes whenever possible.

#### Device Connection



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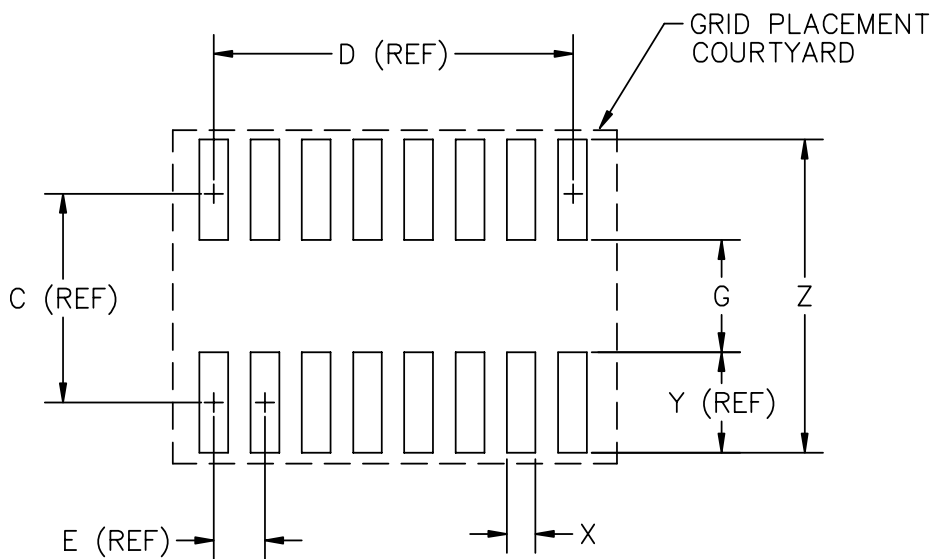
### Outline Drawing - SO-16



DIM <sup>N</sup>	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.386	.393	9.80	10.0	②
B	.150	.158	3.80	4.00	②
C	.228	.244	5.80	6.20	—
D	.050	BSC	1.27	BSC	—
E	.013	.020	0.33	0.51	—
F	.004	.010	.10	.25	—
G	.053	.069	1.35	1.75	—
H	.010	.020	.25	.50	—
J	.007	.010	.19	.25	—
K	0°	8°	0°	8°	—
L	.016	.050	.40	1.27	—

② DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTUSIONS

### Land Pattern - SO-16



DIM <sup>N</sup>	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
C	—	.197	—	5.00	—
D	—	.35	—	8.89	—
E	—	.05	—	1.27	—
G	.102	.110	2.60	2.80	—
X	.02	.03	.60	.80	—
Y	—	.095	—	2.40	—
Z	.28	.29	7.20	7.40	—

① GRID PLACEMENT COURTYARD IS 22 X 16 ELEMENTS (11mm X 8mm) IN ACCORDANCE WITH THE INTERNATIONAL GRID DETAILED IN IEC PUBLICATION 97.

**PROTECTION PRODUCTS****Ordering Information**

<b>Part Number</b>	<b>Working Voltage</b>	<b>Qty per Reel</b>	<b>Reel Size</b>
LCDA12C-8.TE	12V	2,500	13 Inch
LCDA15C-8.TE	15V	2,500	13 Inch

Note:

(1) No suffix indicates tube pack.

**Contact Information**

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