LH168A

384-output TFT-LCD Source Driver IC

DESCRIPTION

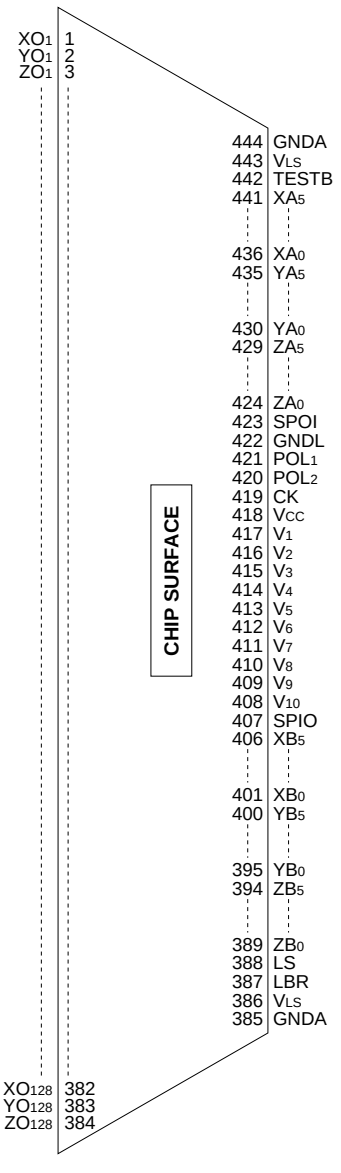
The LH168A is a 384-output TFT-LCD source driver IC which can simultaneously display 262 144 colors in 64 gray scales.

FEATURES

- Number of LCD drive outputs : 384
- Built-in 6-bit digital input DAC
- 2-port input for each circuit of data inputs R, G and B, and it is possible to sample and hold display data of two pixels at the same time
- Possible to display 262 144 colors in 64 gray scales with reference voltage input of 10 gray scales : This reference voltage input corresponds to γ correction and intermediate reference voltage input can be abbreviated
- Cascade connection
- Sampling sequence :
  Output shift direction can be selected
  XO_1, YO_1, $ZO_1 \rightarrow XO_{128}$, YO_{128}, ZO_{128} or
  ZO_{128}, YO_{128}, $XO_{128} \rightarrow ZO_1$, YO_1, XO_1
- Shift clock frequency : 55 MHz (MAX.)
- Supply voltages
  – V_{CC} (for logic system) : +2.7 to +3.6 V
  – V_{LS} (for LCD drive system) : +3.0 to +5.5 V
- Package : 444-pin TCP (Tape Carrier Package)

PIN CONNECTIONS

444-PIN TCP TOP VIEW

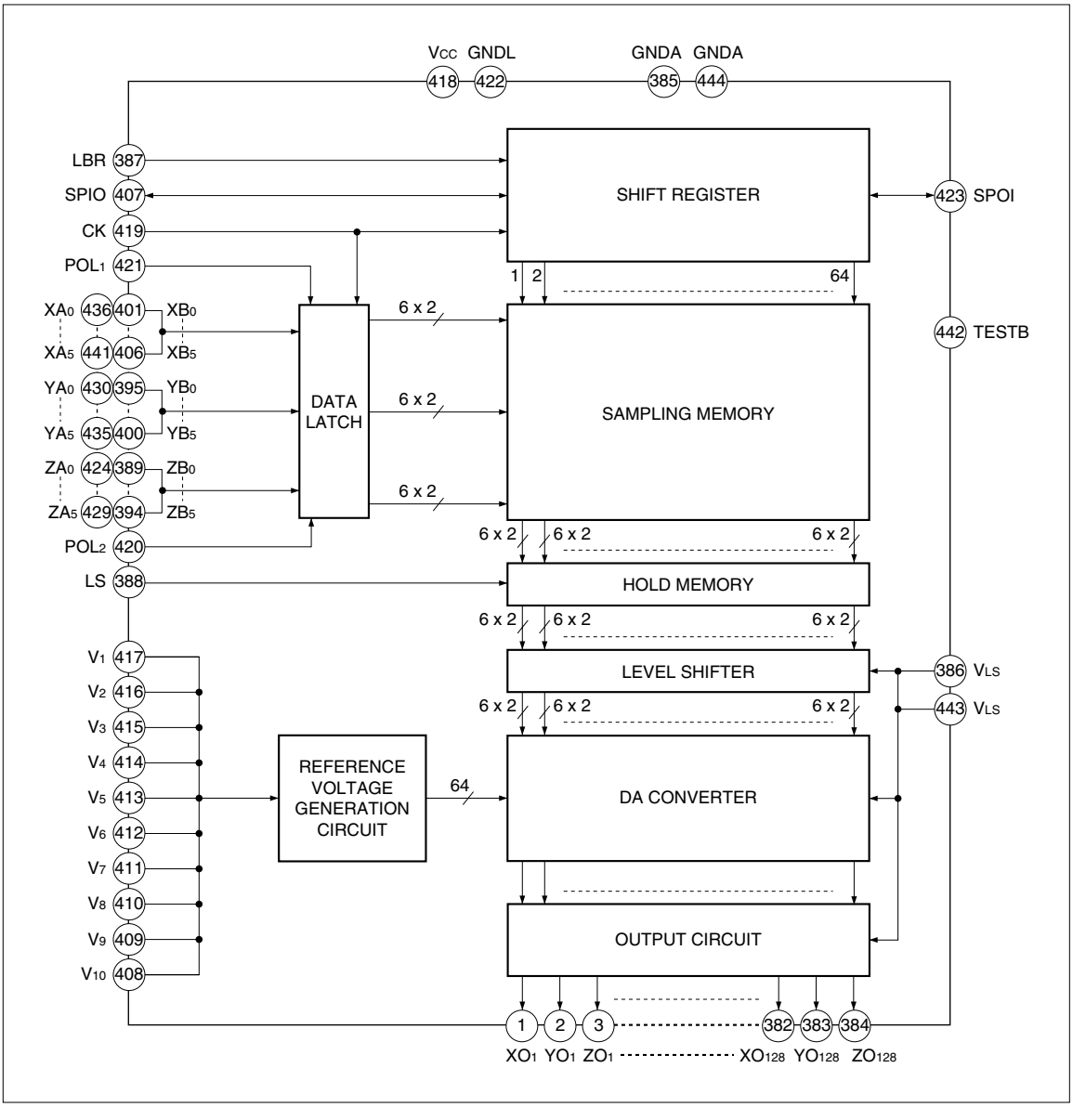


NOTE :
Doesn't prescribe TCP outline.

PIN DESCRIPTION

PIN NO.	SYMBOL	I/O	DESCRIPTION
1 to 384	XO_1-ZO_{128}	O	LCD drive output pins
385, 444	GNDA	–	Ground pins for analog circuit
386, 443	V_{LS}	–	Power supply pins for analog circuit
387	LBR	I	Shift direction selection input pin
388	LS	I	Latch input pin
389 to 394	ZB_0-ZB_5	I	Data input pins
395 to 400	YB_0-YB_5	I	Data input pins
401 to 406	XB_0-XB_5	I	Data input pins
407	SPIO	I/O	Start pulse input/cascade output pin
408 to 417	V_{10}-V_1	I	Reference voltage input pins
418	V_{CC}	–	Power supply pin for digital circuit
419	CK	I	Shift clock input pin
420, 421	POL_2, POL_1	I	Input data polarity exchange input pins
422	GNDL	–	Ground pin for digital circuit
423	SPOI	I/O	Start pulse input/cascade output pin
424 to 429	ZA_0-ZA_5	I	Data input pins
430 to 435	YA_0-YA_5	I	Data input pins
436 to 441	XA_0-XA_5	I	Data input pins
442	TESTB	I	IC test pin

BLOCK DIAGRAM



FUNCTIONAL OPERATIONS OF EACH BLOCK

BLOCK	FUNCTION
Shift Register	Used as a bi-directional shift register which performs the shifting operation by CK and selects bits for data sampling.
Data Latch	Used to temporary latch the input data which is sent to the sampling memory.
Sampling Memory	Used to sample the data to be entered by time sharing.
Hold Memory	Used for temporary latch processing of data in the sampling memory by LS input.
Level Shifter	Used to shift the data in the hold memory to the power supply level of the analog circuit unit and sends the shifted data to DA converter.
Reference Voltage Generation Circuit	Used to generate a gamma-corrected 64-level voltage by the resistor dividing circuit.
DA Converter	Used to generate an analog signal according to the display data and sends the signal to the output circuit.
Output Circuit	Used as a voltage follower, configured with an operational amplifier and an output buffer, which outputs analog signals of 64 gray scales to LCD drive output pin.

INPUT/OUTPUT CIRCUITS

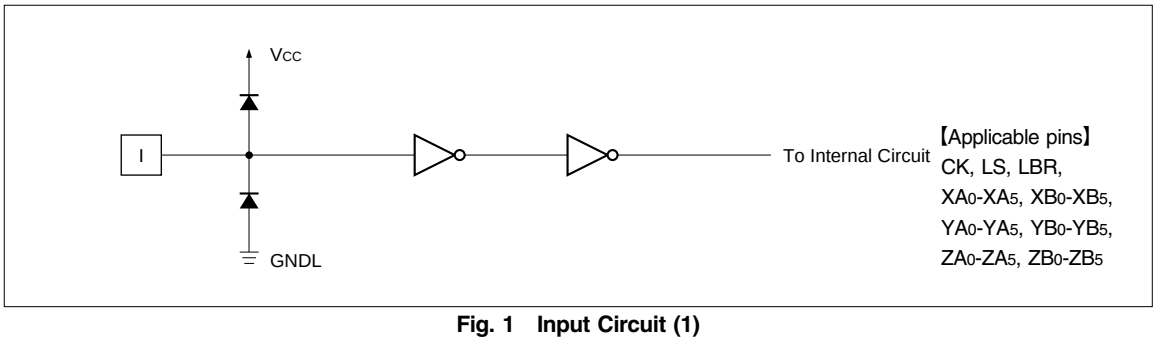


Fig. 1 Input Circuit (1)

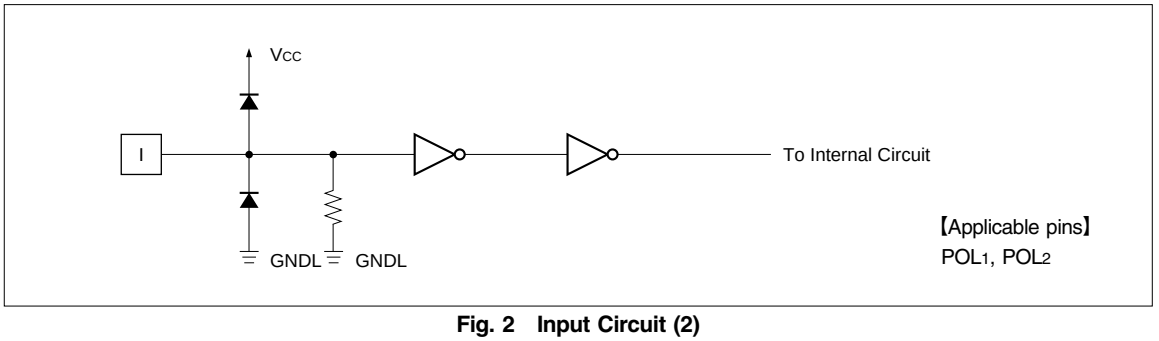


Fig. 2 Input Circuit (2)

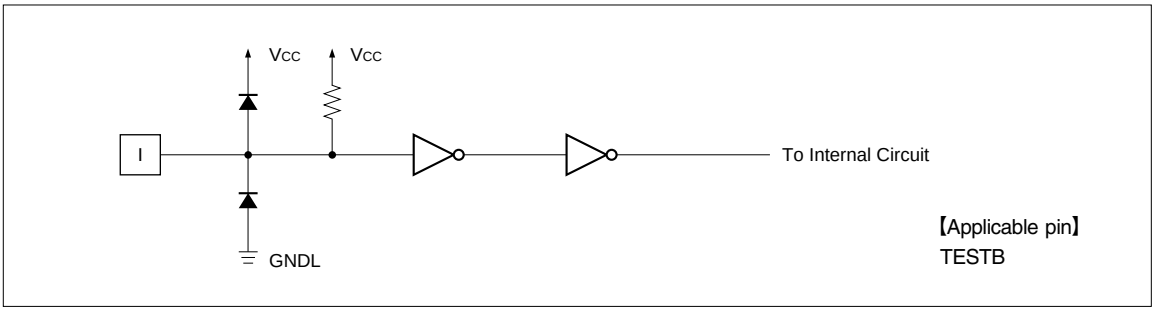


Fig. 3 Input Circuit (3)

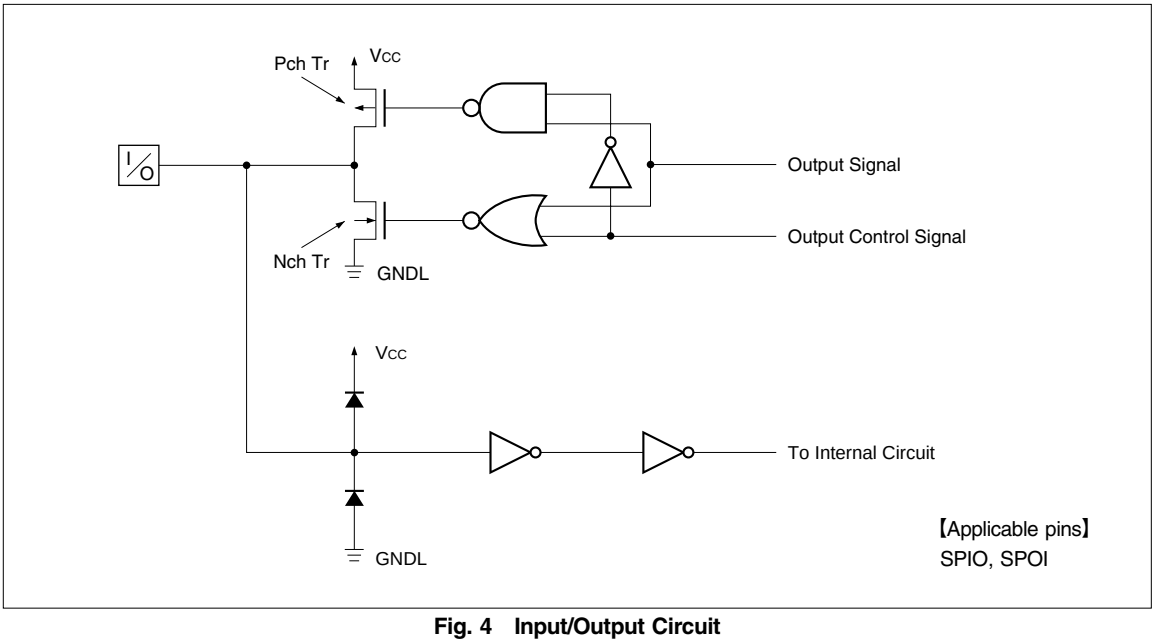


Fig. 4 Input/Output Circuit

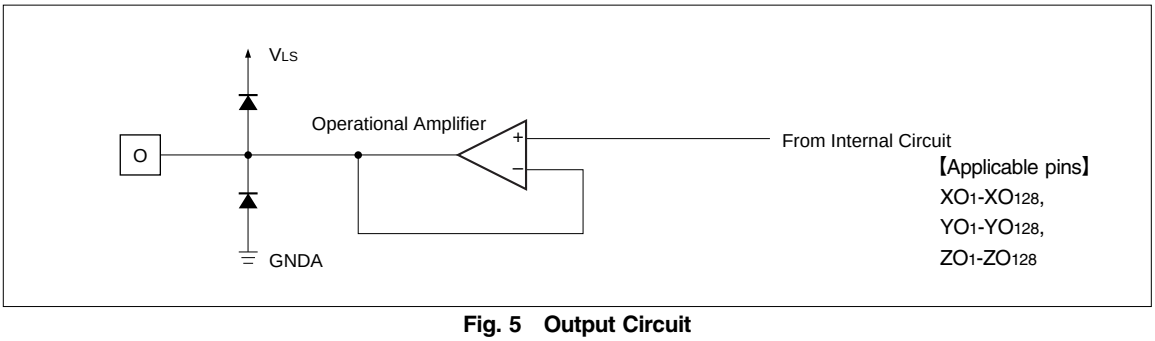


Fig. 5 Output Circuit

FUNCTIONAL DESCRIPTION

Pin Functions

SYMBOL	FUNCTIONS
V_{CC}	Used as power supply pin for digital circuit, connected to +2.7 to +3.6 V.
V_{LS}	Used as power supply pin for analog circuit, connected to +3.0 to +5.5 V.
GNDL	Used as ground pin for logic circuit, connected to 0 V.
GNDA	Used as ground pin for LCD drive circuit, connected to 0 V.
SPIO SPOI	Used as input pins of start pulse and also used as output pins for cascade connection. When "H" is input into start pulse input pin, data sampling is started. On completion of sampling, "H" pulse is output to output pin for cascade connection. Pin functions are selected by LBR. For selecting, refer to **"Functional Operations"**.
LBR	Used as input pin for selecting the shift register direction. For selecting, refer to **"Functional Operations"**.
LS	Used as input pin for parallel transfer from sampling memory to hold memory. Data is transferred at the rising edge and output from LCD drive output pin.
CK	Used as shift clock input pin. Data is latched into sampling memory from data input pin at the rising edge.
V_1-V_{10}	Used as reference voltage input pins. Hold the reference voltage fixed during the period of LCD drive output. For relation between input data and output voltage values, refer to **"Output Voltage Value"**. For internal gamma correction, refer to **"Gamma Correction Value"**.
XA_0-XA_5, YA_0-YA_5 ZA_0-ZA_5, XB_0-XB_5 YB_0-YB_5, ZB_0-ZB_5	Used as data input pins of R, G, and B colors. 6-bit x 2-pixel data are input from data pins at the rising edge of CK. For relation between input data and output voltage values, refer to **"Functional Operations"** and **"Output Voltage Value"**. Select the data to be entered into X, Y, and Z according to picture element arrays of the panel.
XO_1-XO_{128}, YO_1-YO_{128}, ZO_1-ZO_{128}	Used as LCD drive output pins which output the voltage corresponding to the input of data input pins (XA_0 to XA_5, XB_0 to XB_5, YA_0 to YA_5, YB_0 to YB_5, ZA_0 to ZA_5, ZB_0 to ZB_5). Data of XO_1 to XO_{128} correspond to XA_0 to XA_5 and XB_0 to XB_5. Data of YO_1 to YO_{128} correspond to YA_0 to YA_5 and YB_0 to YB_5, and data of ZO_1 to ZO_{128} correspond to ZA_0 to ZA_5 and ZB_0 to ZB_5. For relation between input data and output voltage values, refer to **"Functional Operations"** and **"Output Voltage Value"**.
POL_1 POL_2	Used as input pins for input data polarity exchange. When "L" is entered, display data becomes normal mode. When "H" is entered, input data becomes polarity exchange mode (POL_1 = A system, POL_2 = B system). For relation between input data and output voltage values, refer to **"Output Voltage Value"**. Must be connected to 0 V or opened.
TESTB	Used as pin for IC testing. Must be connected to V_{CC} or opened.

Functional Operations

The following describes the relation between data input pin and output direction.

Data input pin	XA_0-XA_5	YA_0-YA_5	ZA_0-ZA_5	XB_0-XB_5	YB_0-YB_5	ZB_0-ZB_5	·····	XB_0-XB_5	YB_0-YB_5	ZB_0-ZB_5
Output direction	XO_1	YO_1	ZO_1	XO_2	YO_2	ZO_2	·····	XO_{128}	YO_{128}	ZO_{128}

The following describes the relation between LBR pin, SPOI pin, SPIO pin and output direction.

PIN	OUTPUT DIRECTION	
	RIGHT SHIFT (XO_1, YO_1, $ZO_1 \rightarrow XO_{128}$, YO_{128}, ZO_{128})	LEFT SHIFT (ZO_{128}, YO_{128}, $XO_{128} \rightarrow ZO_1$, YO_1, XO_1)
LBR	H	L
SPOI	Input	Output
SPIO	Output	Input

NOTE :

Color data corresponding to X, Y, and Z vary depending on the output direction.

Output Voltage Value

Two voltages are selected from all of the reference voltages (V_1-V_{10}) by the upper 3-bit data (D_5, D_4 and D_3) of the 6-bit input data (D_5, D_4, D_3, D_2, D_1 and D_0) taken by time sharing, and intermediate value is determined by the lower 3-bit data (D_2, D_1 and D_0).

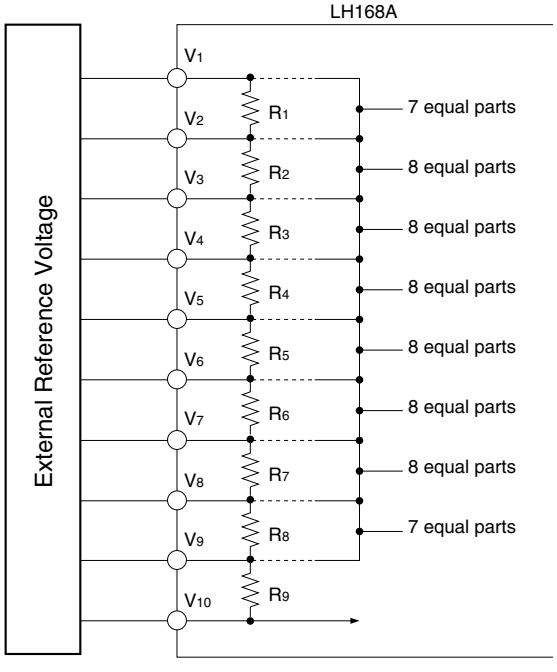
Relation between input data and output voltage values is shown below.

INPUT DATA	OUTPUT VOLTAGE		INPUT DATA	OUTPUT VOLTAGE	
	POL_1, POL_2 = "L"	POL_1, POL_2 = "H"		POL_1, POL_2 = "L"	POL_1, POL_2 = "H"
0	V_1	V_{10}	20	$V_6 + (V_5 - V_6) \times 7/8$	V_5
1	$V_2 + (V_1 - V_2) \times 6/7$	V_9	21	$V_6 + (V_5 - V_6) \times 6/8$	$V_5 + (V_4 - V_5) \times 1/8$
2	$V_2 + (V_1 - V_2) \times 5/7$	$V_9 + (V_8 - V_9) \times 1/7$	22	$V_6 + (V_5 - V_6) \times 5/8$	$V_5 + (V_4 - V_5) \times 2/8$
3	$V_2 + (V_1 - V_2) \times 4/7$	$V_9 + (V_8 - V_9) \times 2/7$	23	$V_6 + (V_5 - V_6) \times 4/8$	$V_5 + (V_4 - V_5) \times 3/8$
4	$V_2 + (V_1 - V_2) \times 3/7$	$V_9 + (V_8 - V_9) \times 3/7$	24	$V_6 + (V_5 - V_6) \times 3/8$	$V_5 + (V_4 - V_5) \times 4/8$
5	$V_2 + (V_1 - V_2) \times 2/7$	$V_9 + (V_8 - V_9) \times 4/7$	25	$V_6 + (V_5 - V_6) \times 2/8$	$V_5 + (V_4 - V_5) \times 5/8$
6	$V_2 + (V_1 - V_2) \times 1/7$	$V_9 + (V_8 - V_9) \times 5/7$	26	$V_6 + (V_5 - V_6) \times 1/8$	$V_5 + (V_4 - V_5) \times 6/8$
7	V_2	$V_9 + (V_8 - V_9) \times 6/7$	27	V_6	$V_5 + (V_4 - V_5) \times 7/8$
8	$V_3 + (V_2 - V_3) \times 7/8$	V_8	28	$V_7 + (V_6 - V_7) \times 7/8$	V_4
9	$V_3 + (V_2 - V_3) \times 6/8$	$V_8 + (V_7 - V_8) \times 1/8$	29	$V_7 + (V_6 - V_7) \times 6/8$	$V_4 + (V_3 - V_4) \times 1/8$
A	$V_3 + (V_2 - V_3) \times 5/8$	$V_8 + (V_7 - V_8) \times 2/8$	2A	$V_7 + (V_6 - V_7) \times 5/8$	$V_4 + (V_3 - V_4) \times 2/8$
B	$V_3 + (V_2 - V_3) \times 4/8$	$V_8 + (V_7 - V_8) \times 3/8$	2B	$V_7 + (V_6 - V_7) \times 4/8$	$V_4 + (V_3 - V_4) \times 3/8$
C	$V_3 + (V_2 - V_3) \times 3/8$	$V_8 + (V_7 - V_8) \times 4/8$	2C	$V_7 + (V_6 - V_7) \times 3/8$	$V_4 + (V_3 - V_4) \times 4/8$
D	$V_3 + (V_2 - V_3) \times 2/8$	$V_8 + (V_7 - V_8) \times 5/8$	2D	$V_7 + (V_6 - V_7) \times 2/8$	$V_4 + (V_3 - V_4) \times 5/8$
E	$V_3 + (V_2 - V_3) \times 1/8$	$V_8 + (V_7 - V_8) \times 6/8$	2E	$V_7 + (V_6 - V_7) \times 1/8$	$V_4 + (V_3 - V_4) \times 6/8$
F	V_3	$V_8 + (V_7 - V_8) \times 7/8$	2F	V_7	$V_4 + (V_3 - V_4) \times 7/8$
10	$V_4 + (V_3 - V_4) \times 7/8$	V_7	30	$V_8 + (V_7 - V_8) \times 7/8$	V_3
11	$V_4 + (V_3 - V_4) \times 6/8$	$V_7 + (V_6 - V_7) \times 1/8$	31	$V_8 + (V_7 - V_8) \times 6/8$	$V_3 + (V_2 - V_3) \times 1/8$
12	$V_4 + (V_3 - V_4) \times 5/8$	$V_7 + (V_6 - V_7) \times 2/8$	32	$V_8 + (V_7 - V_8) \times 5/8$	$V_3 + (V_2 - V_3) \times 2/8$
13	$V_4 + (V_3 - V_4) \times 4/8$	$V_7 + (V_6 - V_7) \times 3/8$	33	$V_8 + (V_7 - V_8) \times 4/8$	$V_3 + (V_2 - V_3) \times 3/8$
14	$V_4 + (V_3 - V_4) \times 3/8$	$V_7 + (V_6 - V_7) \times 4/8$	34	$V_8 + (V_7 - V_8) \times 3/8$	$V_3 + (V_2 - V_3) \times 4/8$
15	$V_4 + (V_3 - V_4) \times 2/8$	$V_7 + (V_6 - V_7) \times 5/8$	35	$V_8 + (V_7 - V_8) \times 2/8$	$V_3 + (V_2 - V_3) \times 5/8$
16	$V_4 + (V_3 - V_4) \times 1/8$	$V_7 + (V_6 - V_7) \times 6/8$	36	$V_8 + (V_7 - V_8) \times 1/8$	$V_3 + (V_2 - V_3) \times 6/8$
17	V_4	$V_7 + (V_6 - V_7) \times 7/8$	37	V_8	$V_3 + (V_2 - V_3) \times 7/8$
18	$V_5 + (V_4 - V_5) \times 7/8$	V_6	38	$V_9 + (V_8 - V_9) \times 6/7$	V_2
19	$V_5 + (V_4 - V_5) \times 6/8$	$V_6 + (V_5 - V_6) \times 1/8$	39	$V_9 + (V_8 - V_9) \times 5/7$	$V_2 + (V_1 - V_2) \times 1/7$
1A	$V_5 + (V_4 - V_5) \times 5/8$	$V_6 + (V_5 - V_6) \times 2/8$	3A	$V_9 + (V_8 - V_9) \times 4/7$	$V_2 + (V_1 - V_2) \times 2/7$
1B	$V_5 + (V_4 - V_5) \times 4/8$	$V_6 + (V_5 - V_6) \times 3/8$	3B	$V_9 + (V_8 - V_9) \times 3/7$	$V_2 + (V_1 - V_2) \times 3/7$
1C	$V_5 + (V_4 - V_5) \times 3/8$	$V_6 + (V_5 - V_6) \times 4/8$	3C	$V_9 + (V_8 - V_9) \times 2/7$	$V_2 + (V_1 - V_2) \times 4/7$
1D	$V_5 + (V_4 - V_5) \times 2/8$	$V_6 + (V_5 - V_6) \times 5/8$	3D	$V_9 + (V_8 - V_9) \times 1/7$	$V_2 + (V_1 - V_2) \times 5/7$
1E	$V_5 + (V_4 - V_5) \times 1/8$	$V_6 + (V_5 - V_6) \times 6/8$	3E	V_9	$V_2 + (V_1 - V_2) \times 6/7$
1F	V_5	$V_6 + (V_5 - V_6) \times 7/8$	3F	V_{10}	V_1

γ (gamma) Correction Value

Between reference voltage input pins, 7 or 8 resistors of the same resistance value are connected in series.

When the resistance ratio between respective reference voltage input pins matches the reference voltages (V_2 to V_9) for γ correction of LCD panel, the external power supply of the intermediate voltages (for V_2 to V_9 pins) is not required.



The following shows the ratio of γ correction resistance.

R_9	7.85
R_8	1.98
R_7	1.32
R_6	0.99
R_5	0.91
R_4	1.24
R_3	1.08
R_2	2.15
R_1	2.48

PRECAUTIONS

Precautions when connecting or disconnecting the power supply

This IC has some power supply pins, so it may be permanently damaged by a high current which may flow if voltage is supplied to the LCD drive power supply while the logic system power supply is floating. Therefore, when connecting the power supply, observe the following sequence.

V_{CC} → logic input → V_{LS}, V_1-V_{10}

When disconnecting the power supply, follow the reverse sequence.

Reference voltage input

The relation of the reference voltage input is shown here.

$GNDA < V_1 \leq V_2 \leq \cdots \leq V_9 \leq V_{10} < V_{LS}$ or
$V_{LS} > V_1 \geq V_2 \geq \cdots \geq V_9 \geq V_{10} > GNDA$

Maximum ratings

When connecting or disconnecting the power supply, this IC must be used within the range of the absolute maximum ratings.

Target output load

This IC is designed for a 70 pF output load capacity. When using this IC for other than 70 pF panels, confirm the device is having no problem before using it.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	APPLICABLE PINS	RATING	UNIT	NOTE
Supply voltage	V_{CC}	V_{CC}	−0.3 to +7.0	V	1, 2
	V_{LS}	V_{LS}	−0.3 to +7.0	V	
Input voltage	V_I	V_1-V_{10}	−0.3 to V_{LS} + 0.3	V	
	V_I	SPIO, SPOI, CK, LS, LBR, POL_1, POL_2, TESTB, XA_0-XA_5, XB_0-XB_5, YA_0-YA_5, YB_0-YB_5, ZA_0-ZA_5, ZB_0-ZB_5	−0.3 to V_{CC} + 0.3	V	
Output voltage	V_O	SPIO, SPOI	−0.3 to V_{CC} + 0.3	V	
	V_O	XO_1-ZO_{128}	−0.3 to V_{LS} + 0.3	V	
Storage temperature	T_{STG}		−45 to +125	˚C	

NOTES :

1. T_A = +25 ˚C
2. The maximum applicable voltage on any pin with respect to GNDL and GNDA (0 V).

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V_{CC}	+2.7		+3.6	V	1
	V_{LS}	+3.0		+5.5	V	
Reference voltage input	V_1-V_{10}	0		V_{LS}	V	
Clock frequency	f_{CK}			55	MHz	
LCD drive output load capacity	C_L			70	pF	
Operating temperature	T_{OPR}	−20		+75	˚C	

NOTE :

1. The applicable voltage on any pin with respect to GNDL and GNDA (0 V).

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{CC} = +2.7 to +3.6 V, V_{LS} = +3.0 to +5.5 V, T_{OPR} = −20 to +75 °C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		XA_0-XA_5, YA_0-YA_5, ZA_0-ZA_5, XB_0-XB_5, YB_0-YB_5, ZB_0-ZB_5, SPIO, SPOI, CK, LS, LBR	GNDL		0.3V_{CC}	V	
Input "High" voltage	V_{IH}			0.7V_{CC}		V_{CC}	V	
Output "Low" voltage	V_{OL}	I_{OL} = 0.3 mA	SPIO, SPOI	GNDL		GNDL + 0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = −0.3 mA		V_{CC} − 0.4		V_{CC}	V	
Input "Low" current	I_{ILL}		XA_0-XA_5, YA_0-YA_5, ZA_0-ZA_5, XB_0-XB_5, YB_0-YB_5, ZB_0-ZB_5, SPIO, SPOI, CK, LS, LBR, POL_1, POL_2			1	µA	
Input "High" current	I_{ILH1}		XA_0-XA_5, YA_0-YA_5, ZA_0-ZA_5, XB_0-XB_5, YB_0-YB_5, ZB_0-ZB_5, SPIO, SPOI, CK, LS, LBR			1	µA	
	I_{ILH2}		POL_1, POL_2			400	µA	
Supply current (In operation mode)	I_{CC1}	f_{CK} = 55 MHz f_{LS} = 50 kHz (Data sampling state)	V_{CC}-GNDL			12	mA	
Supply current (In standby mode)	I_{CC2}	f_{CK} = 55 MHz f_{LS} = 50 kHz SPI = GND is fixed. (Standby state)	V_{CC}-GNDL			4	mA	
Supply current (In operation mode)	I_{LS1}	f_{CK} = 55 MHz f_{LS} = 50 kHz (Data sampling state)	V_{LS}-GNDA			10	mA	
Supply current (In standby mode)	I_{LS2}	f_{CK} = 55 MHz f_{LS} = 50 kHz SPI = GND is fixed. (Standby state)	V_{LS}-GNDA			9	mA	
Output voltage range	V_{OUT}		XO_1-ZO_{128}	GNDA + 0.1		V_{LS} − 0.1	V	1
Deviations between output voltage pins	V_{OD}			−20		20	mV	
Output current	I_{O1}, I_{O2}			20	50		µA	2
Resistance between reference voltage input pins	R_{GMA}		V_1-V_{10}	10		30	kΩ	

NOTES :

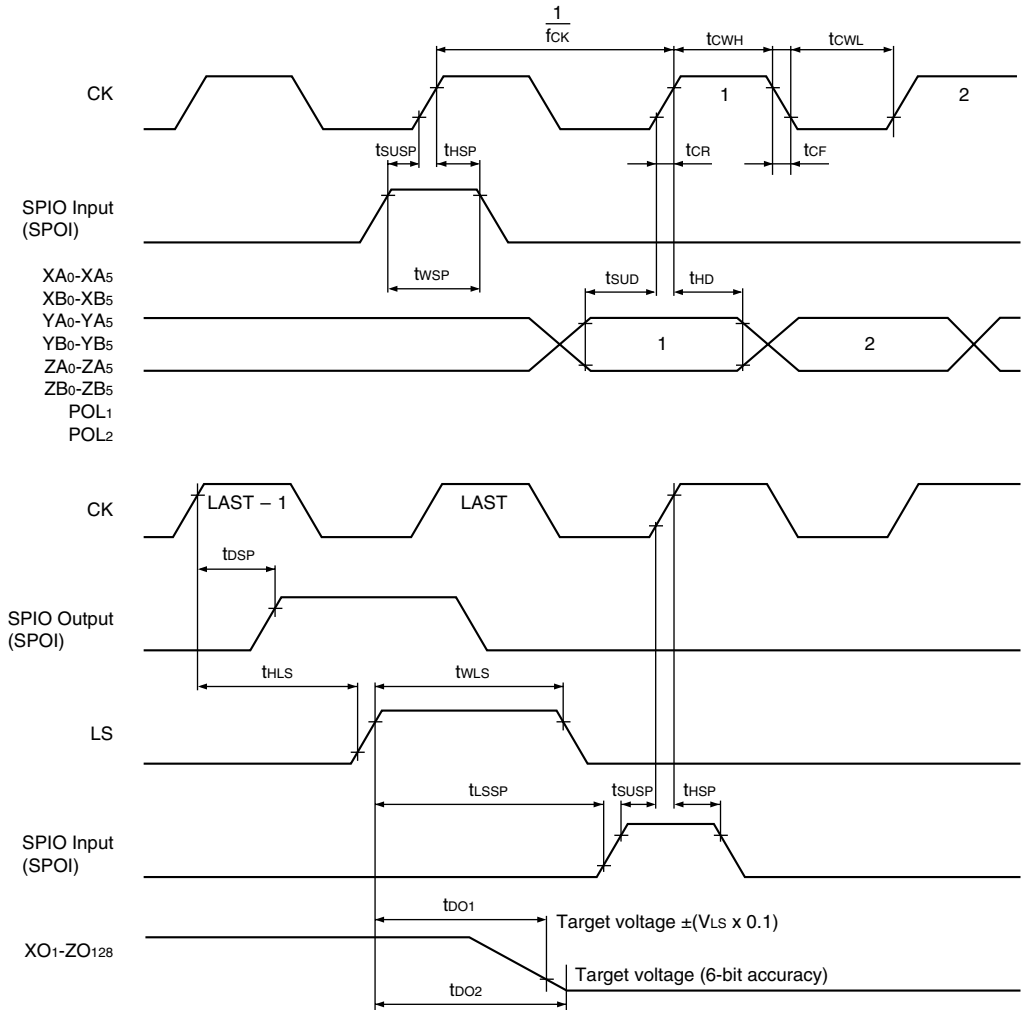
1. Criterion of evaluating voltage deviations.
   (a) Between output voltage pins
   Measuring values : Output voltage value at the time after 10 µs at the rising edge of LS. (Average of several times)
   (Conditions) Output load capacity is 70 pF.
   In a state when the reference voltage is fixed.
   Expecting values : Calculated following these specifications.
   (Conditions) In a state when the reference voltage is fixed.
   (b) Between LCD drivers
   Measuring values : Applicable to (a).
   (Conditions) Applicable to (a).
   Expecting values : Applicable to (a).
   (Conditions) Applicable to (a).
   Each input voltage between the LCD drivers must be made perfectly equal by connecting corresponding reference voltage input pins.
2. I_{O1} : Applied voltage = 3.0 V for output pins XO_1 to ZO_{128}.
   Output voltage = 2.5 V for output pins XO_1 to ZO_{128}.
   V_{LS} = 5.0 V
   I_{O2} : Applied voltage = 2.0 V for output pins XO_1 to ZO_{128}.
   Output voltage = 2.5 V for output pins XO_1 to ZO_{128}.
   V_{LS} = 5.0 V

AC Characteristics

(V_{CC} = +2.7 to +3.6 V, V_{LS} = +3.0 to +5.5 V, T_{OPR} = –20 to +75 ˚C)

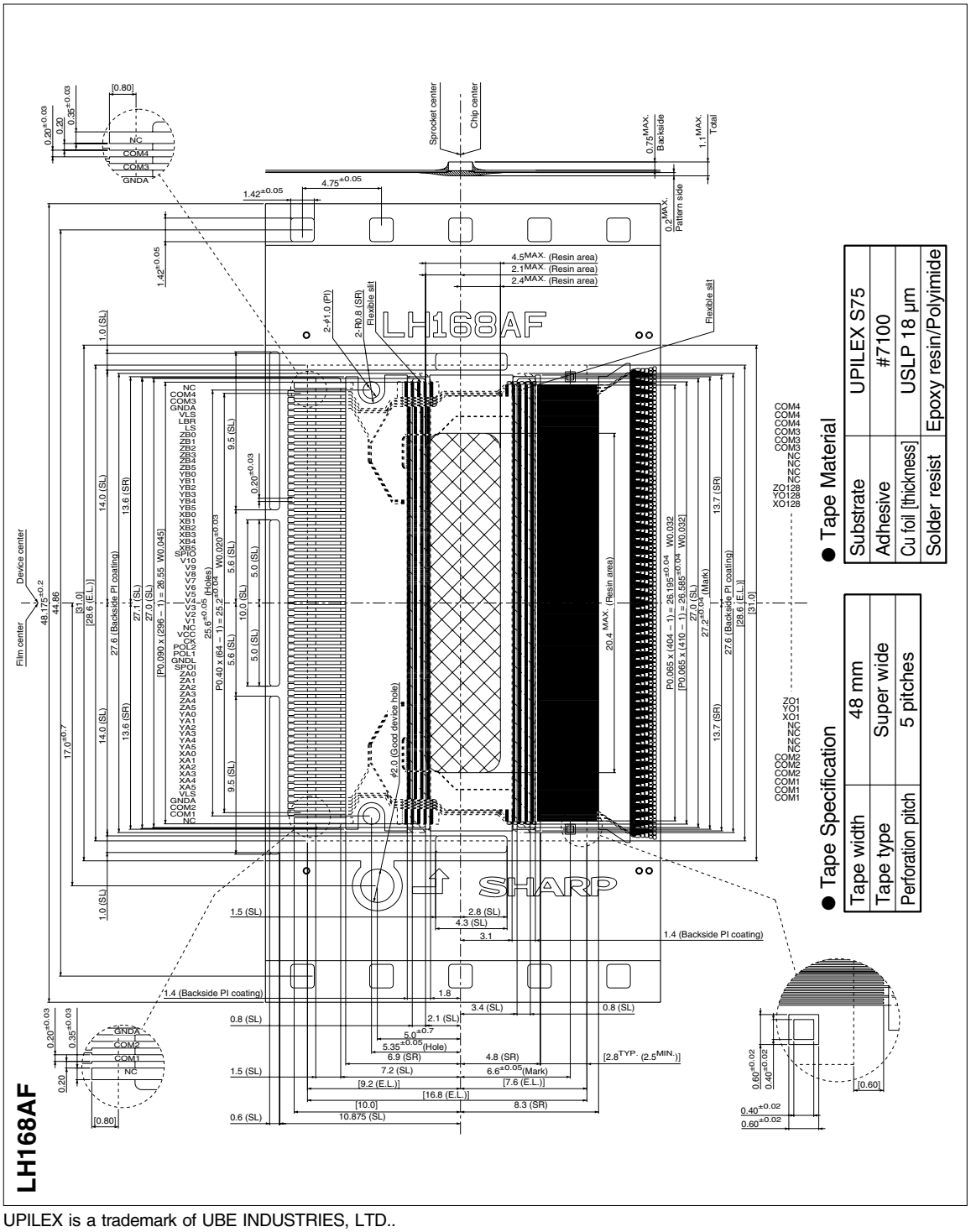
PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT
Clock frequency	f_{CK}		CK			55	MHz
"H" level pulse width	t_{CWH}			4			ns
"L" level pulse width	t_{CWL}			4			ns
Input rise time	t_{CR}					4	ns
Input fall time	t_{CF}					4	ns
Data setup time	t_{SUD}		XA_0-XA_5, YA_0-YA_5, ZA_0-ZA_5, XB_0-XB_5, YB_0-YB_5, ZB_0-ZB_5, POL_1, POL_2	4			ns
Data hold time	t_{HD}			0			ns
Start pulse setup time	t_{SUSP}		SPIO, SPOI	4			ns
Start pulse hold time	t_{HSP}			0			ns
Start pulse width	t_{WSP}					$\frac{1}{f_{CK}}$	ns
Start pulse output delay time	t_{DSP}	C_L = 10 pF				12	ns
LCD drive output delay time 1	t_{DO1}	C_L = 70 pF	XO_1-ZO_{128}			3	µs
LCD drive output delay time 2	t_{DO2}	C_L = 70 pF				10	µs
LS signal-SPI signal set up time	t_{LSSP}		LS	$\frac{1}{f_{CK}}$			ns
LS signal-CK signal hold time	t_{HLS}			9			ns
LS signal "H" level width	t_{WLS}			$\frac{1}{f_{CK}}$			ns

Timing Chart



PACKAGE

(Unit : mm)



● Tape Material

Substrate	UPILEX S75
Adhesive	#7100
Cu foil [thickness]	USLP 18 µm
Solder resist	Epoxy resin/Polyimide

● Tape Specification

Tape width	48 mm
Tape type	Super wide
Perforation pitch	5 pitches

LH168AF

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