LH53B16R00

CMOS 16M (1M × 16/512K × 32) MROM

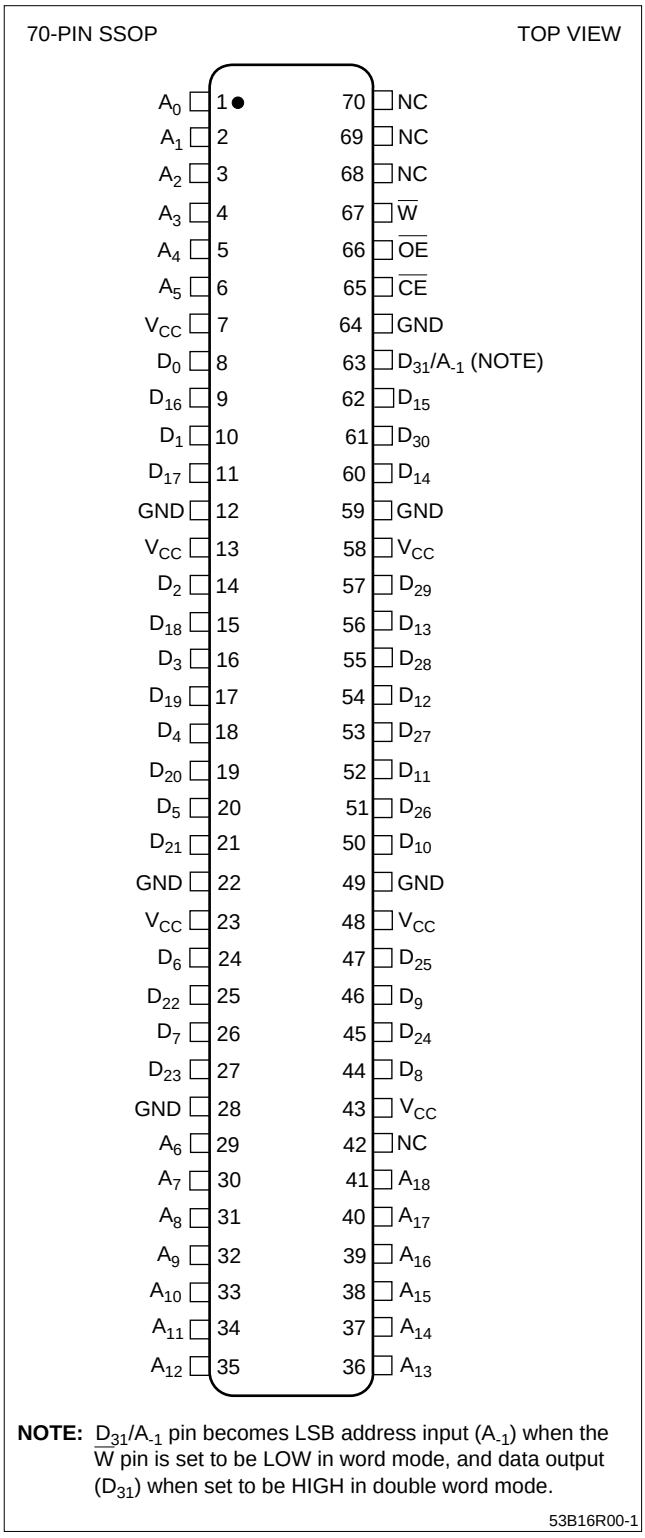
FEATURES

- 1,048,576 × 16 bit organization
  (Word mode: $\overline{W}$ = V_{IL})
  524,288 × 32 bit organization
  (Double Word mode: $\overline{W}$ = V_{IH})
- Access time: 120 ns (MAX.)
  Access time in page mode: 50 ns (MAX.)
- Supply current:
  - Operating: 180 mA (MAX.)
  - Standby: 300 µA (MAX.)
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Static operation
- Package:
  70-pin, 500-mil SSOP
- Others:
  - Non programmable
  - Not designed or rated as radiation
  - hardened
  - CMOS process (P type silicon substrate)

DESCRIPTION

The LH53B16R00 is a 16M-bit CMOS mask ROM (mask-programmable-read-only memory) organized as 1,048,576 × 16 bits (Word mode) or 524,288 × 32 bits (Double Word mode). It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS



NOTE: D_{31}/A_{-1} pin becomes LSB address input (A_{-1}) when the $\overline{W}$ pin is set to be LOW in word mode, and data output (D_{31}) when set to be HIGH in double word mode.

53B16R00-1

Figure 1. Pin Connections

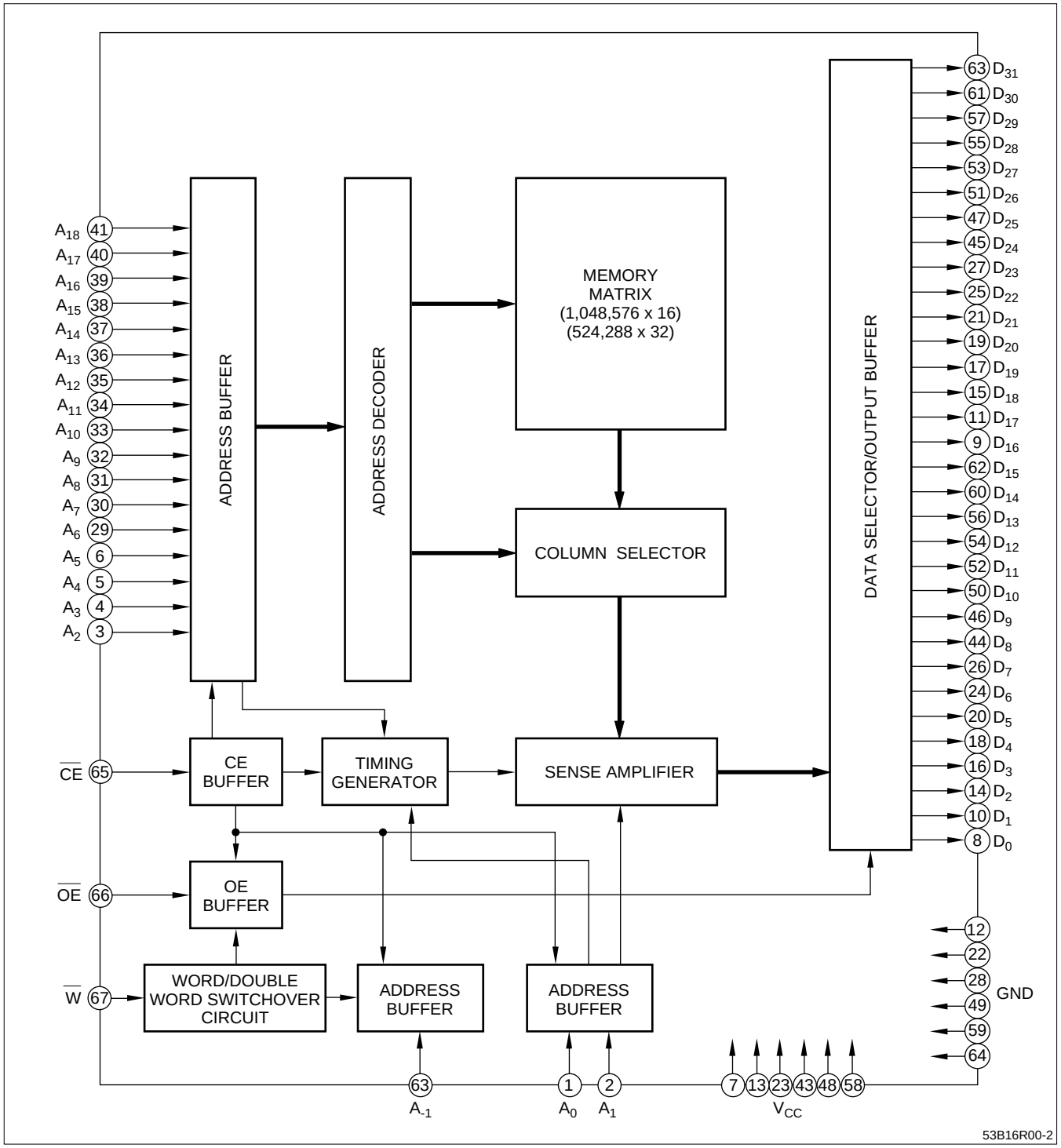


Figure 2. LH53B16R00 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_{-1} - A_1	Address input (page mode operation)
A_2 - A_{18}	Address input
D_0 - D_{31}	Data output
$\overline{W}$	×16 bit / ×32 bit (word/double word) mode select input

SIGNAL	PIN NAME
$\overline{CE}$	Chip enable input
$\overline{OE}$	Output enable input
V_{CC}	Power pin (+5 V)
GND	Ground
NC	No connection

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{W}$	A_{-1} (D_{31})	DATA OUTPUT		ADDRESS INPUT		SUPPLY CURRENT
				D_0 - D_{15}	D_{16} - D_{31}	LSB	MSB	
H	X	X	X	High-Z	High-Z	—	—	Standby (I_{SB})
L	H	X	X	High-Z	High-Z	—	—	Operating
L	L	H	—	D_0 - D_{15}	D_{16} - D_{31}	A_0	A_{18}	Operating
L	L	L	L	D_0 - D_{15}	High-Z	A_{-1}	A_{18}	Operating
L	L	L	H	D_{16} - D_{31}	High-Z	A_{-1}	A_{18}	Operating

NOTE:
X = Don't care; High-Z = High-impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	-0.3 to +7.0	V
Input voltage	V_{IN}	-0.3 to V_{CC} + 0.3	V
Output voltage	V_{OUT}	-0.3 to V_{CC} + 0.3	V
Operating temperature	T_{OPR}	0 to +70	°C
Storage temperature	T_{STG}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input 'High' voltage	V_{IH}	—	2.2	V_{CC} +0.3	V	—
Input 'Low' voltage	V_{IL}	—	-0.3	0.8	V	—
Output 'High' voltage	V_{OH}	I_{OH} = -400 µA	2.4	—	V	—
Output 'Low' voltage	V_{OL}	I_{OL} = 2.0 mA	—	0.4	V	—
Input leakage current	$\| I_{LI} \|$	V_{IN} = 0 V to V_{CC}	—	10	µA	—
Output leakage current	$\| I_{LO} \|$	V_{OUT} = 0 V to V_{CC}	—	10	µA	1
Operating current	I_{CC1}	t_{RC} = 120 ns	—	180	mA	2
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}	—	2	mA	—
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V	—	300	µA	—
Input capacitance	C_{IN}	f = 1 MHz, t_A = 25°C	—	10	pF	—
Output capacitance	C_{OUT}		—	10	pF	—

NOTES:
1. $\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IH}, output is open
2. V_{IN} = V_{IH}, V_{IL}, $\overline{CE}$ = V_{IL}, output is open

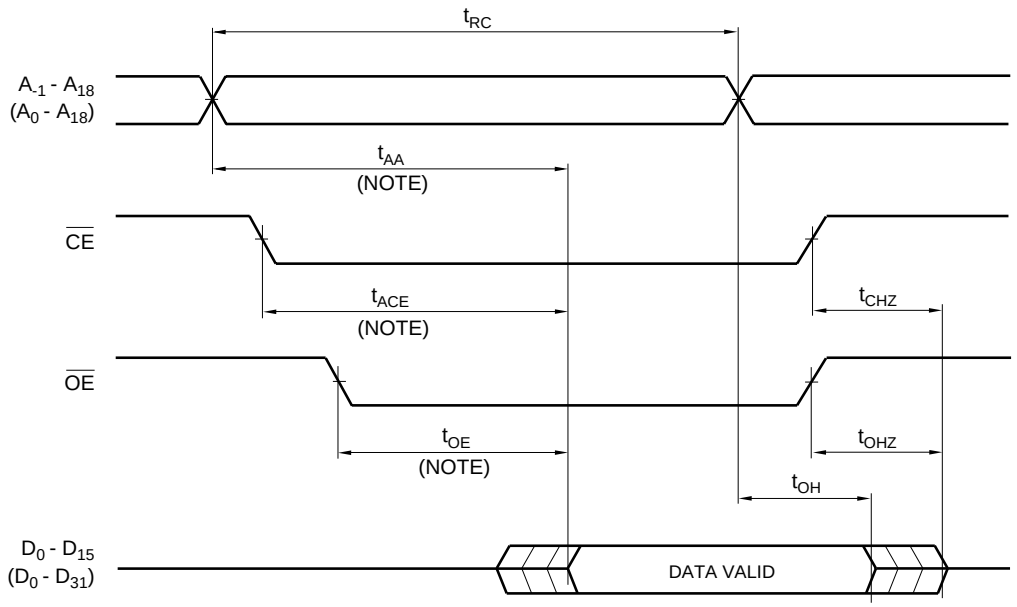
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	120	—	ns	—
Address access time	t_{AA}	—	120	ns	—
Chip enable access time	t_{ACE}	—	120	ns	—
Page address access time	t_{APA}	—	50	ns	
Output enable delay time	t_{OE}	—	50	ns	—
Output hold time	t_{OH}	5	—	ns	—
Output floating time	t_{CHZ}	—	40	ns	1
	t_{OHZ}	—	40	ns	

NOTE:
1. Determined by the time for the output to be opened. (Irrespective of output voltage)

AC TEST CONDITIONS

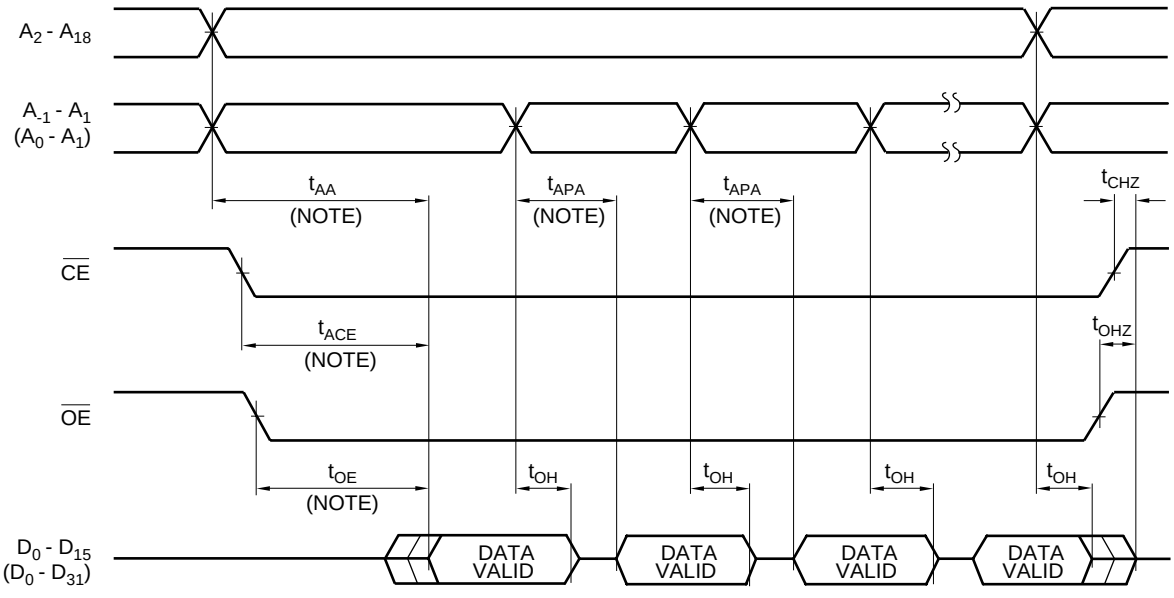
PARAMETER	RATING
Input voltage amplitude	0.4 V to 2.6 V
Input signal rise time	10 ns
Input signal fall time	10 ns
Input/output reference level	1.5 V
Output load condition	1TTL + 100 pF



NOTE: The output data becomes valid when the last intervals, t_{AA}, t_{ACE}, t_{APA}, or t_{OE}, have concluded.

53B16R00-3

Figure 3. Read Cycle



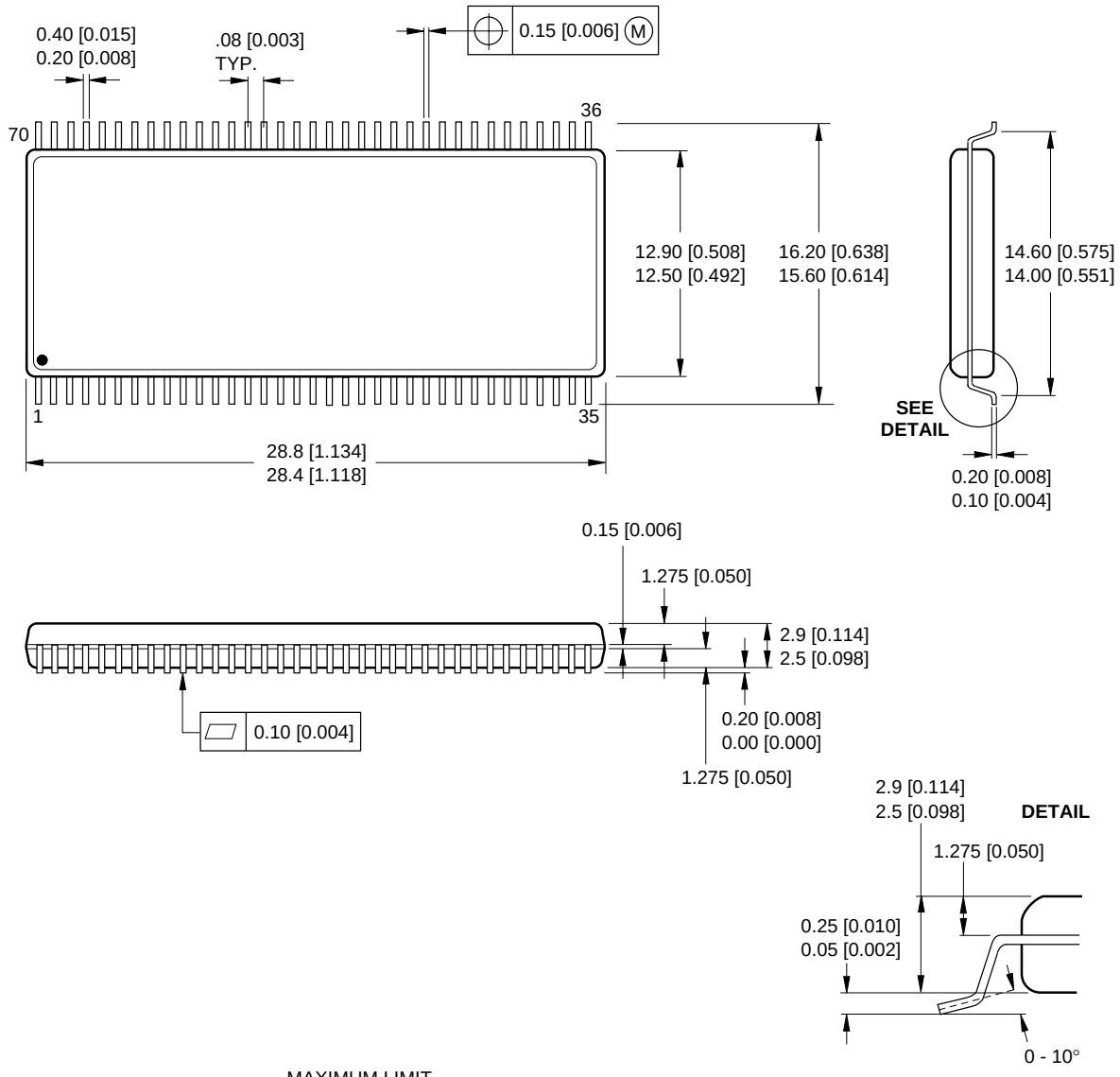
NOTE: The output data becomes valid when the last intervals, t_{AA}, t_{ACE}, t_{APA}, or t_{OE}, have concluded.

53B16R00-4

Figure 4. Page Mode Read Cycle

PACKAGE DIAGRAM

70SSOP (SSOP70-P-500)



ORDERING INFORMATION

LH53B16R00	N
Device Type	Package

N — 70-pin, 500-mil SSOP (SSOP70-P-500)

LH53B16R00 — CMOS 16M (1M x 16 or 500K x 32) Mask-Programmable ROM with page mode operation

Example: LH53B16R00N (CMOS 16M (1M x 16 or 500K x 32) Mask-Programmable ROM, 70-pin, 500-mil SSOP)

53B16R00-5