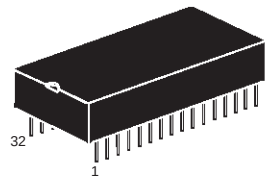
M48Z512A
M48Z512AY

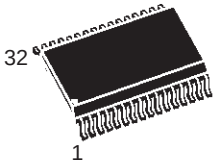
4 Mbit (512Kb x8) ZEROPOWER® SRAM

- INTEGRATED LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT and BATTERY
- CONVENTIONAL SRAM OPERATION; UNLIMITED WRITE CYCLES
- 10 YEARS of DATA RETENTION in the ABSENCE of POWER
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- WRITE PROTECT VOLTAGES (V_{PFD} = Power-fail Deselect Voltage):
  - M48Z512A: 4.50V ≤ V_{PFD} ≤ 4.75V
  - M48Z512AY: 4.20V ≤ V_{PFD} ≤ 4.50V
- BATTERY INTERNALLY ISOLATED UNTIL POWER IS APPLIED
- PIN and FUNCTION COMPATIBLE with JEDEC STANDARD 512K x 8 SRAMs
- SURFACE MOUNT CHIP SET PACKAGING INCLUDES a 28-PIN SOIC and a 32-LEAD TSOP (SNAPHAT TOP TO BE ORDERED SEPARATELY)
- SOIC PACKAGE PROVIDES DIRECT CONNECTION for a SNAPHAT TOP WHICH CONTAINS the BATTERY
- SNAPHAT® HOUSING (BATTERY) IS REPLACEABLE

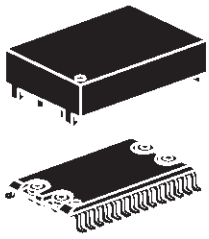


PMDIP32 (PM)
Module

SNAPHAT (SH)
Battery



TSOP II 32
(10 x 20mm)



SOH28

Surface Mount Chip Set Solution (CS)

Figure 1. Logic Diagram

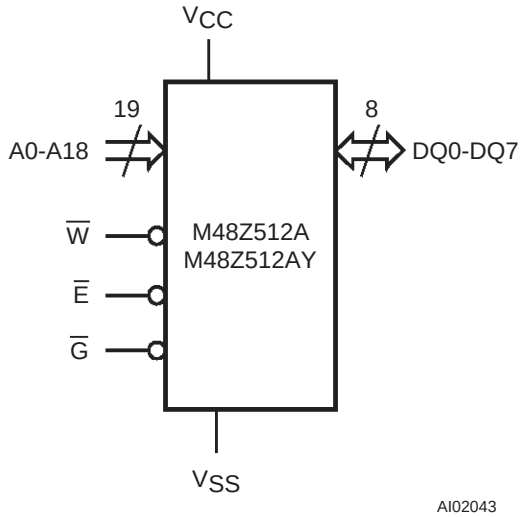


Table 1. Signal Names

A0-A18	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature (V_{CC} Off)	–40 to 70	°C
T_{BIAS}	Temperature Under Bias	–40 to 70	°C
T_{SLD} (2)	Lead Solder Temperature for 10 seconds	260	°C
V_{IO}	Input or Output Voltages	–0.3 to 7	V
V_{CC}	Supply Voltage	–0.3 to 7	V

Note: 1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum rating conditions for extended periods of time may affect reliability.

2. Soldering temperature not to exceed 260°C for 10 seconds (total thermal budget not to exceed 150°C for longer than 30 seconds).

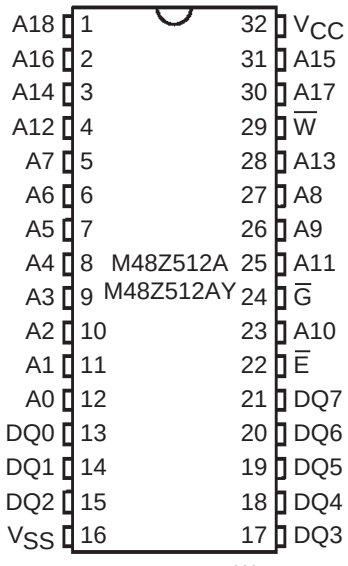
CAUTION: *Negative undershoots below –0.3V are not allowed on any pin while in the Battery Back-up mode.*

Table 3. Operating Modes

Mode	V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	4.75V to 5.5V or 4.5V to 5.5V	V_{IH}	X	X	High Z	Standby
Write		V_{IL}	X	V_{IL}	D_{IN}	Active
Read		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
Read		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min)	X	X	X	High Z	CMOS Standby
Deselect	≤ V_{SO}	X	X	X	High Z	Battery Back-up Mode

Note: 1. X = V_{IH} or V_{IL}; V_{SO} = Battery Back-up Switchover Voltage.

Figure 2. DIP Connections



DESCRIPTION

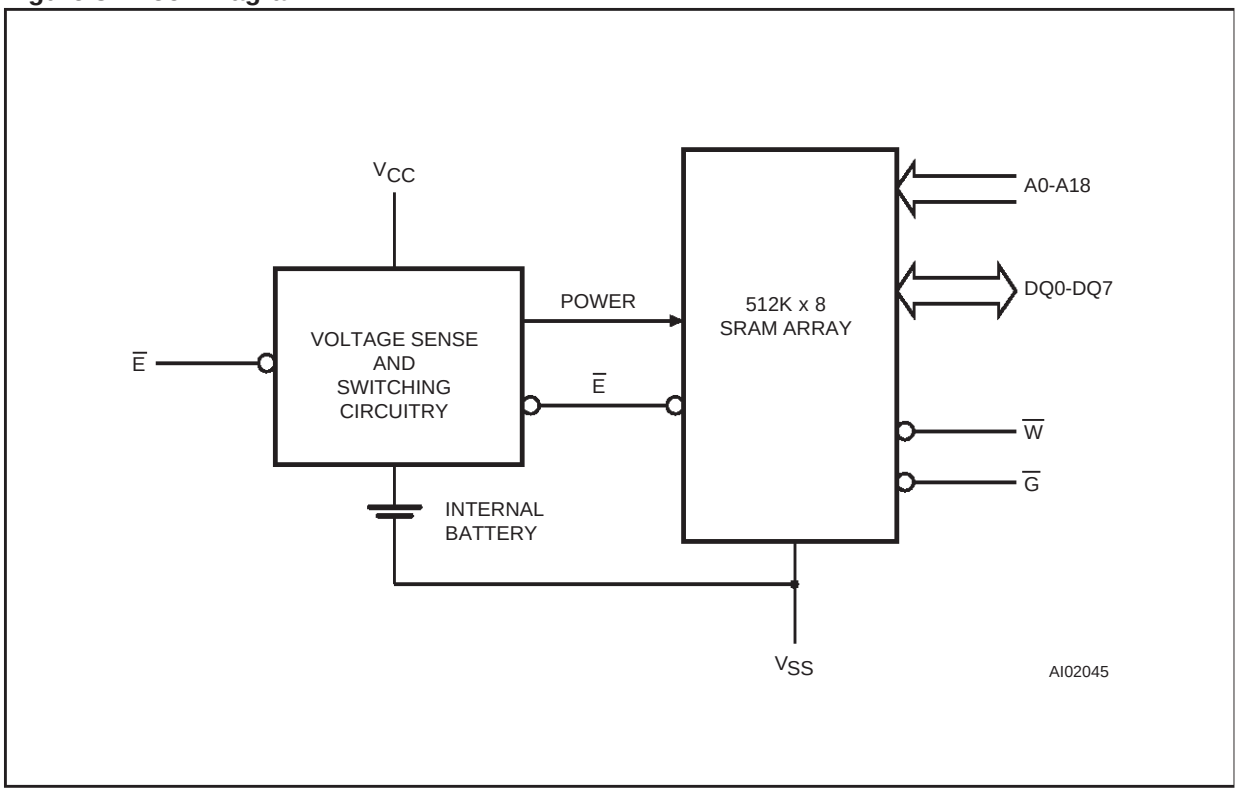
The M48Z512A/512AY ZEROPOWER® RAM is a non-volatile 4,194,304 bit Static RAM organized as 524,288 words by 8 bits. The device combines an internal lithium battery, a CMOS SRAM and a control circuit in a plastic 32 pin DIP Module.

For surface mount environments ST provides a Chip Set solution consisting of a 28 pin 330mil SOIC NVRAM Supervisor (M40Z300) and a 32 pin TSOP Type II (10 x 20mm) LPSRAM (M68Z512) packages.

The unique design allows the SNAPHAT battery package to be mounted on top of the SOIC package after the completion of the surface mount process. Insertion of the SNAPHAT housing after reflow prevents potential battery damage due to the high temperatures required for device surface-mounting. The SNAPHAT housing is keyed to prevent reverse insertion.

The SNAPHAT battery package is shipped separately in plastic anti-static tubes or in Tape & Reel form. The part number is "M4Zxx-BR00SH1".

Figure 3. Block Diagram

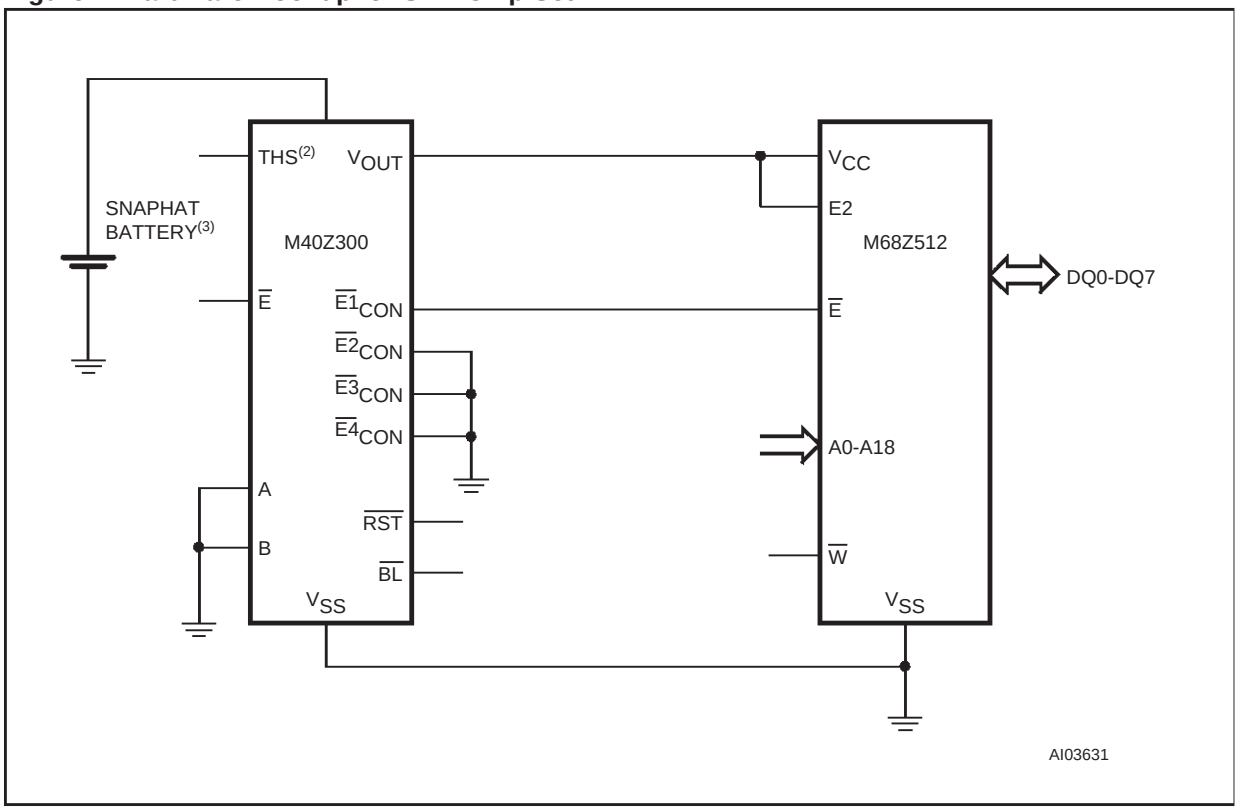


The M48Z512A/512AY also has its own Power-fail Detect circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the battery which maintains data until valid power returns.

The ZEROPOWER RAM replaces industry standard SRAMs. It provides the nonvolatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

The M48Z512A/512AY has its own Power-fail Detect Circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operations brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the battery which sustains data until valid power returns.

Figure 4. Hardware Hookup for SMT Chip Set (1)



Note: 1. For pin connections, see individual data sheets for M40Z300 and M68Z512 at www.st.com.
2. Connect THS pin to V_{OUT} if $4.2V \le V_{PFD} \le 4.5V$ (M48Z512AY) or connect THS pin to V_{SS} if $4.5V \le V_{PFD} \le 4.75V$ (M48Z512A).
3. SNAPHAT top ordered separately.

Table 4. AC Measurement Conditions

Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 5. AC Testing Load Circuit

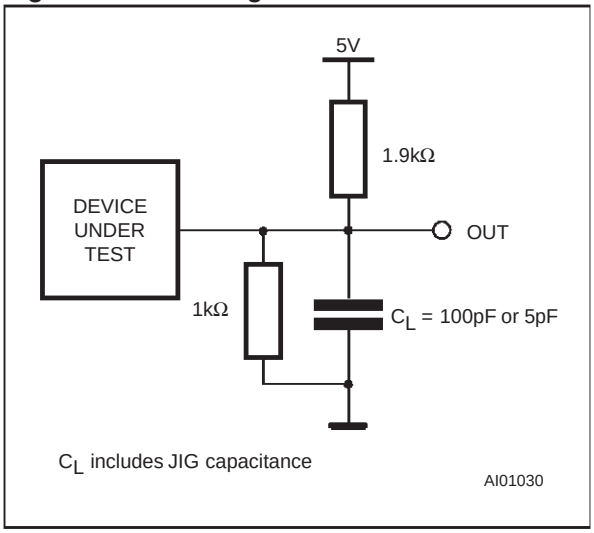


Table 5. Capacitance (1, 2)
(T_A = 25 °C, f = 1MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		10	pF
C_{IO} (3)	Input / Output Capacitance	V_{OUT} = 0V		10	pF

Note: 1. Effective capacitance measured with power supply at 5V.
2. Sampled only, not 100% tested.
3. Outputs deselected.

Table 6. DC Characteristics
(T_A = 0 to 70 °C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI} (1)	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO} (1)	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±1	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, Outputs open		115	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		10	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E} \ge V_{CC} - 0.2V$		5	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.4		V

Note: 1. Outputs deselected.

Table 7. Power Down/Up Trip Points DC Characteristics (1)
(T_A = 0 to 70 °C)

Symbol	Parameter		Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage	M48Z512A	4.5	4.6	4.75	V
		M48Z512AY	4.2	4.3	4.5	V
V_{SO}	Battery Back-up Switchover Voltage			3		V
t_{DR} (2)	Data Retention Time		10			YEARS

Note: 1. All voltages referenced to V_{SS}.
2. At 25 °C.

Table 8. Power Down/Up AC Characteristics
(T_A = 0 to 70 °C)

Symbol	Parameter	Min	Max	Unit
t_F (1)	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs
t_{FB} (2)	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10		µs
t_{WP}	Write Protect Time from V_{CC} = V_{PFD}	40	150	µs
t_R	V_{SO} to V_{PFD} (max) V_{CC} Rise Time	0		µs
t_{ER}	$\overline{E}$ Recovery Time	40	120	ms

Note: 1. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200µs after V_{CC} passes V_{PFD} (min).
2. V_{PFD} (min) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.

Figure 6. Power Down/Up Mode AC Waveforms

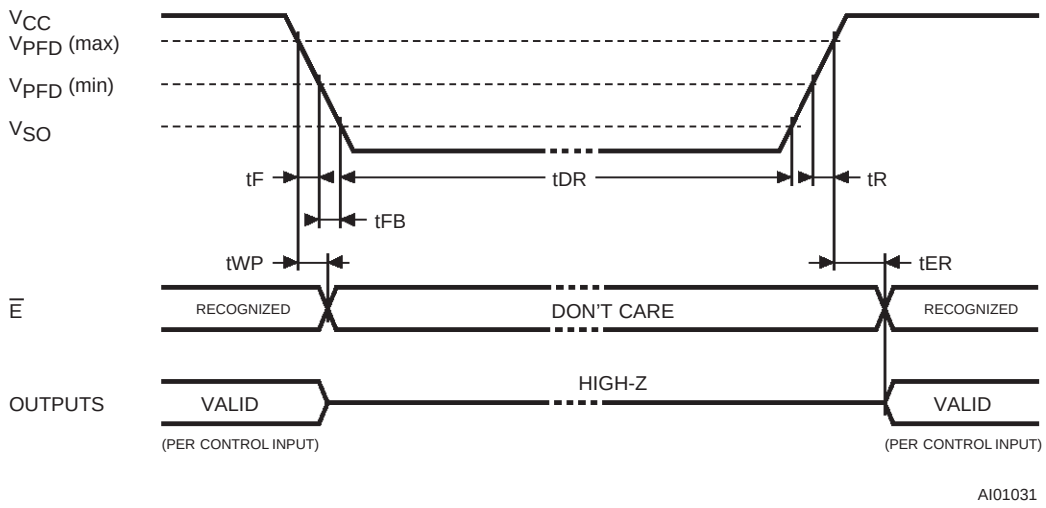
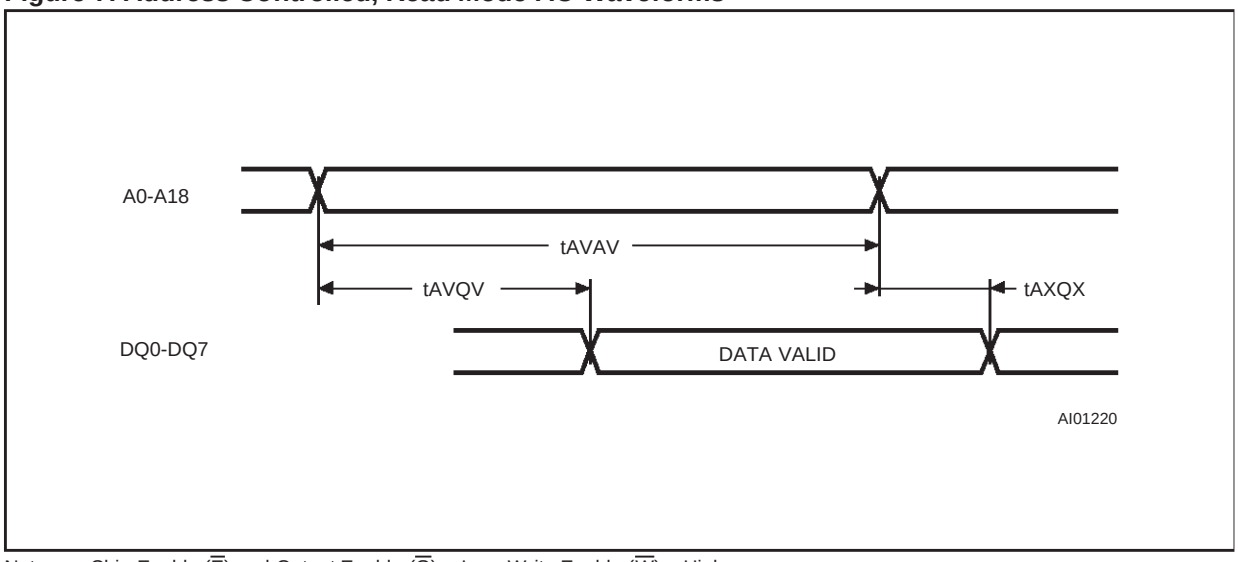


Table 9. Read Mode AC Characteristics
(T_A = 0 to 70 °C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48Z512A/M48Z512AY				Unit
		-70		-85		
		Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time	70		85		ns
t_{AVQV} (1)	Address Valid to Output Valid		70		85	ns
t_{ELQV} (1)	Chip Enable Low to Output Valid		70		85	ns
t_{GLQV} (1)	Output Enable Low to Output Valid		35		45	ns
t_{ELQX} (2)	Chip Enable Low to Output Transition	5		5		ns
t_{GLQX} (2)	Output Enable Low to Output Transition	5		5		ns
t_{EHQZ} (2)	Chip Enable High to Output Hi-Z		30		35	ns
t_{GHQZ} (2)	Output Enable High to Output Hi-Z		20		25	ns
t_{AXQX} (1)	Address Transition to Output Transition	5		5		ns

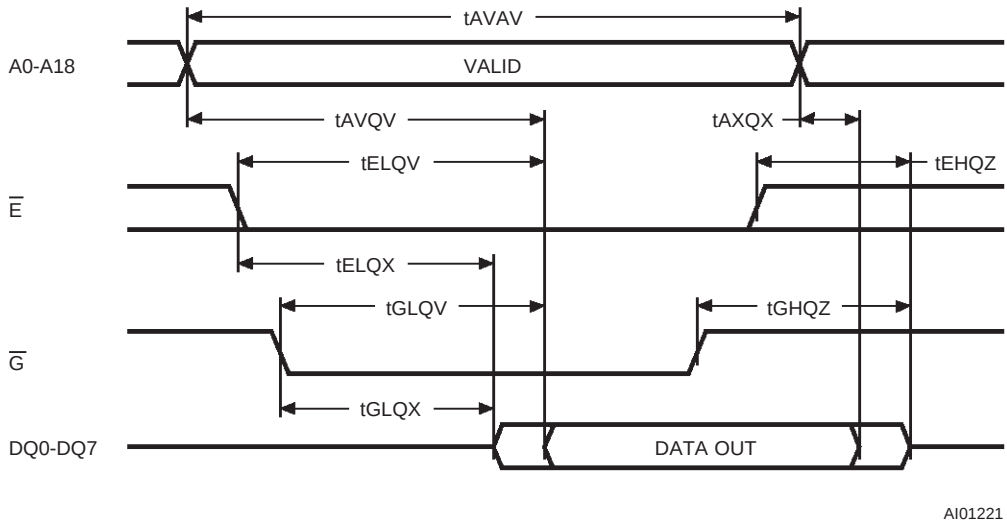
Note: 1. C_L = 100pF.
2. C_L = 5pF.

Figure 7. Address Controlled, Read Mode AC Waveforms



Note: Chip Enable ($\overline{E}$) and Output Enable ($\overline{G}$) = Low, Write Enable ($\overline{W}$) = High.

Figure 8. Chip Enable or Output Enable Controlled, Read Mode AC Waveforms



Note: Write Enable ($\overline{W}$) = High.

READ MODE

The M48Z512A/512AY is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low. The device architecture allows ripple-through access of data from eight of 4,194,304 locations in the static storage array. Thus, the unique address specified by the 19 Address Inputs defines which one of the 524,288 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within Address Access time (t_{AVQV}) after the last address input signal is stable, providing that the $\overline{E}$ (Chip Enable) and $\overline{G}$ (Output Enable) access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the later of Chip Enable Access time (t_{ELQV}) or Output Enable Access Time (t_{GLQV}). The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E}$ and $\overline{G}$ remain low, output data will remain valid for Output Data Hold time (t_{AXQX}) but will go indeterminate until the next Address Access.

Table 10. Write Mode AC Characteristics
(T_A = 0 to 70 °C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48Z512A/M48Z512AY				Unit
		-70		-85		
		Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time	70		85		ns
t_{AVWL}	Address Valid to Write Enable Low	0		0		ns
t_{AVEL}	Address Valid to Chip Enable Low	0		0		ns
t_{WLWH}	Write Enable Pulse Width	55		65		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	55		75		ns
t_{WHAX}	Write Enable High to Address Transition	5		5		ns
t_{EHAX}	Chip Enable High to Address Transition	15		15		ns
t_{DVWH}	Input Valid to Write Enable High	30		35		ns
t_{DVEH}	Input Valid to Chip Enable High	30		35		ns
t_{WHDX}	Write Enable High to Input Transition	0		0		ns
t_{EHDX}	Chip Enable High to Input Transition	10		10		ns
t_{WLQZ} (1, 2)	Write Enable Low to Output Hi-Z		25		30	ns
t_{AVWH}	Address Valid to Write Enable High	65		75		ns
t_{AVEH}	Address Valid to Chip Enable High	65		75		ns
t_{WHQX} (1, 2)	Write Enable High to Output Transition	5		5		ns

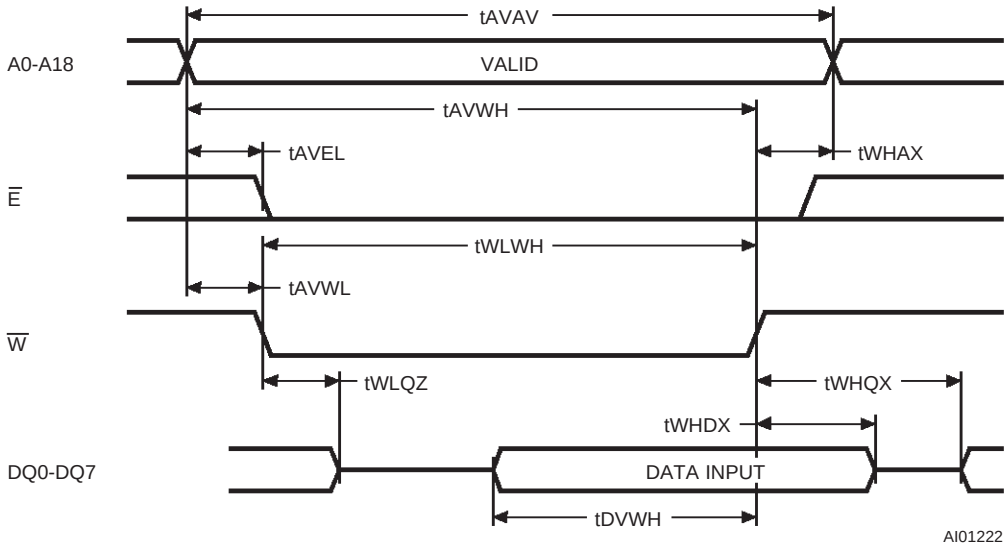
Note: 1. C_L = 5pF.
2. If $\overline{E}$ goes low simultaneously with $\overline{W}$ going low, the outputs remain in the high impedance state.

WRITE MODE

The M48Z512A/512AY is in the Write Mode whenever $\overline{W}$ and $\overline{E}$ are active. The start of a write is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$.

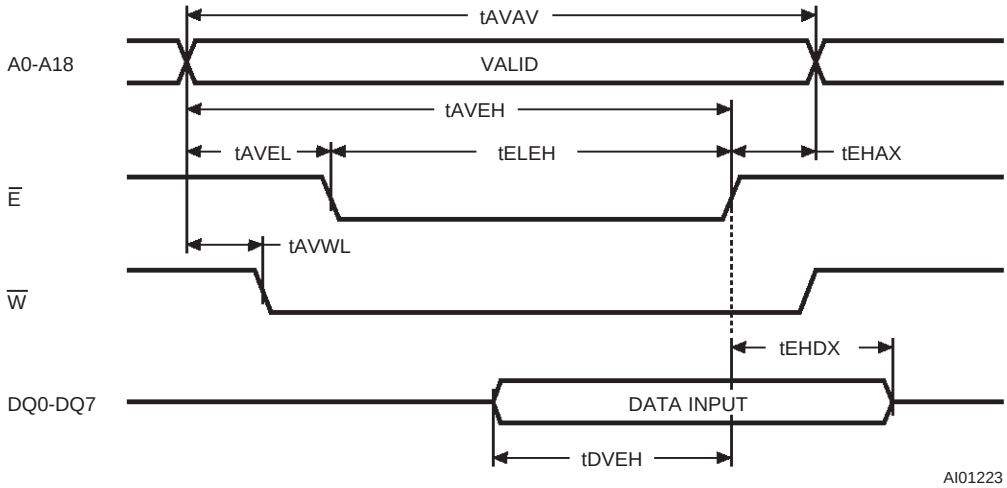
The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for a minimum of t_{EHAX} from $\overline{E}$ or t_{WHAX} from $\overline{W}$ prior to the initiation of another read or write cycle. Data-in must be valid t_{DVEH} or t_{DVWH} prior to the end of write and remain valid for t_{EHDX} or t_{WHDX} afterward. $\overline{G}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

Figure 9. Write Enable Controlled, Write AC Waveforms



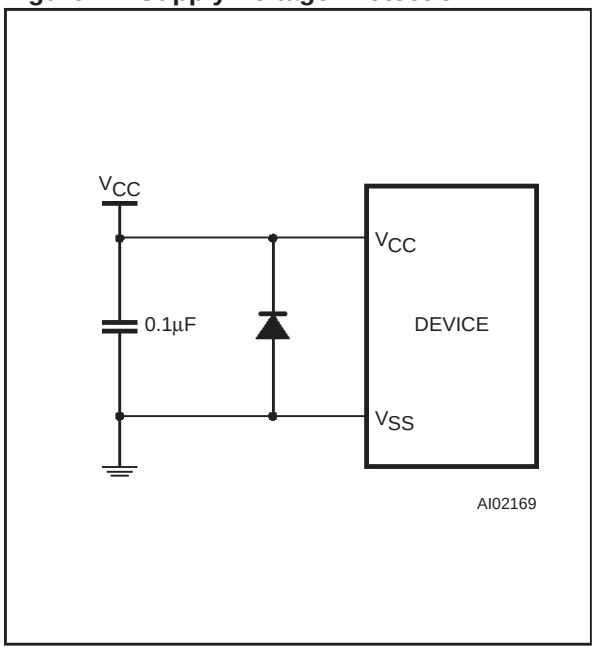
Note: Output Enable ($\overline{G}$) = High.

Figure 10. Chip Enable Controlled, Write AC Waveforms



Note: Output Enable ($\overline{G}$) = High.

Figure 11. Supply Voltage Protection



DATA RETENTION MODE

With valid V_{CC} applied, the M48Z512A/512AY operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself t_{WP} after V_{CC} falls below V_{PFD}. All outputs become high impedance, and all inputs are treated as "don't care."

If power fail detection occurs during a valid access, the memory cycle continues to completion. If the memory cycle fails to terminate within the time t_{WP}, write protection takes place. When V_{CC} drops below V_{SO}, the control circuit switches power to the internal energy source which preserves data.

The internal coin cell will maintain data in the M48Z512A/512AY after the initial application of V_{CC} for an accumulated period of at least 10 years when V_{CC} is less than V_{SO}. As system power returns and V_{CC} rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}. Write protection continues for t_{ER} after V_{CC} reaches V_{PFD} to allow for processor stabilization. After t_{ER}, normal RAM operation can resume.

For more information on Battery Storage Life refer to the Application Note AN1012.

POWER SUPPLY DECOUPLING and UNDERSHOOT PROTECTION

I_{CC} transients, including those produced by output switching, can produce voltage fluctuations, resulting in spikes on the V_{CC} bus. These transients can be reduced if capacitors are used to store energy, which stabilizes the V_{CC} bus. The energy stored in the bypass capacitors will be released as low going spikes are generated or energy will be absorbed when overshoots occur. A ceramic bypass capacitor value of 0.1µF (as shown in Figure 11) is recommended in order to provide the needed filtering.

In addition to transients that are caused by normal SRAM operation, power cycling can generate negative voltage spikes on V_{CC} that drive it to values below V_{SS} by as much as one Volt. These negative spikes can cause data corruption in the SRAM while in battery backup mode. To protect from these voltage spikes, it is recommeded to connect a schottky diode from V_{CC} to V_{SS} (cathode connected to V_{CC}, anode to V_{SS}). Schottky diode 1N5817 is recommended for through hole and MBRS120T3 is recommended for surface mount.

Table 11. Ordering Information Scheme

Example: M48Z512AY -85 PM 1

Device Type

M48Z

Supply Voltage and Write Protect Voltage

512A = V_{CC} = 4.75V to 5.5V; V_{PFD} = 4.5V to 4.75V

512AY = V_{CC} = 4.5V to 5.5V; V_{PFD} = 4.2V to 4.5V

Speed

-70 = 70ns

-85 = 85ns

Package

PM = PMDIP32

CS (1) = Surface Mount Chip Set solution M40Z300 (SOH28) + M68Z512 (TSOP II 32)

Temperature Range

1 = 0 to 70 °C

9 (2) = Extended Temperature

Note: 1. The SOIC package (SOH28) requires the battery package (SNAPHAT) which is ordered separately under the part number "M4Zxx-BR00SH1" in plastic tube or "M4Zxx-BR00SH1TR" in Tape & Reel form.

2. Contact Sales Offices for availability of Extended Temperature.

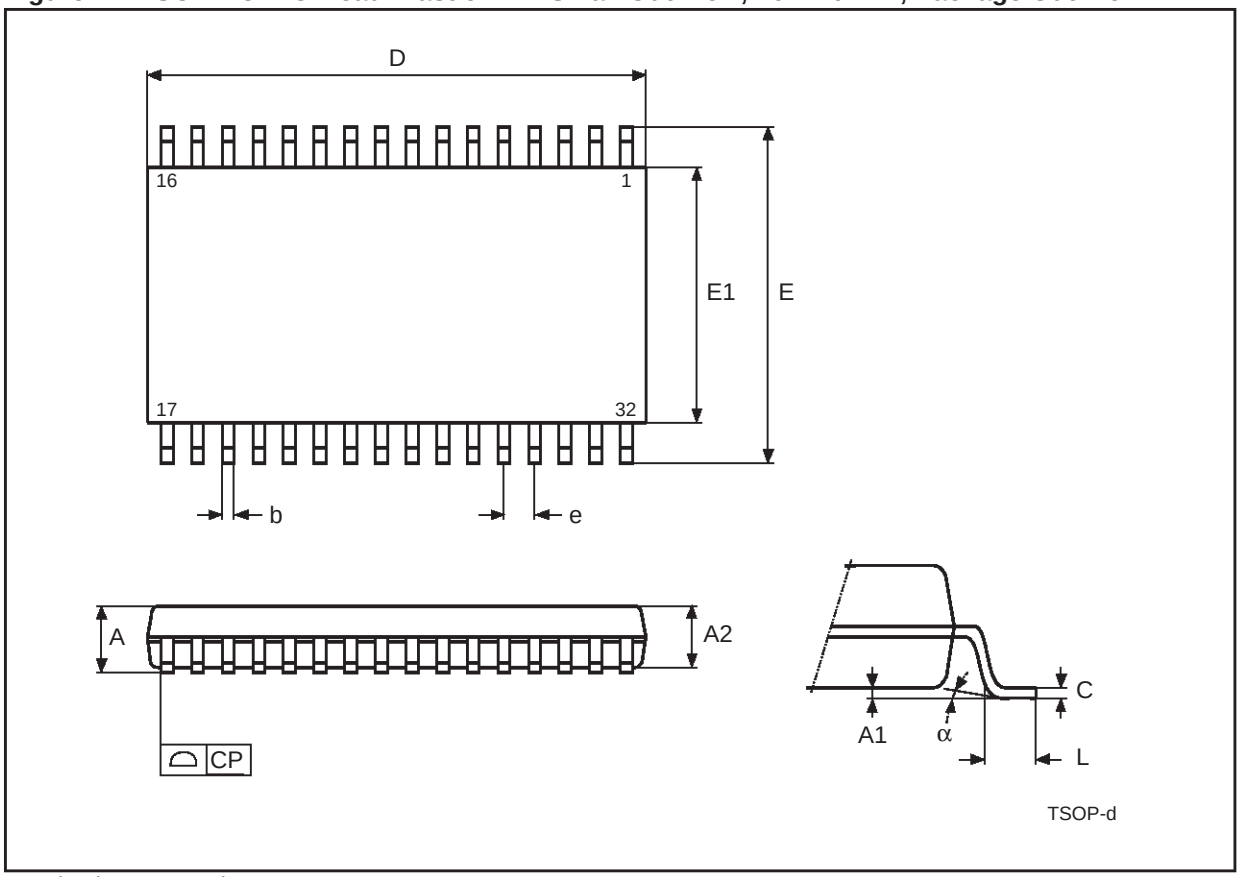
Caution: Do not place the SNAPHAT battery package "M4Zxx-BR00SH1" in conductive foam since this will drain the lithium button-cell battery.

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

Table 12. TSOP II 32 - 32 lead Plastic Thin Small Outline II, 10 x 20 mm, Package Mechanical Data

Symbol	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.15		0.002	0.006
A2		0.95	1.05		0.037	0.041
b		0.30	0.52		0.012	0.020
C		0.12	0.21		0.005	0.008
CP			0.10			0.004
D		20.82	21.08		0.820	0.830
e	1.27	–	–	0.050	–	–
E		11.56	11.96		0.455	0.471
E1		10.03	10.29		0.395	0.405
L		0.40	0.60		0.016	0.024
α		0°	5°		0°	5°
N	32			32		

Figure 12. TSOP II 32 - 32 lead Plastic Thin Small Outline II, 10 x 20 mm, Package Outline

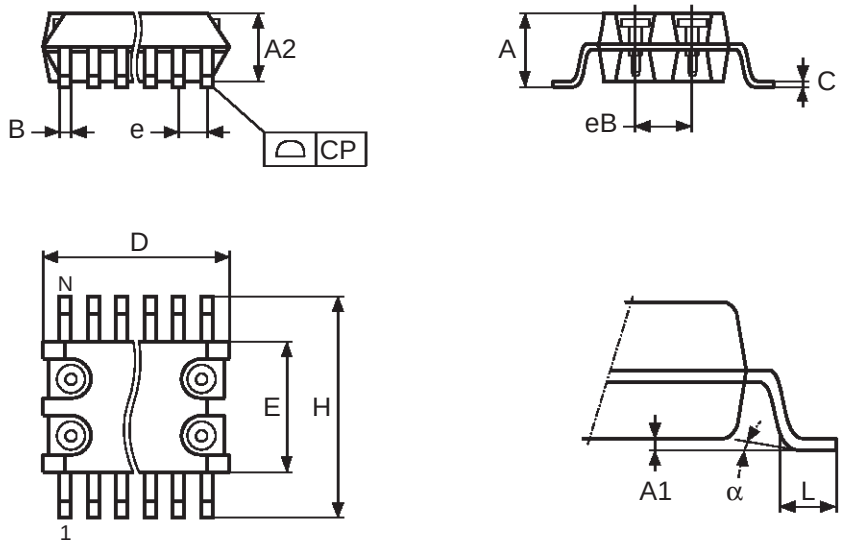


Drawing is not to scale.

Table 13. SOH28 - 28 lead Plastic Small Outline, battery SNAPHAT, Package Mechanical Data

Symbol	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			3.05			0.120
A1		0.05	0.36		0.002	0.014
A2		2.34	2.69		0.092	0.106
B		0.36	0.51		0.014	0.020
C		0.15	0.32		0.006	0.012
D		17.71	18.49		0.697	0.728
E		8.23	8.89		0.324	0.350
e	1.27	–	–	0.050	–	–
eB		3.20	3.61		0.126	0.142
H		11.51	12.70		0.453	0.500
L		0.41	1.27		0.016	0.050
α		0°	8°		0°	8°
N	28			28		
CP			0.10			0.004

Figure 13. SOH28 - 28 lead Plastic Small Outline, battery SNAPHAT, Package Outline



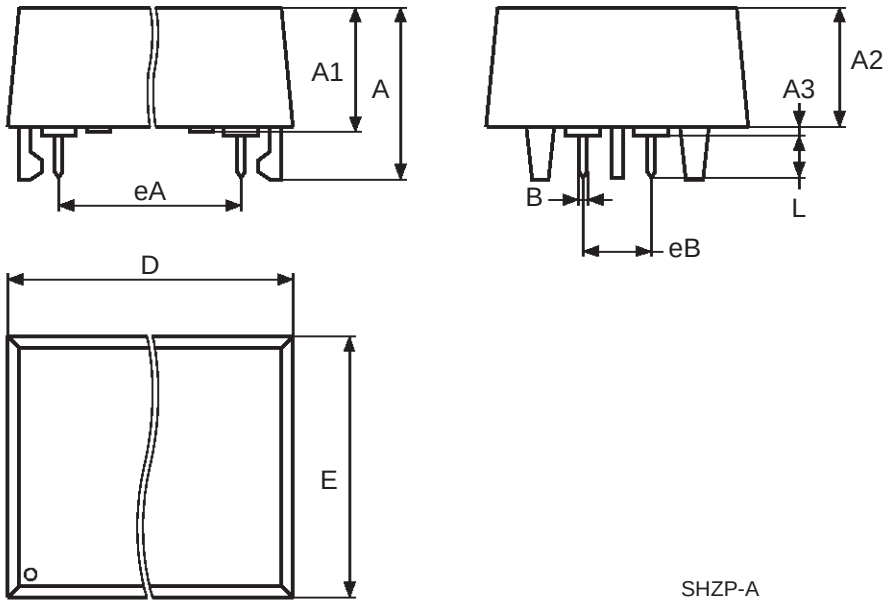
SOH-A

Drawing is not to scale.

Table 14. M4Z32-BR00SH SNAPHAT Housing for 120 mAh Battery, Package Mechanical Data

Symbol	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			10.54			0.415
A1		8.00	8.51		0.315	0.335
A2		7.24	8.00		0.285	0.315
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		17.27	18.03		0.680	0.710
eA		15.55	15.95		0.612	0.628
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

Figure 14. M4Z32-BR00SH SNAPHAT Housing for 120 mAh Battery, Package Outline

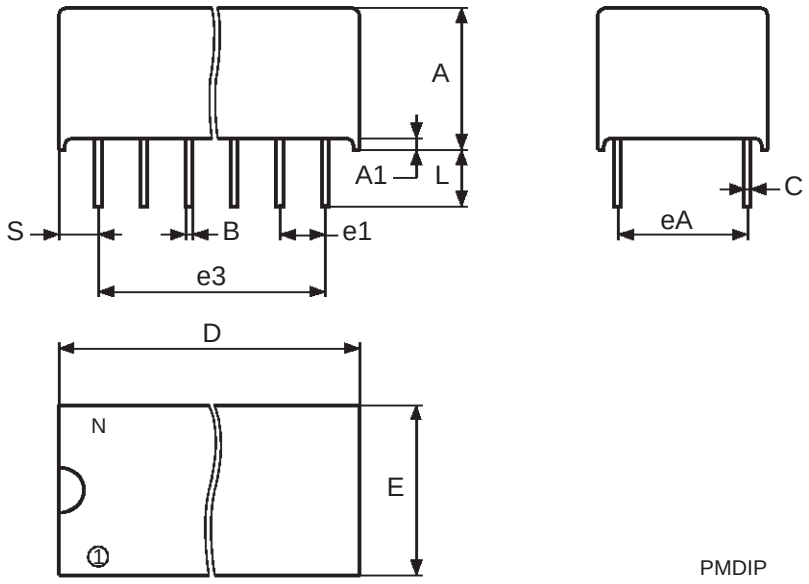


Drawing is not to scale.

Table 15. PMDIP32 - 32 pin Plastic Module DIP, Package Mechanical Data

Symbol	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		9.27	9.52		0.365	0.375
A1		0.38	–		0.015	–
B		0.43	0.59		0.017	0.023
C		0.20	0.33		0.008	0.013
D		42.42	43.18		1.670	1.700
E		18.03	18.80		0.710	0.740
e1		2.29	2.79		0.090	0.110
e3		34.29	41.91		1.350	1.650
eA		14.99	16.00		0.590	0.630
L		3.05	3.81		0.120	0.150
S		1.91	2.79		0.075	0.110
N	32			32		

Figure 15. PMDIP32 - 32 pin Plastic Module DIP, Package Outline



Drawing is not to scale.