

# M52342FP

## PLL-Split VIF/SIF IC

REJ03F0165-0200

Rev.2.00

Jun 14, 2006

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### Description

The M52342FP is IF signal-processing IC for VCRs and TVs. It enables the PLL detection system despite size as small as that of conventional quasi-synchronous VIF/SIF detector, IF/RF AGC, SIF limiter, FM detector, QIF AGC and EQ AMP.

### Features

- Video detection output is 2 V<sub>p-p</sub>. It has built-in EQ AMP.
- The package is a 24-pin flat package, suitable for space saving.
- The video detector uses PLL for full synchronous detection circuit. It produces excellent characteristics of DG, DP, 920 kHz beat, and cross color.
- Dynamic AGC realizes high-speed response with only single filter.
- Video IF and sound IF signal processing are separated from each other. VCO output is used to obtain intercarrier. This PLL-SPLIT method and built-in QIF AGC provide good sound sensitivity and reduces buzz.
- As AFT output voltage uses the APC output voltage, VCO coil is not used.
- Audio FM demodulation uses PLL system, so it has wide frequency range with no external parts and no adjustment.

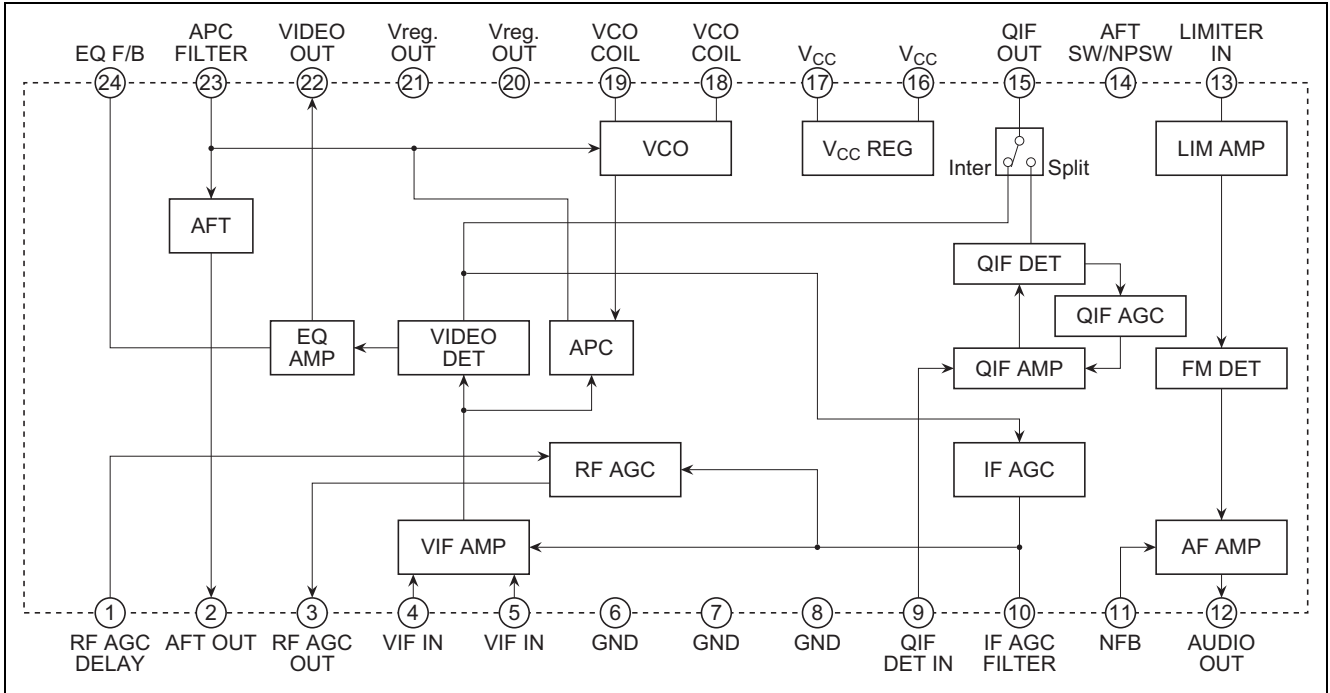
### Application

TV sets, VCR tuners

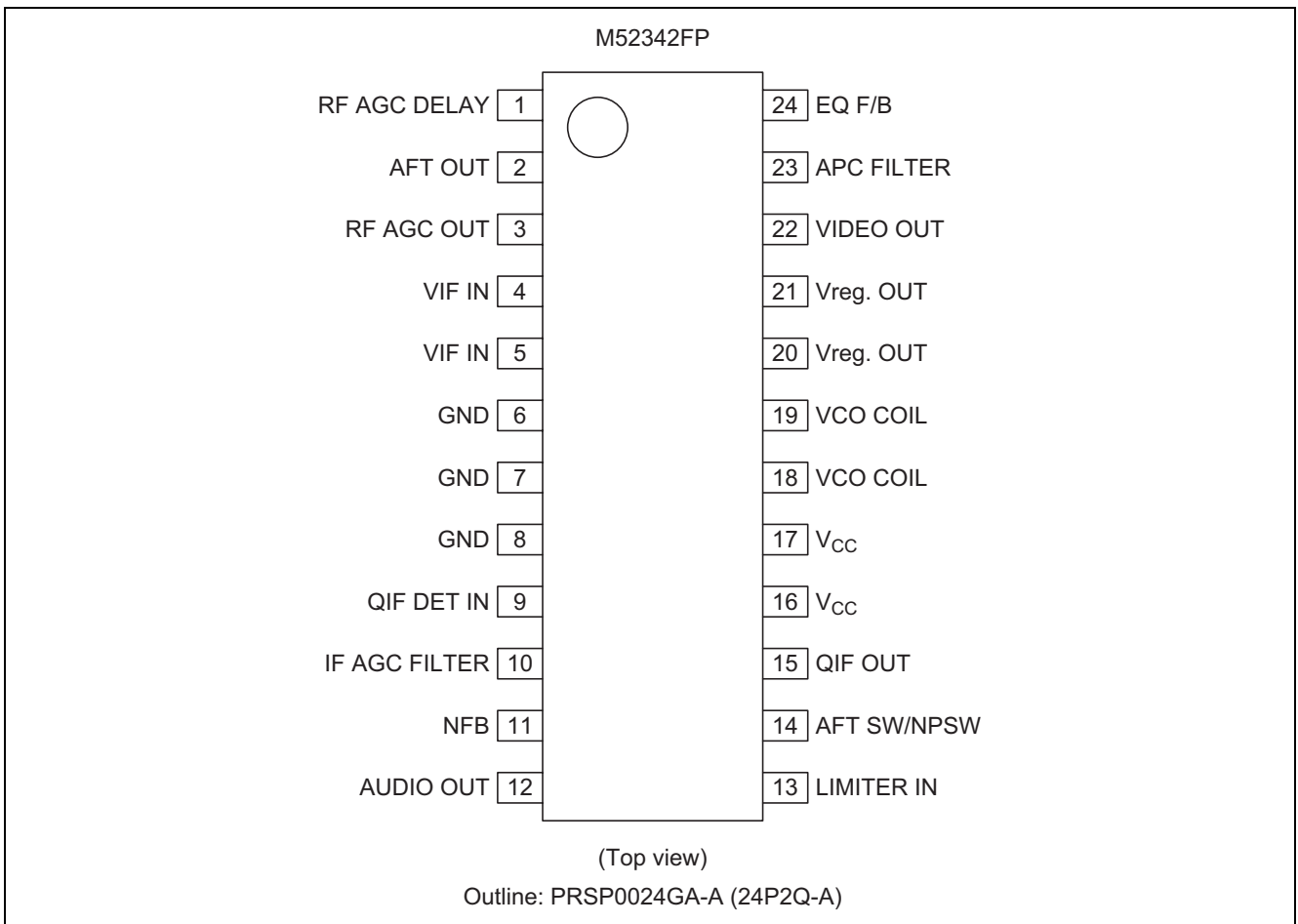
### Recommended Operating Condition

- In case of V<sub>CC</sub> and V<sub>reg</sub>. OUT short
  - Supply voltage range: 4.75 to 5.25 V
  - Recommended supply voltage: 5.0 V
- In case of V<sub>reg</sub>. OUT open
  - Supply voltage range: 8.5 to 12.5 V

### Block Diagram



### Pin Arrangement



## Absolute Maximum Ratings

(Ta = 25°C, surge protection capacitance 200 pF resistance 0, unless otherwise noted)

Item	Symbol	Ratings	Unit	Condition
Supply voltage1	V <sub>CC</sub>	13.2	V	V <sub>CC</sub> and Vreg. OUT is not connected to each other.
Supply voltage Vreg. OUT	Vreg. OUT	6.0	V	V <sub>CC</sub> and Vreg. OUT is not connected to each other.
Power dissipation	Pd	1524	mW	
Operating temperature	T <sub>opr</sub>	-20 to +75	°C	
Storage temperature	T <sub>stg</sub>	-40 to +150	°C	
Surge voltage resistance	Surge	200	V	

## Ambient Operating Condition

(Ta = 25°C, unless otherwise noted)

Supply Voltage	Supply Voltage Range	Recommended Supply Voltage
In case of V <sub>CC</sub> and Vreg. OUT short	4.75 to 5.25 V	5.0 V
In case of Vreg. OUT open	8.5 to 12.5 V	

## Electrical Characteristics

(V<sub>CC</sub> = 5 V, Ta = 25°C, unless otherwise noted)

Item	Symbol	Test Circuit	Test Point	Input Point	Input SG	Limits			Unit	Test Conditions			
						Min.	Typ.	Max.		External Power Supply			Switches set to position 1 unless otherwise indicated
										V7	V8	V12	
VIF section													
Circuit current1 V <sub>CC</sub> = 5V	I <sub>CC1</sub>	1	A	VIF IN	SG1	33	46	59	mA			5	V <sub>CC</sub> = 5V SW17 = 1, SW14 = 2
Circuit current2 V <sub>CC</sub> = 12V	I <sub>CC2</sub>	1	A	VIF IN	SG1	33	46	59	mA			5	V <sub>CC</sub> = 12V SW14 = SW17 = 2
Vreg voltage	V <sub>CC2</sub>	1	TP17			4.60	4.95	5.30	V			5	V <sub>CC</sub> = 12V SW7 = 2
Video output DC voltage	V18	1	TP18A			3.2	3.5	3.8	V		0		SW8 = 2
Video output voltage	V <sub>o det</sub>	1	TP18A	VIF IN	SG1	1.8	2.1	2.4	V <sub>P-P</sub>				
Video S/N	Video S/N	1	TP18B	VIF IN	SG2	51	56	—	dB				SW18 = 2
Video band width	BW	1	TP18A	VIF IN	SG3	7.0	9.0	—	MHz		Variable		SW8 = 2
Input sensitivity	V <sub>IN MIN</sub>	1	TP18A	VIF IN	SG4	—	48	52	dBμ				

(V<sub>CC</sub> = 5 V, T<sub>a</sub> = 25°C, unless otherwise noted)

Item	Symbol	Test Circuit	Test Point	Input Point	Input SG	Limits			Unit	Test Conditions			Switches set to position 1 unless otherwise indicated	
						Min.	Typ.	Max.		External Power Supply				
										V7	V8	V12		
Maximum allowable input	VIN MAX	1	TP18A	VIF IN	SG5	101	105	—	dBμ					
AGC control range input	GR					50	57	—	dB					
IF AGC voltage	V8	1	TP8	VIF IN	SG6	2.9	3.2	3.5	V					
Maximum IF AGC voltage	V8H	1	TP8			4.0	4.4	—	V					
Minimum IF AGC voltage	V8L	1	TP8	VIF IN	SG7	2.2	2.4	2.6	V					
Maximum RF AGC voltage	V3H	1	TP3	VIF IN	SG6	4.2	4.7	—	V					
						8.0	8.9	—						(V <sub>CC</sub> = 9V)
						11.0	11.9	—						(V <sub>CC</sub> = 12V)
Minimum RF AGC voltage	V3L	1	TP3	VIF IN	SG7	—	0.1	0.5	V					
						—	0.2	0.7						(V <sub>CC</sub> = 9V)
						—	0.2	0.7						(V <sub>CC</sub> = 12V)
RF AGC operation voltage	V3	1	TP3	VIF IN	SG8	89	92	95	dBμ					
Capture range U	CL-U	1	TP18A	VIF IN	SG9	1.0	1.7	—	MHz					
Capture range L	CL-L	1	TP18A	VIF IN	SG9	1.8	2.4	—	MHz					
Capture range T	CL-T	1				3.1	4.1	—	MHz					
AFT sensitivity		1	TP2	VIF IN	SG10	20	30	60	mV/ kHz			3.3		
AFT maximum voltage	V2H	1	TP2	VIF IN	SG10	3.85	4.15	—	V			3.3		
						7.7	8.1	—						(V <sub>CC</sub> = 9V)
						10.7	11.1	—						(V <sub>CC</sub> = 12V)
AFT minimum voltage	V2L	1	TP2	VIF IN	SG10	—	0.7	1.2	V			3.3		
						—	0.7	1.2						(V <sub>CC</sub> = 9V)
						—	0.7	1.2						(V <sub>CC</sub> = 12V)
AFT defeat1	AFT def1	1	TP2	VIF IN	SG10	2.2	2.5	2.8	V			1.6 5		
						4.1	4.5	4.9						(V <sub>CC</sub> = 9V)
						5.5	6.0	6.5						(V <sub>CC</sub> = 12V)
AFT defeat2	AFT def2	1	TP2	VIF IN	SG10	2.2	2.5	2.8	V			4.6		
						4.1	4.5	4.9						(V <sub>CC</sub> = 9V)
						5.5	6.0	6.5						(V <sub>CC</sub> = 12V)
Inter modulation	IM	1	TP18A	VIF IN	SG11	35	40	—	dB		Variable		SW8 = 2	

(V<sub>CC</sub> = 5 V, T<sub>a</sub> = 25°C, unless otherwise noted)

Item	Symbol	Test Circuit	Test Point	Input Point	Input SG	Limits			Unit	Test Conditions			Switches set to position 1 unless otherwise indicated
						Min.	Typ.	Max.		External Power Supply			
										V7	V8	V12	
Differential gain	DG	1	TP18A	VIF IN	SG12	—	2	5	%				
Differential phase	DP	1	TP18A	VIF IN	SG12	—	2	5	deg				
Sync. tip level	V18 SYNC	1	TP18A	VIF IN	SG2	0.85	1.15	1.45	V				
VIF input resistor	RINV	2	TP4			—	1.2	—	kΩ				
VIF input capacitance	CINV	2	TP4			—	5	—	pF				
SIF section													
QIF output1	QIF1	1	TP13	VIF IN QIF IN	SG2 SG13	94	100	106	dBμ				
QIF output2	QIF2	1	TP13	VIF IN QIF IN	SG2 SG14	94	100	106	dBμ				
SIF detection output	Vos	1	TP13	VIF IN	SG15	94	100	106	dBμ	0		5	SW7 = 2
AF output DC voltage	V1	1	TP10	SIF IN	SG20	1.6	2.2	2.8	V			5	
AF output (4.5MHz)	VOAF1	1	TP10	SIF IN	SG16	400	560	800	mVrms			5	
AF output (5.5MHz)	VOAF2	1	TP10	SIF IN	SG21	320	450	630	mVrms			0	
AF output distortion (4.5MHz)	THD AF1	1	TP10	SIF IN	SG16	—	0.2	0.9	%			5	
AF output distortion (5.5MHz)	THD AF2	1	TP10	SIF IN	SG21	—	0.2	0.9	%			0	
Limiting sensitivity (4.5MHz)	LIM1	1	TP10	SIF IN	SG17 SG19	—	42	55	dBμ			5	
Limiting sensitivity (5.5MHz)	LIM2	1	TP10	SIF IN	SG22 SG24	—	42	55	dBμ			0	
AM rejection (4.5MHz)	AMR1	1	TP10	SIF IN	SG18	55	62	—	dB			5	
AM rejection (5.5MHz)	AMR2	1	TP10	SIF IN	SG23	55	64	—	dB			0	
AF S/N (4.5MHz)	AF S/N1	1	TP10	SIF IN	SG20	55	62	—	dB			5	
AF S/N (5.5MHz)	AF S/N2	1	TP10	SIF IN	SG25	55	64	—	dB			0	

(V<sub>CC</sub> = 5 V, T<sub>a</sub> = 25°C, unless otherwise noted)

Item	Symbol	Test Circuit	Test Point	Input Point	Input SG	Limits			Unit	Test Conditions			
						Min.	Typ.	Max.		External Power Supply			Switches set to position 1 unless otherwise indicated
										V7	V8	V12	
SIF input resistance	RINS	2	TP7			—	1.5	—	kΩ				
SIF input capacitance	CINS	2	TP7			—	4	—	pF				
Control section													
QIF control	C <sub>QIF</sub>	1	TP7			—	0.7	1.0	V	Variable		SW7 = 2	

### Pin 14 Voltage Control

Pin 14 Voltage (V)		AF	AFT
0 to 2.3	0 to 0.6	PAL	NORMAL
	1.0 to 2.3		DEFEAT
2.7 to 5.0	2.7 to 4.0	NTSC	NORMAL
	4.4 to 5.0		DEFEAT

### Electrical Characteristics Test Method

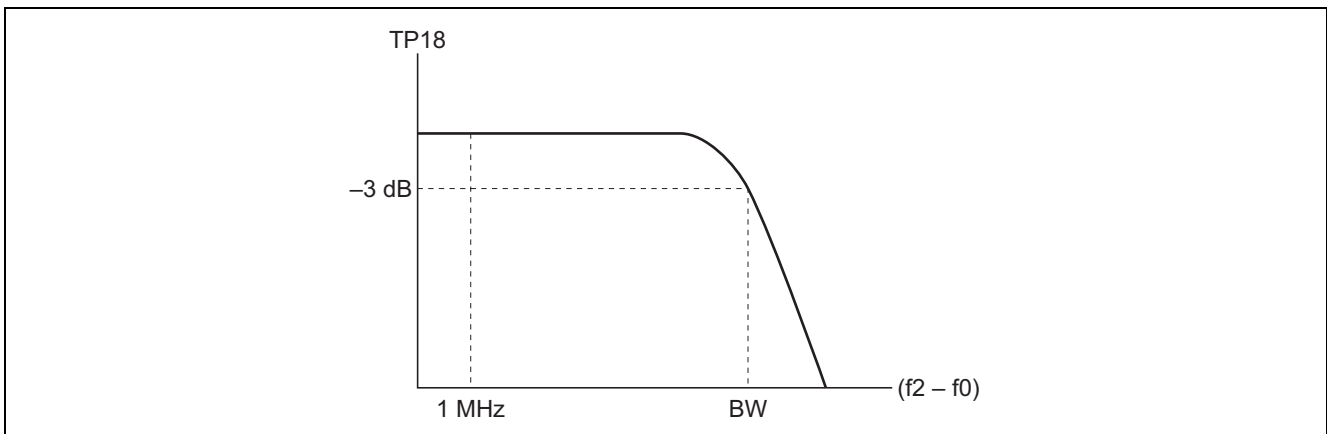
#### Video S/N

Input SG2 into VIF IN and measure the video out (Pin 22) noise in r.m.s at TP22B through a 5 MHz (−3 dB) L.P.F.

$$S/N = 20 \log \left( \frac{0.7 \cdot V_o \text{ det}}{\text{NOISE}} \right) \text{ (dB)}$$

#### BW Video Band Width

1. Measure the 1MHz component level of EQ output TP22A with a spectrum analyzer when SG3 (f<sub>2</sub> = 57.75 MHz) is input into VIF IN. At that time, measure the voltage at TP10 with SW10, set to position 2, and then fix V10 at that voltage.
2. Reduce f<sub>2</sub> and measure the value of (f<sub>2</sub> − f<sub>0</sub>) when the (f<sub>2</sub> − f<sub>0</sub>) component level reaches −3 dB from the 1 MHz component level as shown below.



### VIN MIN Input sensitivity

Input SG4 ( $V_i = 90 \text{ dB}\mu$ ) into VIF IN, and then gradually reduce  $V_i$  and measure the input level when the 20 kHz component of EQ output TP22A reaches  $-3 \text{ dB}$  from  $V_o \text{ det}$  level.

### VIN MAX Maximum Allowable Input

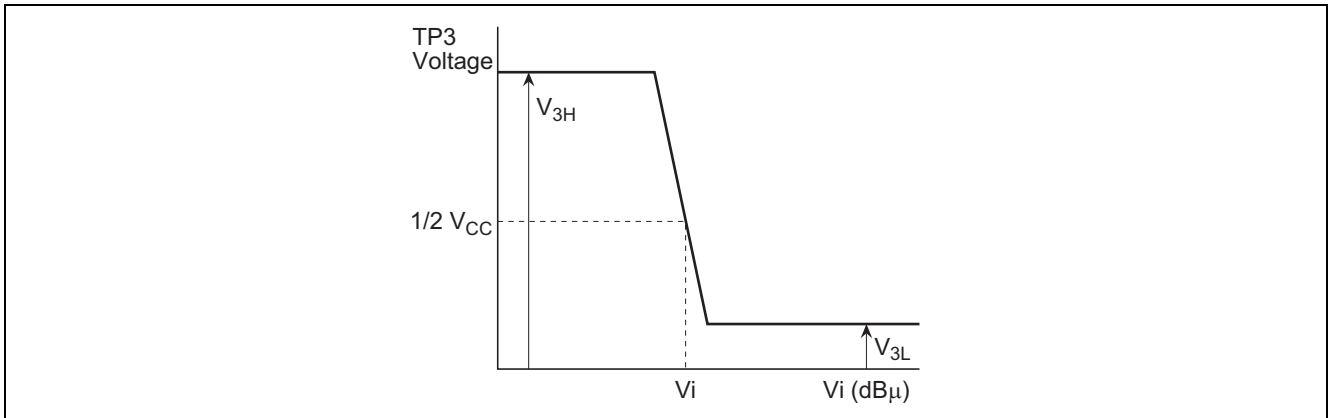
1. Input SG5 ( $V_i = 90 \text{ dB}\mu$ ) into VIF IN, and measure the level of the 20 kHz component of EQ output.
2. Gradually increase the  $V_i$  of SG and measure the input level when the output reaches  $-3 \text{ dB}$ .

### GR AGC Control Range

$$\text{GR} = \text{VIN MAX} - \text{VIN MIN} \text{ (dB)}$$

### V3 RF AGC Operating Voltage

Input SG8 into VIF IN, and gradually reduce  $V_i$  and then measure the input level when RF AGC output TP3 reaches  $1/2 V_{CC}$ , as shown below.



### CL-U Capture Range

1. Increase the frequency of SG9 until the VCO is out of locked-oscillation.
2. Decrease the frequency of SG9 and measure the frequency  $f_U$  when the VCO locks.

$$\text{CL-U} = f_U - 58.75 \text{ (MHz)}$$

### CL-L Capture Range

1. Decrease the frequency of SG9 until the VCO is out of locked-oscillation.
2. Increase the frequency of SG9 and measure the frequency  $f_L$  when the VCO locks.

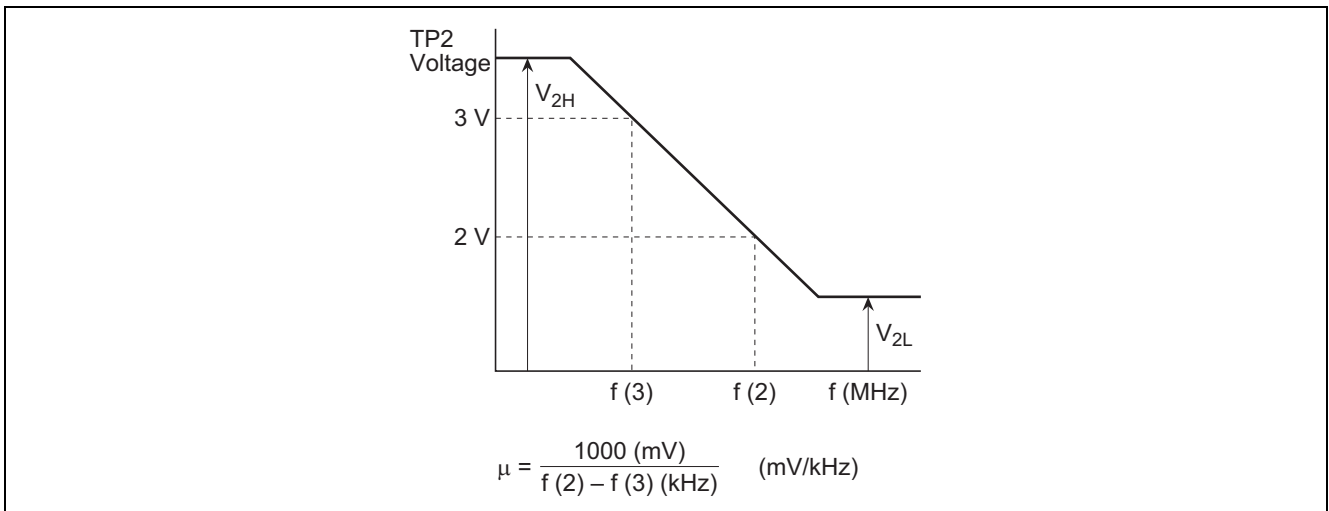
$$\text{CL-L} = 58.75 - f_L \text{ (MHz)}$$

### CL-T Capture Range

$$\text{CL-T} = \text{CL-U} + \text{CL-L} \text{ (MHz)}$$

### $\mu$ AFT Sensitivity, $V_{2H}$ Maximum AFT Voltage, $V_{2L}$ Minimum AFT Voltage

1. Input SG10 into VIF IN, and set the frequency of SG10 so that the voltage of AFT output TP2 is 3 V. This frequency is named  $f(3)$ .
2. Set the frequency of SG10 so that the AFT output voltage is 2 V. This frequency is named  $f(2)$ .
3. IN the graph, maximum and minimum DC voltage are  $V_{2H}$  and  $V_{2L}$ , respectively.

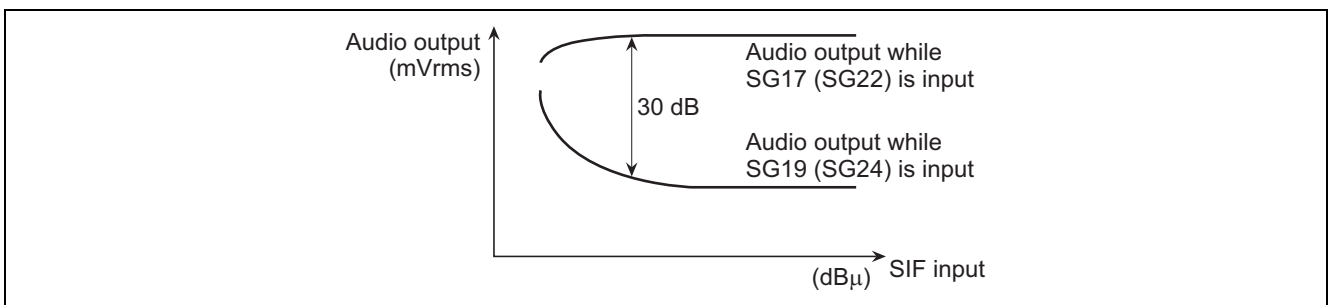


### IM Intermodulation

1. Input SG11 into VIF IN, and measure EQ output TP22A with an oscilloscope.
2. Adjust AGC filter voltage V10 so that the minimum DC level of the output waveform is 1.0 V.
3. At this time, measure, TP22A with a spectrum analyzer.  
The intermodulation is defined as a difference between 920 kHz and 3.58 MHz frequency components.

### LIM Limiting Sensitivity

1. Input SG17 (SG22) into SIF input, and measure the 400 Hz component level of AF output TP12.
2. Input SG19 (SG24) into SIF input, and measure the 400 Hz component level of AF output TP12.
3. The input limiting sensitivity is defined as the input level when a difference between each 400 Hz components of audio output (TP12) is 30 dB, as shown below.



### AMR AM Rejection

1. Input SG18 (SG23) into SIF input, and measure the output level of AF output TP12. This level is named VAM.
2. AMR is;

$$\text{AMR} = 20 \log \left( \frac{V_{oAF} \text{ (mVrms)}}{V_{AM} \text{ (mVrms)}} \right) \quad (\text{dB})$$



**AF S/N**

1. Input SG19 (SG24) into SIF input, and measure the output noise level of AF output TP1. This level is named VN.
2. S/N is;

$$S/N = 20 \log \left( \frac{V_{oAF} \text{ (mVrms)}}{V_N \text{ (mVrms)}} \right) \text{ (dB)}$$

**C<sub>QIF</sub> QIF Control**

Lower the voltage of V9, and measure the voltage of V9 when DC voltage of TP15 begins to change.

**The Note in The System Setup**

M52342FP has 2 power supply pins of V<sub>CC</sub> (pin 16, 17) and V<sub>reg. OUT</sub> (pin 20, 21) . V<sub>CC</sub> is for AFT output, RF AGC output circuits and 5 V regulated power circuit and V<sub>reg. OUT</sub> is for the other circuit blocks.

In case M52342FP is used together with other ICs like VIF operating at more than 5 V, the same supply voltage as that of connected ICs is applied to V<sub>CC</sub> and V<sub>reg. OUT</sub> is opened. The other circuit blocks, connected to V<sub>reg. OUT</sub> are powered by internal 5 V regulated power supply.

In case the connecting ICs are operated at 5 V, 5 V is supplied to both V<sub>CC</sub> and V<sub>reg. OUT</sub>.

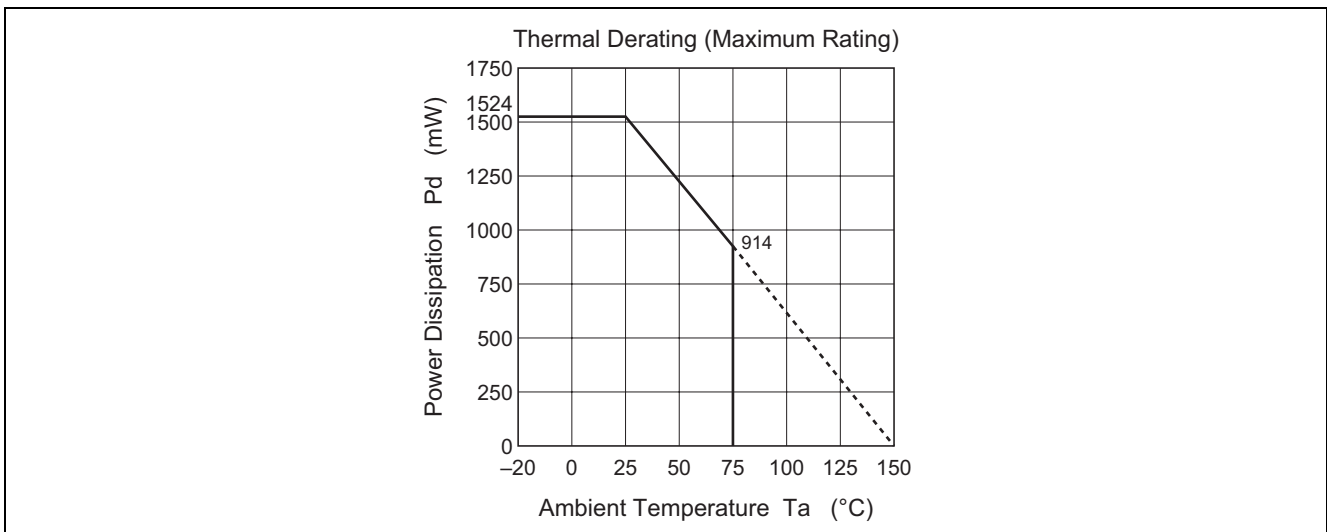
**Logic Table**

		AF	AFT
10 k "H"	20 k "H"	NTSC	DEFEAT
	20 k "L"		NORMAL
10 k "L"	20 k "H"	PAL	DEFEAT
	20 k "L"		NORMAL

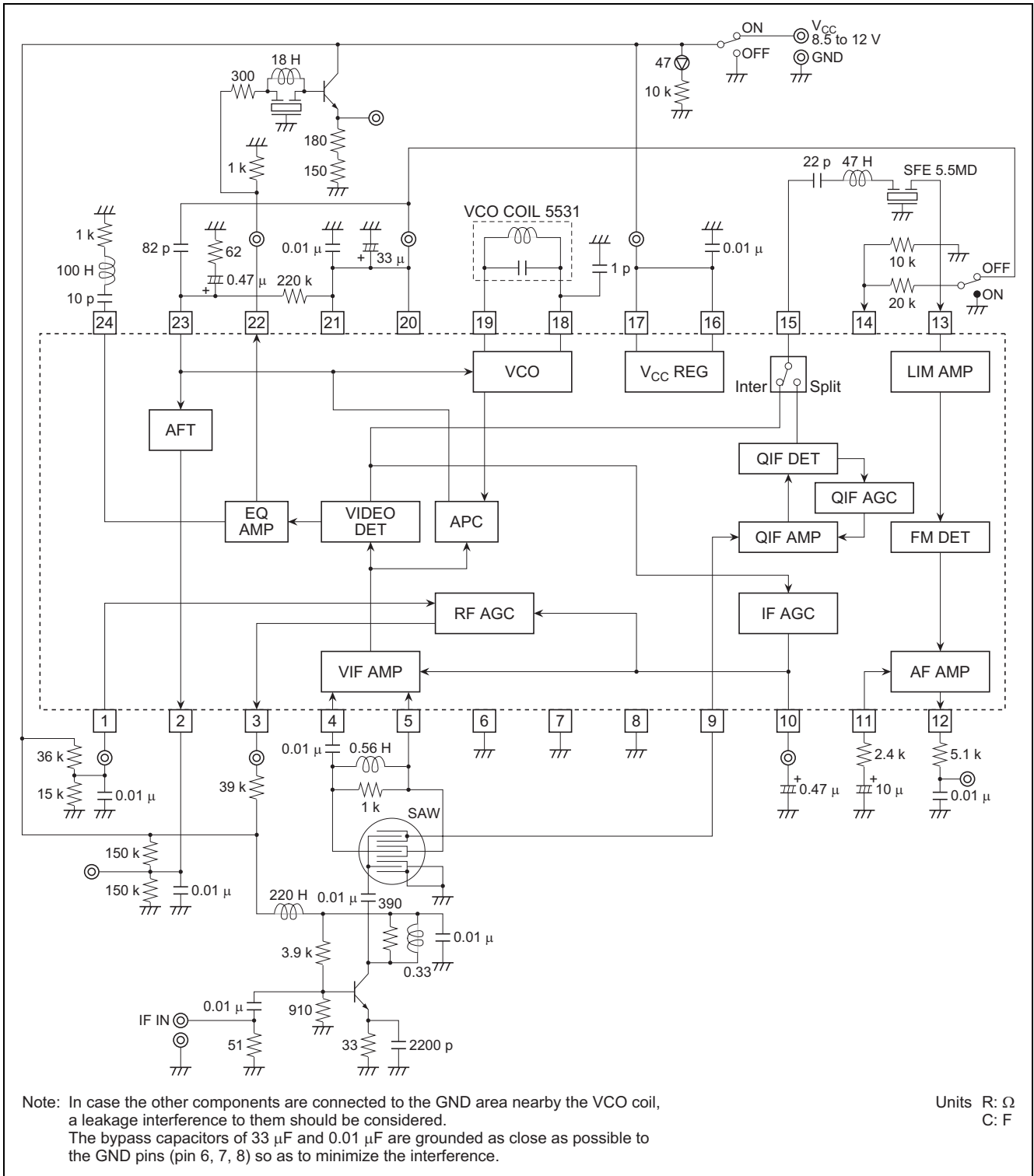
## Input Signal

SG No.	Signals (50 Ω Termination)
1	$f_0 = 58.75$ MHz AM 20 kHz 77.8% 90 dB $\mu$
2	$f_0 = 58.75$ MHz 90 dB $\mu$ CW
3	$f_1 = 58.75$ MHz 90 dB $\mu$ CW (Mixed signal) $f_2 =$ Frequency variable 70 dB $\mu$ CW (Mixed signal)
4	$f_0 = 58.75$ MHz AM 20 kHz 77.8% level variable
5	$f_0 = 58.75$ MHz AM 20 kHz 14.0% level variable
6	$f_0 = 58.75$ MHz 80 dB $\mu$ CW
7	$f_0 = 58.75$ MHz 110 dB $\mu$ CW
8	$f_0 = 58.75$ MHz CW level variable
9	$f_0 =$ variable AM 20 kHz 77.8% 90dB $\mu$
10	$f_0 =$ variable 90dB $\mu$ CW
11	$f_1 = 58.75$ MHz 90 dB $\mu$ CW (Mixed signal) $f_2 = 55.17$ MHz 80 dB $\mu$ CW (Mixed signal) $f_3 = 54.25$ MHz 80 dB $\mu$ CW (Mixed signal)
12	$f_0 = 58.75$ MHz 87.5% TV modulation ten-step waveform Sync tip level 90 dB $\mu$
13	$f_1 = 54.25$ MHz 95 dB $\mu$ CW
14	$f_1 = 54.25$ MHz 75 dB $\mu$ CW
15	$f_1 = 58.75$ MHz 90 dB $\mu$ CW (Mixed signal) $f_2 = 54.25$ MHz 70 dB $\mu$ CW (Mixed signal)
16	$f_0 = 4.5$ MHz 90 dB $\mu$ FM 400 Hz $\pm$ 25 kHz dev
17	$f_0 = 4.5$ MHz FM 400 Hz $\pm$ 25 kHz dev level variable
18	$f_0 = 4.5$ MHz 90 dB $\mu$ AM 400 Hz 30%
19	$f_0 = 4.5$ MHz 90dB $\mu$ CW
20	$f_0 = 4.5$ MHz CW level variable
21	$f_0 = 5.5$ MHz 90dB $\mu$ FM 400 Hz $\pm$ 50 kHz dev
22	$f_0 = 5.5$ MHz FM 400 Hz $\pm$ 50 kHz dev level variable
23	$f_0 = 5.5$ MHz 90 dB $\mu$ AM 400 Hz 30%
24	$f_0 = 5.5$ MHz 90dB $\mu$ CW
25	$f_0 = 5.5$ MHz CW level variable

## Typical Characteristics

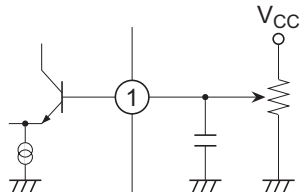


Typical Application Example (for 38.9 MHz Split)



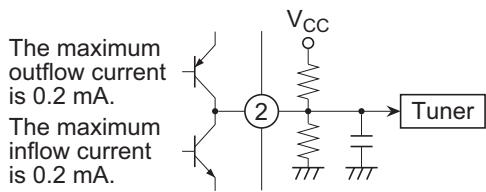
## Pin Description

### Pin 1 (RF AGC DELAY)



An applied voltage to the pin 1 is for changing a RF AGC delay point.

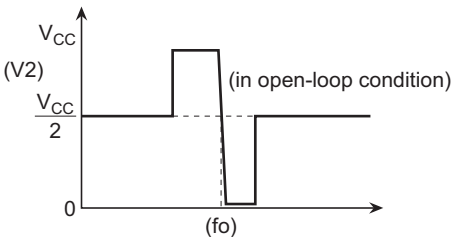
### Pin 2 (AFT OUT)



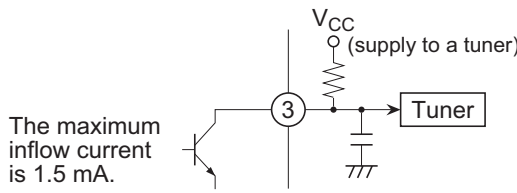
The maximum outflow current is 0.2 mA.  
The maximum inflow current is 0.2 mA.

Since an AFT output is provided by a high impedance source, the detection sensitivity can be set by an external resistor.

The muting operation will be on in following two cases;  
1) the APC is out of locking,  
2) the video output becomes small enough in a weak electric field.

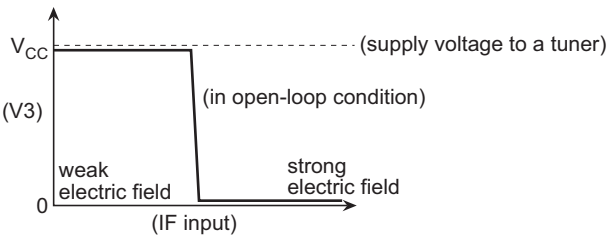


### Pin 3 (RF AGC OUT)



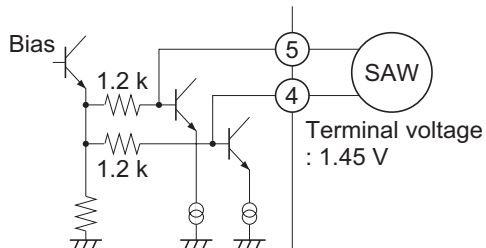
The maximum inflow current is 1.5 mA.

A current mode output is available in the reverse AGC operation.  
The fluctuation of a bottom voltage is made small by loading higher impedance for a deep saturation.



Note: Connecting a nonpolarity capacitor of 1  $\mu$ F between pin1 and pin3 improves AGC operating speed. In that case, the capacitors between pin1/pin3 and ground should be removed.

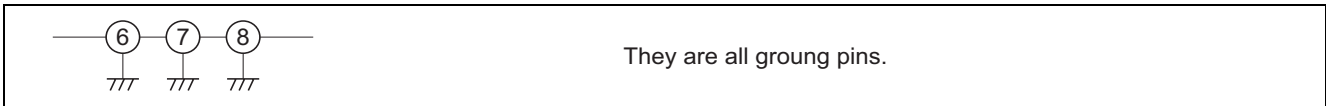
### Pin 4, Pin 5 (VIF IN)



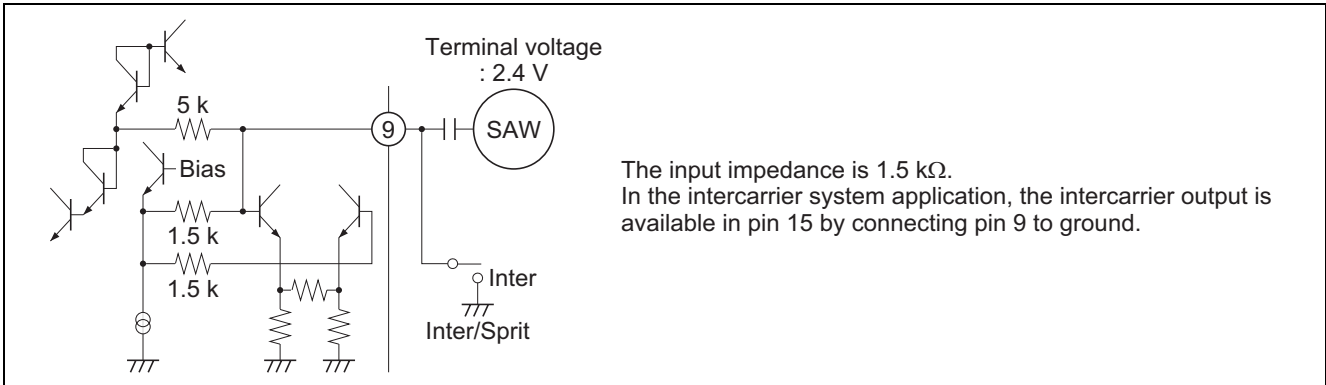
Terminal voltage : 1.45 V

It should be designed considering careful impedance matching with the SAW filter.

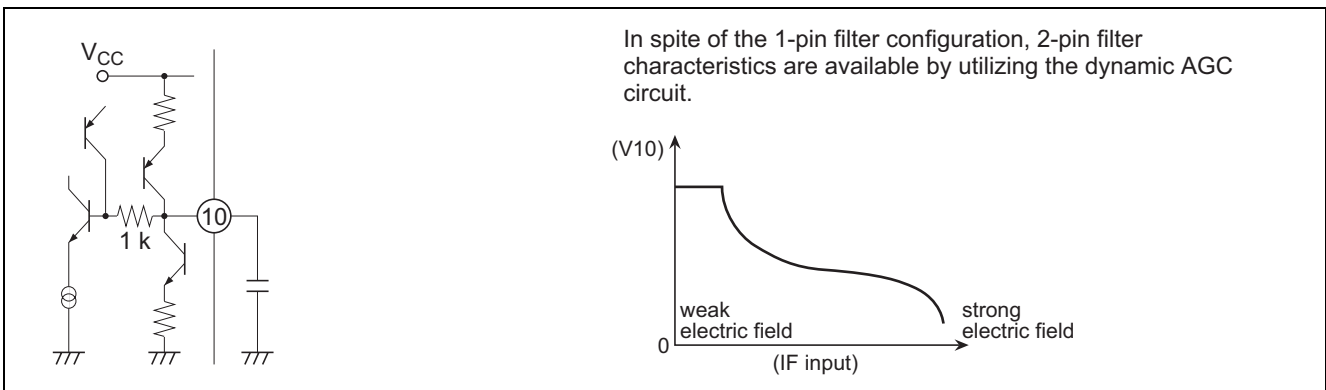
**Pin 6, Pin 7, Pin 8 (GND)**



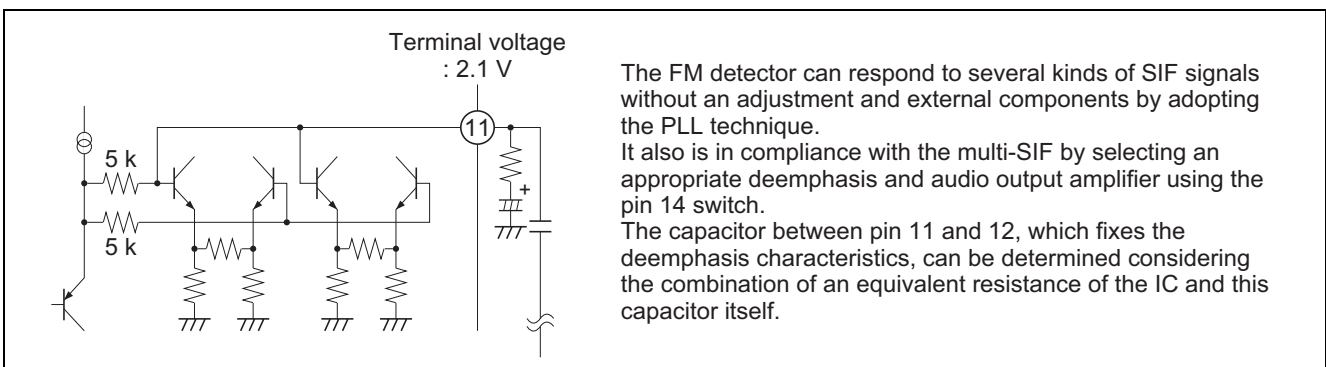
**Pin 9 (QIF DET IN)**



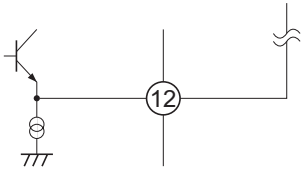
**Pin 10 (IF AGC FILTER)**



**Pin 11 (NFB)**



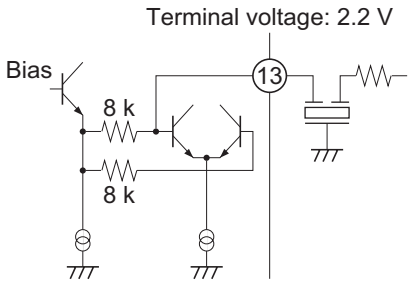
**Pin 12 (AUDIO OUT)**



Terminal voltage: 2.2 V

In the 4.5 MHz application, the internal voltage gain is increased by 6-dB in comparison with the other applications and then the signals are delivered through an emitter follower.

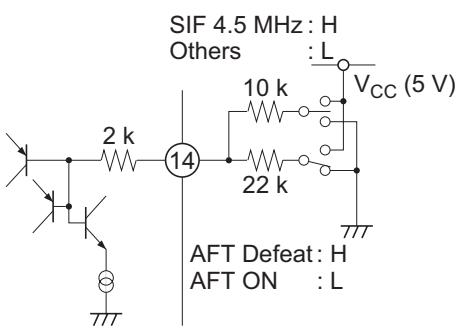
**Pin 13 (LIMITER IN)**



Terminal voltage: 2.2 V

The input impedance is 8 kΩ.

**Pin 14 (AFT SW/NPSW)**



SIF 4.5 MHz : H  
Others : L

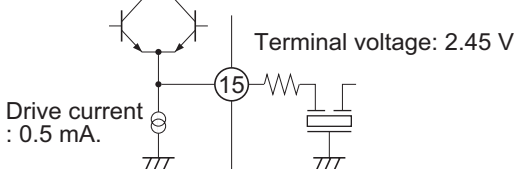
AFT Defeat : H  
AFT ON : L

It works as a switch by connecting the resistor to 5 V (High) or GND (Low), alternately.

10k	20k	AF AMP	AFT	Pin 14 Applied Voltage
H	H	4.5 MHz	Defeat	4.4 to 5.0 V
H	L	4.5 MHz	Normal	2.7 to 4.0 V
L	H	Other	Defeat	1.0 to 2.3 V
L	L	Other	Normal	0 to 0.6 V

The terminal voltage is set by the external resistors because of an open base input.

**Pin 15 (QIF OUT)**

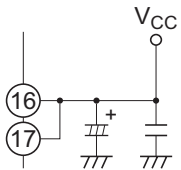


Terminal voltage: 2.45 V

Drive current : 0.5 mA.

In both the split and intercarrier system, the carrier signal to SIF provided from pin 15 through an emitter follower.

**Pin 16, Pin 17 (V<sub>CC</sub>)**



The recommended supply voltage is 5 V or 9 to 12 V. In the case of 5 V supply, these pins should be tied to pin 20 and pin 21. In the case of 9 to 12 V supply, a regulated output of 5 V are available in pin 20 and pin 21.

**Pin 18, Pin 19 (VCO COIL)**

Connecting a tuning coil and capacitor to these pins enables an oscillation. The tuning capacitor of about 30 pF is recommended. The oscillation frequency is tuned in  $f_0$ . In the actual adjustment, the coil is tuned so that the AFT voltage is reached to  $V_{CC}/2$  with  $f_0$  as an input. The printed pattern around these pins should be designed carefully to prevent an pull-in error of VCO, caused by the leakage interference from the large signal level oscillator to adjacent pins. The interconnection also should be designed as short as possible.

**Pin 20, Pin 21 (Vreg. OUT)**

It is a regulated 5 V output which has current drive capability of approximately 15 mA.

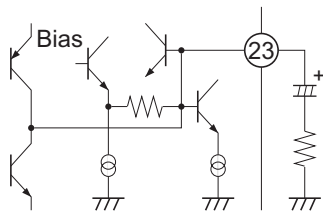
**Pin 22 (VIDEO OUT)**

An output amplitude is positive  $2 V_{P-P}$  in the case of 87.5% video modulation.

Internal driving current: 3 mA

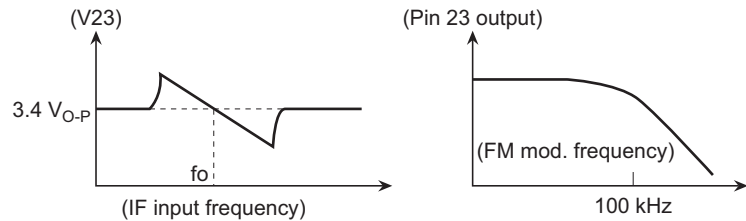
1.1  $V_{O-P}$

## Pin 23 (APC FILTER)

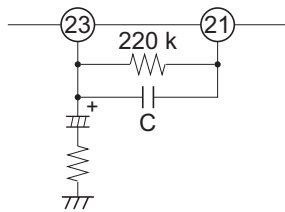


In the locked state, the cut-off frequency of the filter is adjusted effectively by an external resistor so that it will be in the range of around 30 to 200 kHz.

In case the cut-off frequency is lower, the pull-in speed becomes slow. On the other hand, a higher cut-off frequency widens the pull-in range and bandwidth, which results in a degradation in the S/N ratio. So, in the actual TV system design, the appropriate constant should be chosen for getting desirable performance considering above conditions.



In the application, an offset between AFT center frequency and VCO free-running frequency, can be improved by connecting a 220 kΩ resistor to  $V_{CC}$  supply (pin 21).



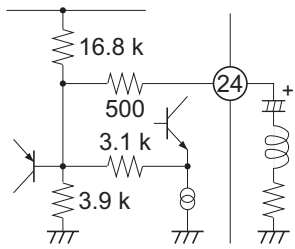
A buzz noise also decreases by connecting a capacitor from pin 23 to  $V_{CC}$  (pin 21) or GND. This effect utilizes the signal interference on the printed circuit board. So, the determination that which connection is effective, to  $V_{CC}$  or GND, is done by a cut and try method.

The capacitor of less than 680 pF, which depends on Q of VCO coil, is recommended to prevent an APC pull-in range from narrowing.

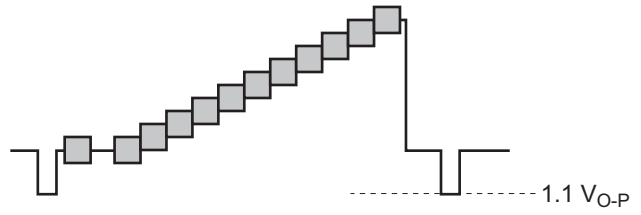
Taking it into consideration in the actual TV set design.



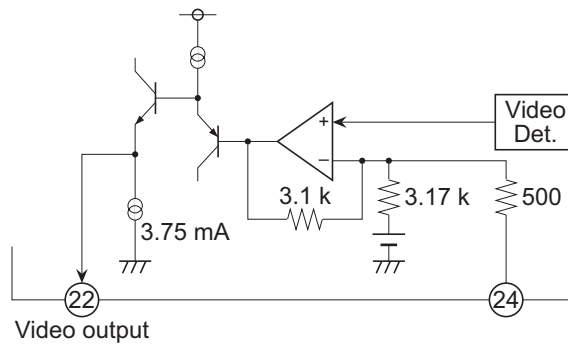
Pin 24 (EQ F/B)



Both the external coil and capacitor determine the frequency response of EQ output. The series connected resistor is for damping.



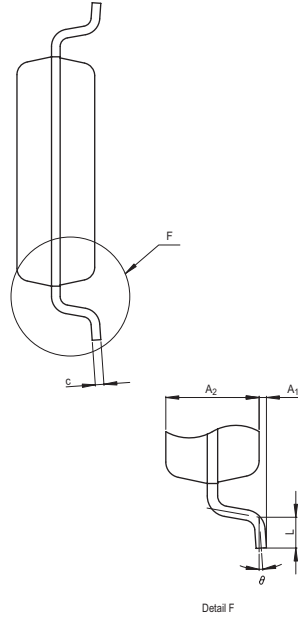
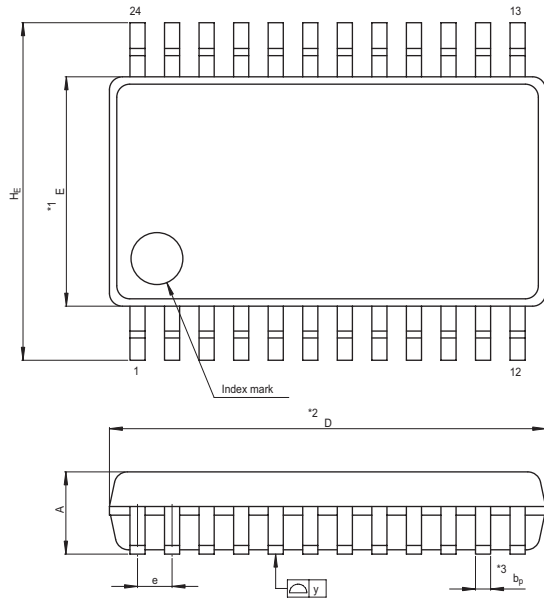
In the intercarrier system, the following phenomenon should be considered; a strong equalization (EQ) enlarge the sound carrier output from pin 22, because the EQ is applied before an audio trap. In that case, the next two solutions are recommended; decrease in S level of SAW, avoiding to peak a sound carrier in EQ.



Circuit Diagram of EQ Amp.

# Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SSOP24-5.3x10.1-0.80	PRSP0024GA-A	24P2Q-A	0.2g



NOTE)  
 1. DIMENSIONS \*\*1" AND \*\*2"  
 DO NOT INCLUDE MOLD FLASH.  
 2. DIMENSION \*\*3" DOES NOT  
 INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	10.0	10.1	10.2
E	5.2	5.3	5.4
A <sub>2</sub>	—	1.8	—
A	—	—	2.1
A <sub>1</sub>	0	0.1	0.2
b <sub>p</sub>	0.3	0.35	0.45
c	0.18	0.2	0.25
θ	0°	—	8°
H <sub>E</sub>	7.5	7.8	8.1
e	0.65	0.8	0.95
y	—	—	0.10
L	0.4	0.6	0.8

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