



# M76DW52003TA M76DW52003BA

## 32Mbit (4Mb x8/ 2Mb x16, Dual Bank, Boot Block) Flash Memory and 4Mbit (256Kb x16) SRAM, Multiple Memory Product

PRELIMINARY DATA

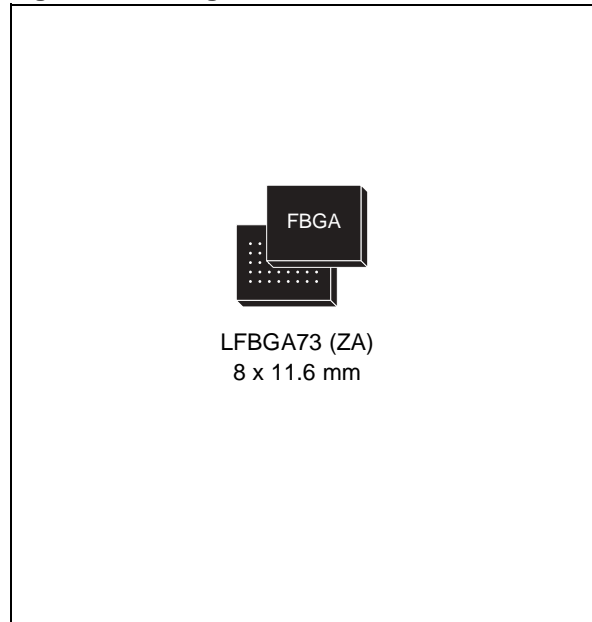
### FEATURES SUMMARY

- MULTIPLE MEMORY PRODUCT
  - 32 Mbit (4Mb x8 or 2Mb x16), Dual Bank, Boot Block, Flash Memory
  - 4 Mbit (256Kb x 16) SRAM
- SUPPLY VOLTAGE
  - $V_{CCF} = 2.7V$  to  $3.3V$
  - $V_{CCS} = 2.7V$  to  $3.3V$
  - $V_{PPF} = 12V$  for Fast Program (optional)
- ACCESS TIME: 70, 90ns
- LOW POWER CONSUMPTION
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 0020h
  - Top Device Code, M76DW52003TA: 225Eh
  - Bottom Device Code, M76DW52003BA: 225Fh

### FLASH MEMORY

- PROGRAMMING TIME
  - $10\mu s$  per Byte/Word typical
  - Double Word/ Quadruple Byte Program
- MEMORY BLOCKS
  - Dual Bank Memory Array: 8Mbit+24Mbit
  - Parameter Blocks (Top or Bottom Location)
- DUAL OPERATIONS
  - Read in one bank while Program or Erase in other
- ERASE SUSPEND and RESUME MODES
  - Read and Program another Block during Erase Suspend
- UNLOCK BYPASS PROGRAM COMMAND
  - Faster Production/Batch Programming
- $V_{PP}/\overline{WP}$  PIN for FAST PROGRAM and WRITE PROTECT
- TEMPORARY BLOCK UNPROTECTION MODE
- COMMON FLASH INTERFACE
  - 64 bit Security Code

Figure 1. Package



- EXTENDED MEMORY BLOCK
    - Extra block used as security block or to store additional information
  - 100,000 PROGRAM/ERASE CYCLES per BLOCK
- ### SRAM
- 4 Mbit (256Kb x 16)
  - ACCESS TIME: 70ns
  - LOW  $V_{CCS}$  DATA RETENTION: 1.5V
  - POWER DOWN FEATURES USING TWO CHIP ENABLE INPUTS

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## M76DW52003TA, M76DW52003BA

### SUMMARY DESCRIPTION

The M76DW52003TA and M76DW52003BA are low voltage Multiple Memory Products that combine two memory devices; a 32 Mbit Dual Bank, boot block Flash memory (M29DW323D(T/B)) and a 4Mbit SRAM. This document should be read in conjunction with the M29DW323D datasheet.

Recommended operating conditions do not allow both the Flash and SRAM devices to be active at the same time.

The memory is offered in an LFBGA73 (8 x 11.6mm, 0.8 mm pitch) package and is supplied with all the bits erased (set to '1').

Figure 2. Logic Diagram

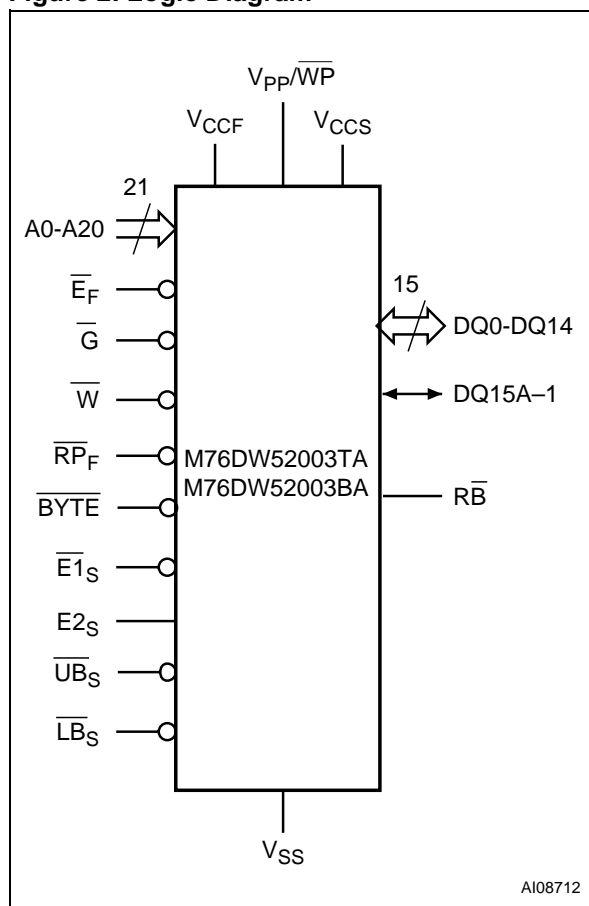
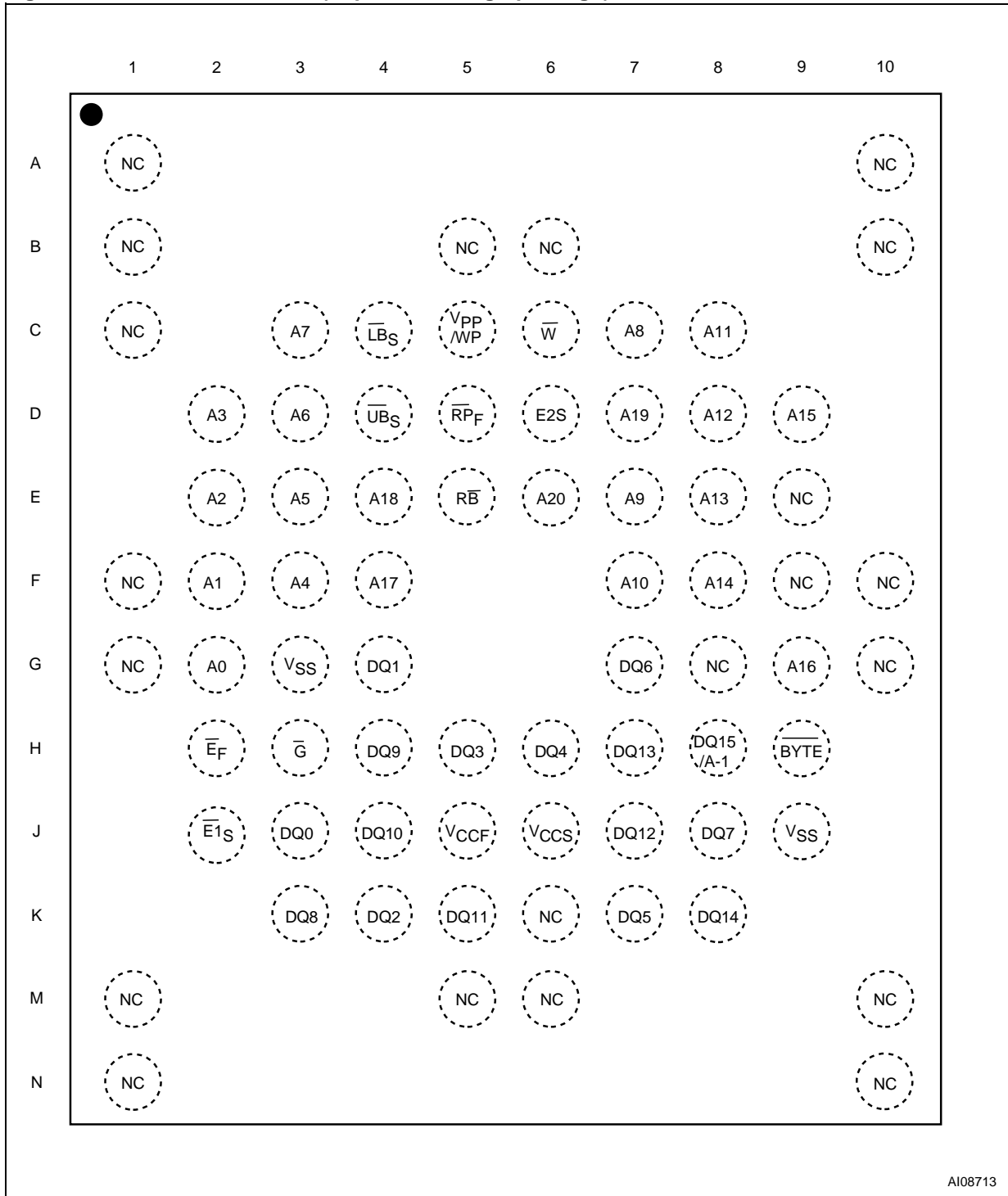


Table 1. Signal Names

A0-A17	Address Inputs common to the Flash Memory and SRAM
A18-A20	Address Inputs for Flash Memory only
DQ0-DQ7	Data Inputs/Outputs
DQ8-DQ14	Data Inputs/Outputs
DQ15A-1	Data Input/Output or Address Input
$\bar{G}$	Output Enable Input
$\bar{W}$	Write Enable Input
VCCF	Flash Power Supply
VPP/WP	VPP/Write Protect
VSS	Ground
VCCS	SRAM Power Supply
VSSS	SRAM Ground
NC	Not Connected Internally
<b>Flash Memory Control Functions</b>	
$\bar{E}_F$	Chip Enable Input
$\bar{RPF}$	Reset/Block Temporary Unprotect
$\bar{RB}$	Ready/Busy Output
$\bar{BYTE}$	Byte/Word Organization Select
<b>SRAM Control Functions</b>	
$\bar{E}_{1S}, E_{2S}$	Chip Enable Inputs
$\bar{UB}_S$	Upper Byte Enable Input
$\bar{LB}_S$	Lower Byte Enable Input

Figure 3. LFBGA Connections (Top view through package)



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## SIGNAL DESCRIPTION

See Figure 2 Logic Diagram and Table 1, Signal Names, for a brief overview of the signals connected to this device.

**Address Inputs (A0-A17).** Addresses A0-A17 are common inputs for the Flash and the SRAM components. The Address Inputs select the cells in the memory array to access during Bus Read operations. During Bus Write operations they control the commands sent to the Command Interface of the internal state machine. The Flash memory is accessed through the Chip Enable ( $\overline{E}_F$ ) and Write Enable ( $\overline{W}$ ) signals, while the SRAM is accessed through two Chip Enable signals ( $E_{1S}$  and  $E_{2S}$ ) and the Write Enable signal ( $\overline{W}$ ).

**Address Inputs (A18-A20).** Addresses A18-A20 are inputs for the Flash component only. The Flash memory is accessed through the Chip Enable ( $\overline{E}_F$ ) and Write Enable ( $\overline{W}$ ) signals

**Data Inputs/Outputs (DQ0-DQ7).** The Data I/O outputs the data stored at the selected address during a Bus Read operation. During Bus Write operations they represent the commands sent to the Command Interface of the Program/Erase Controller.

**Data Inputs/Outputs (DQ8-DQ14).** The Data I/O outputs the data stored at the selected address during a Bus Read operation when  $\overline{BYTE}$  is High,  $V_{IH}$ . When  $\overline{BYTE}$  is Low,  $V_{IL}$ , these pins are not used and are high impedance. During Bus Write operations the Command Register does not use these bits. When reading the Status Register these bits should be ignored.

**Data Input/Output or Address Input (DQ15A-1).** When  $\overline{BYTE}$  is High,  $V_{IH}$ , this pin behaves as a Data Input/Output pin (as DQ8-DQ14). When  $\overline{BYTE}$  is Low,  $V_{IL}$ , this pin behaves as an address pin; DQ15A-1 Low will select the LSB of the addressed Word, DQ15A-1 High will select the MSB. Throughout the text consider references to the Data Input/Output to include this pin when  $\overline{BYTE}$  is High and references to the Address Inputs to include this pin when  $\overline{BYTE}$  is Low except when stated explicitly otherwise.

**Flash Chip Enable ( $\overline{E}_F$ ).** The Chip Enable input activates the memory control logic, input buffers, decoders and sense amplifiers. When Chip Enable is at  $V_{IL}$  and  $\overline{RP}_F$  is at  $V_{IH}$  the device is in active mode. When Chip Enable is at  $V_{IH}$  the memory is deselected, the outputs are high impedance and the power consumption is reduced to the stand-by level.

**Output Enable ( $\overline{G}$ ).** The Output Enable,  $\overline{G}$ , controls the Bus Read operation of the device.

**Write Enable ( $\overline{W}$ ).** The Write Enable,  $\overline{W}$ , controls the Bus Write operation of the device.

**$V_{PP}$ /Write Protect ( $V_{PP}/\overline{WP}$ ).** The  $V_{PP}$ /Write Protect pin provides two functions. The  $V_{PP}$  function allows the Flash memory to use an external high voltage power supply to reduce the time required for Program operations. This is achieved by bypassing the unlock cycles and/or using the Double Word or Quadruple Byte Program commands. The Write Protect function provides a hardware method of protecting the two outermost boot blocks in the Flash memory.

When  $V_{PP}$ /Write Protect is Low,  $V_{IL}$ , the memory protects the two outermost boot blocks; Program and Erase operations in these blocks are ignored while  $V_{PP}$ /Write Protect is Low, even when  $\overline{RP}_F$  is at  $V_{ID}$ .

When  $V_{PP}$ /Write Protect is High,  $V_{IH}$ , the memory reverts to the previous protection status of the two outermost boot blocks. Program and Erase operations can now modify the data in these blocks unless the blocks are protected using Block Protection.

When  $V_{PP}$ /Write Protect is raised to  $V_{PP}$  the memory automatically enters the Unlock Bypass mode. When  $V_{PP}$ /Write Protect returns to  $V_{IH}$  or  $V_{IL}$  normal operation resumes. During Unlock Bypass Program operations the memory draws  $I_{PP}$  from the pin to supply the programming circuits. See the M29DW323D datasheet for more details.

**Reset/Block Temporary Unprotect ( $\overline{RP}_F$ ).** The Reset/Block Temporary Unprotect pin can be used to apply a Hardware Reset to the memory or to temporarily unprotect all Blocks that have been protected.

Note that if  $V_{PP}/\overline{WP}$  is at  $V_{IL}$ , then the two outermost boot blocks will remain protected even if  $\overline{RP}_F$  is at  $V_{ID}$ .

A Hardware Reset is achieved by holding Reset/Block Temporary Unprotect Low,  $V_{IL}$ , for at least  $t_{PLPX}$ . After Reset/Block Temporary Unprotect goes High,  $V_{IH}$ , the memory will be ready for Bus Read and Bus Write operations after  $t_{PHEL}$  or  $t_{RHEL}$ , whichever occurs last. See the M29DW323D datasheet for more details.

Holding  $\overline{RP}_F$  at  $V_{ID}$  will temporarily unprotect the protected Blocks in the memory. Program and Erase operations on all blocks will be possible. The transition from  $V_{IH}$  to  $V_{ID}$  must be slower than  $t_{PHPHH}$ .

**Ready/Busy Output ( $\overline{RB}$ ).** The Ready/Busy pin is an open-drain output that can be used to identify when the Flash memory is performing a Program or Erase operation. During Program or Erase operations Ready/Busy is Low,  $V_{OL}$ . Ready/Busy is high-impedance during Read mode, Auto Select mode and Erase Suspend mode.

After a Hardware Reset, Bus Read and Bus Write operations cannot begin until Ready/Busy becomes high-impedance.

**Byte/Word Organization Select ( $\overline{\text{BYTE}}$ ).** The Byte/Word Organization Select pin is used to switch between the x8 and x16 Bus modes of the Flash memory. When Byte/Word Organization Select is Low,  $V_{IL}$ , the Flash memory is in x8 mode, when it is High,  $V_{IH}$ , the Flash memory is in x16 mode.

**SRAM Chip Enable ( $\overline{\text{E1S}}$ ,  $\text{E2S}$ ).** The Chip Enable inputs activate the SRAM memory control logic, input buffers and decoders.  $\overline{\text{E1S}}$  at  $V_{IH}$  or  $\text{E2S}$  at  $V_{IL}$  deselects the memory and reduces the power consumption to the standby level.  $\overline{\text{E1S}}$  and  $\text{E2S}$  can also be used to control writing to the SRAM memory array, while  $\overline{\text{W}}$  remains at  $V_{IL}$ . It is

not allowed to set  $\overline{\text{EF}}$  at  $V_{IL}$ ,  $\overline{\text{E1S}}$  at  $V_{IL}$  and  $\text{E2S}$  at  $V_{IH}$  at the same time.

**SRAM Upper Byte Enable ( $\overline{\text{UBS}}$ ).** The Upper Byte Enable enables the upper bytes for SRAM (DQ8-DQ15).  $\overline{\text{UBS}}$  is active low.

**SRAM Lower Byte Enable ( $\overline{\text{LBS}}$ ).** The Lower Byte Enable enables the lower bytes for SRAM (DQ0-DQ7).  $\overline{\text{LBS}}$  is active low.

**V<sub>CCF</sub> Supply Voltage (2.7V to 3.3V).**  $V_{CCF}$  provides the power supply to the internal core of the Flash Memory device. It is the main power supply for all operations (Read, Program and Erase).

**V<sub>CCS</sub> Supply Voltage (2.7V to 3.3V).**  $V_{CCS}$  provides the power supply for the SRAM control pins.

**V<sub>SS</sub> Ground.**  $V_{SS}$  is the ground reference for all voltage measurements in the Flash and SRAM chips.

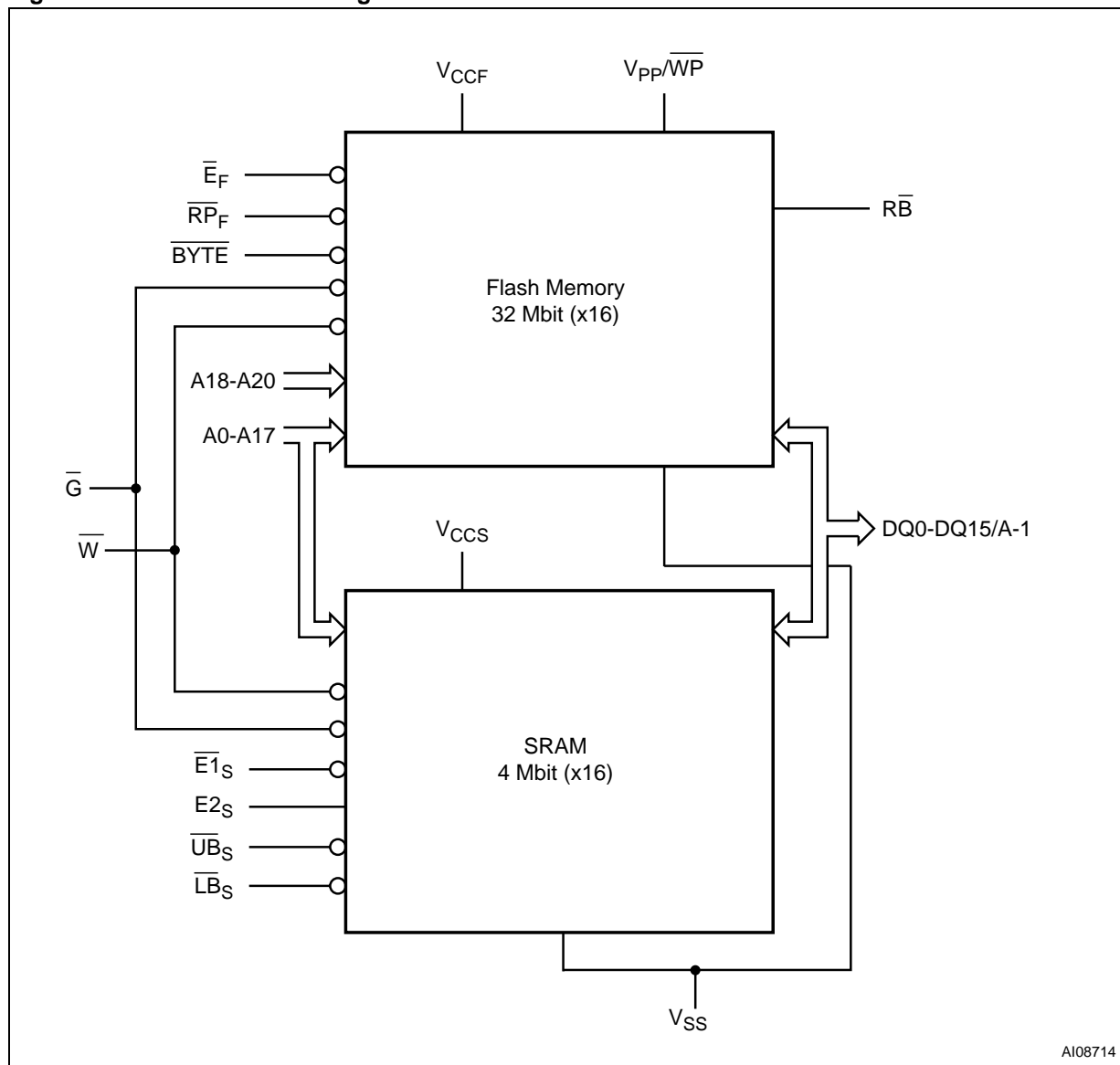
**FUNCTIONAL DESCRIPTION**

The Flash and SRAM components have separate power supplies. They are distinguished by three chip enable inputs:  $\overline{E}_F$  for the Flash memory and,  $\overline{E}_{1S}$  and  $E_{2S}$  for the SRAM.

Recommended operating conditions do not allow both the Flash and the SRAM to be in active mode at the same time. The most common example is

simultaneous read operations on the Flash and the SRAM which would result in a data bus contention. Therefore it is recommended to put the SRAM in the high impedance state when reading the Flash and vice versa (see Table 2 Main Operation Modes for details).

**Figure 4. Functional Block Diagram**



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Table 2. Main Operation Modes,  $\overline{\text{BYTE}} = V_{IH}^{(2)}$ 

Operation Mode		$\overline{E}_F$	$\overline{RPF}$	$\overline{G}$	$\overline{W}$	$\overline{E1}_S$	$E2_S$	$\overline{UB}_S$	$\overline{LB}_S$	DQ15-DQ8	DQ7-DQ0
Flash Memory	Read	$V_{IL}$	$V_{IH}$	$V_{IL}$	$V_{IH}$	SRAM must be disabled				Data Output	
	Write	$V_{IL}$	$V_{IH}$	$V_{IH}$	$V_{IL}$	SRAM must be disabled				Data Input	
	Standby	$V_{IH}$	$V_{CC} \pm 0.3$	X	X	Any SRAM mode is allowed				Hi-Z	
	Output Disable	X	$V_{IH}$	$V_{IH}$	$V_{IH}$	Any SRAM mode is allowed				Hi-Z	
	Reset	X	$V_{IL}$	X	X	Any SRAM mode is allowed				Hi-Z	
SRAM	Read	Flash must be disabled	$V_{IL}$	$V_{IH}$	$V_{IL}$	$V_{IH}$	$V_{IL}$	$V_{IL}$	Data out Word Read		
			$V_{IL}$	$V_{IH}$	$V_{IL}$	$V_{IH}$	$V_{IL}$	$V_{IH}$	Data out	Hi-Z	
			$V_{IL}$	$V_{IH}$	$V_{IL}$	$V_{IH}$	$V_{IH}$	$V_{IL}$	Hi-Z	Data out	
	Write	Flash must be disabled	X	$V_{IL}$	$V_{IL}$	$V_{IH}$	$V_{IL}$	$V_{IL}$	Data in Word Write		
			X	$V_{IL}$	$V_{IL}$	$V_{IH}$	$V_{IH}$	$V_{IL}$	Data in	Hi-Z	
			X	$V_{IL}$	$V_{IL}$	$V_{IH}$	$V_{IL}$	$V_{IH}$	Hi-Z	Data in	
	Standby/ Power Down	Any Flash mode is allowable	X	X	$V_{IH}$	X	X	X	Hi-Z		
			X	X	X	X	$V_{IH}$	$V_{IH}$	Hi-Z		
			X	X	X	$V_{IL}$	X	X	Hi-Z		
	Output Disable	Any Flash mode is allowable	$V_{IH}$	$V_{IH}$	$V_{IL}$	$V_{IH}$	$V_{IL}$	$V_{IL}$	Hi-Z		
			$V_{IH}$	$V_{IH}$	$V_{IL}$	$V_{IH}$	$V_{IL}$	$V_{IH}$	Hi-Z		
			$V_{IH}$	$V_{IH}$	$V_{IL}$	$V_{IH}$	$V_{IH}$	$V_{IL}$	Hi-Z		

Note: 1. X = Don't Care =  $V_{IL}$  or  $V_{IH}$ .

2. This table is also valid when  $\overline{\text{BYTE}} = V_{IL}$ , with the only difference that DQ15-DQ8 are always high impedance in this case.

3. For the Block Protect and Unprotect features, see the M29DW323D datasheet. Only the In-System Technique is available in the stacked product.

4. The Read Manufacturer Code and Read Device Code operations are not available in the stacked product (see the "Bus Operations" Tables in M29DW323D datasheet for details). See the "Auto Select Command" in the M29DW323D to read the Manufacturer and Device Codes.

**FLASH MEMORY DEVICE**

The M76DW52003TA and M76DW52003BA contain one 32 Mbit Flash memory. For detailed information on how to use the Flash memory see the

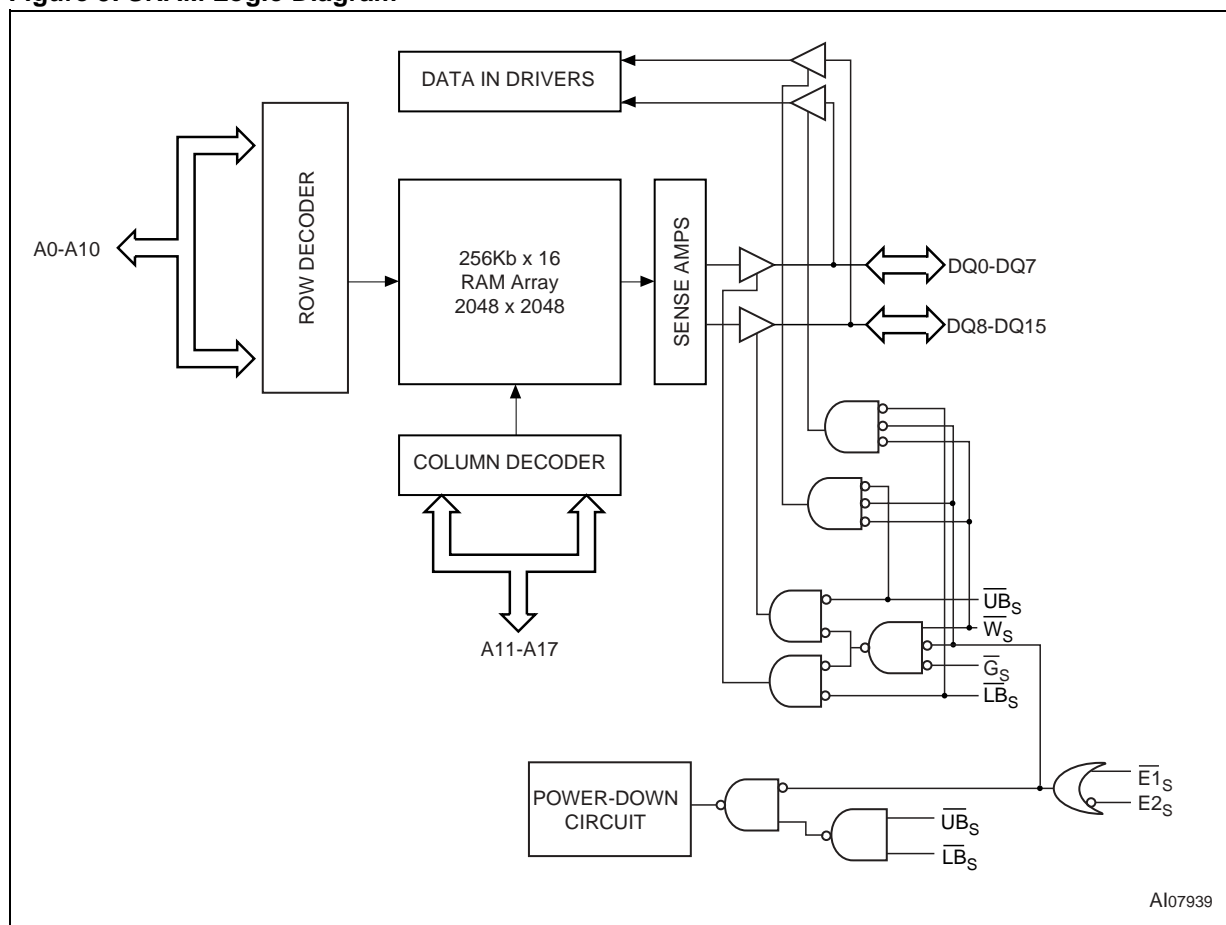
M29DW323D datasheet, which is available on the STMicroelectronics web site, [www.st.com](http://www.st.com).

**SRAM DEVICE**

The SRAM is a 4Mbit asynchronous random access memory which features a super low voltage operation and low current consumption with an access time of 70ns under all conditions. The mem-

ory operations can be performed using a single low voltage supply, 2.7V to 3.3V, which is the same as the Flash voltage supply.

**Figure 5. SRAM Logic Diagram**



## SRAM OPERATIONS

There are five standard operations that control the SRAM component. These are Bus Read, Bus Write, Standby/Power-down, Data Retention and Output Disable. A summary is shown in Table 2, Main Operation Modes

**Read.** Read operations are used to output the contents of the SRAM Array. The SRAM is in Read mode whenever Write Enable,  $\overline{W}_S$ , is at  $V_{IH}$ , Output Enable,  $\overline{G}_S$ , is at  $V_{IL}$ , Chip Enable,  $E1_S$ , is at  $V_{IL}$ , Chip Enable,  $E2_S$ , is at  $V_{IH}$ , and Byte Enable inputs,  $\overline{UB}_S$  and  $\overline{LB}_S$  are at  $V_{IL}$ .

Valid data will be available on the output pins after a time of  $t_{AVQV}$  after the last stable address. If the Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter ( $t_{E1LQV}$ ,  $t_{E2HQV}$ , or  $t_{GLQV}$ ) rather than the address. Data out may be indeterminate at  $t_{E1LQX}$ ,  $t_{E2HQX}$  and  $t_{GLQX}$ , but data lines will always be valid at  $t_{AVQV}$  (see Table 8, Table 8, Figures 8 and 9, SRAM Read AC Characteristics).

**Write.** Write operations are used to write data to the SRAM. The SRAM is in Write mode whenever  $\overline{W}$  and  $\overline{E1}_S$  are at  $V_{IL}$ , and  $E2_S$  is at  $V_{IH}$ . Either the Chip Enable inputs,  $\overline{E1}_S$  and  $E2_S$ , or the Write Enable input,  $\overline{W}_S$ , must be deasserted during address transitions for subsequent write cycles.

A Write operation is initiated when  $\overline{E1}_S$  is at  $V_{IL}$ ,  $E2_S$  is at  $V_{IH}$  and  $\overline{W}$  is at  $V_{IL}$ . The data is latched on the falling edge of  $\overline{E1}_S$ , the rising edge of  $E2_S$  or the falling edge of  $\overline{W}_S$ , whichever occurs last. The Write cycle is terminated on the rising edge of  $\overline{E1}_S$ , the rising edge of  $\overline{W}$  or the falling edge of  $E2_S$ , whichever occurs first.

If the Output is enabled ( $\overline{E1}_S=V_{IL}$ ,  $E2_S=V_{IH}$  and  $\overline{G}_S=V_{IL}$ ), then  $\overline{W}$  will return the outputs to high impedance within  $t_{WLQZ}$  of its falling edge. Care must be taken to avoid bus contention in this type of operation. The Data input must be valid for  $t_{DVVWH}$  before the rising edge of Write Enable, for  $t_{DVE1H}$  before the rising edge of  $\overline{E1}_S$  or for  $t_{DVE2L}$  before the falling edge of  $E2_S$ , whichever occurs first, and remain valid for  $t_{WHDX}$ ,  $t_{E1HAX}$  or  $t_{E2LAX}$  (see Table 9, SRAM Write AC Characteristics, Figures 11, 12, 13 and 14).

**Standby/Power-Down.** The SRAM component has a chip enabled power-down feature which invokes an automatic standby mode (see Table 8, SRAM Read AC Characteristics, Figure 10, SRAM Standby AC Waveforms). The SRAM is in Standby mode whenever either Chip Enable is deasserted,  $\overline{E1}_S$  at  $V_{IH}$  or  $E2_S$  at  $V_{IL}$ . It is also possible when  $\overline{UB}_S$  and  $\overline{LB}_S$  are at  $V_{IH}$ .

**Data Retention.** The SRAM data retention performance as  $V_{CCS}$  goes down to  $V_{DR}$  are described in Table 10, SRAM Low  $V_{CCS}$  Data Retention Characteristic, and Figure 15, SRAM Low  $V_{CCS}$  Data Retention AC Waveforms,  $E1_S$  or  $\overline{UB}_S / \overline{LB}_S$  Controlled. In  $\overline{E1}_S$  controlled data retention mode, the minimum standby current mode is entered when  $\overline{E1}_S \geq V_{CCS} - 0.2V$  and  $E2_S \leq 0.2V$  or  $E2_S \geq V_{CCS} - 0.2V$ . In  $E2_S$  controlled data retention mode, minimum standby current mode is entered when  $E2_S \leq 0.2V$ .

**Output Disable.** The data outputs are high impedance when the Output Enable,  $\overline{G}_S$ , is at  $V_{IH}$  with Write Enable,  $\overline{W}_S$ , at  $V_{IH}$ .

**MAXIMUM RATING**

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not im-

plied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

**Table 3. Absolute Maximum Ratings**

Symbol	Parameter	Value		Unit
		Min	Max	
T <sub>A</sub>	Ambient Operating Temperature <sup>(1)</sup>	-40	85	°C
T <sub>BIAS</sub>	Temperature Under Bias	-50	125	°C
T <sub>STG</sub>	Storage Temperature	-65	150	°C
V <sub>IO</sub>	Input or Output Voltage	-0.5	V <sub>CCF</sub> +0.3	V
V <sub>CCF</sub>	Flash Supply Voltage	-0.6	4	V
V <sub>PPF</sub>	Program Voltage	-0.6	13.5	V
V <sub>CCS</sub>	SRAM Supply Voltage	-0.5	3.8	V

Note: 1. Depends on range.

**DC AND AC PARAMETERS**

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in Table 4, Operating and AC Measurement Conditions. Designers should check that the operating conditions

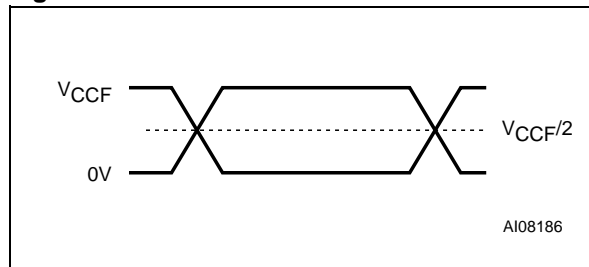
in their circuit match the measurement conditions when relying on the quoted parameters.

The operating and AC measurement parameters given in this section (see Table 4 below) correspond to those of the stand-alone Flash and SRAM devices. For compatibility purposes, the M29DW323D voltage range is restricted to  $V_{CCS}$  in the stacked product.

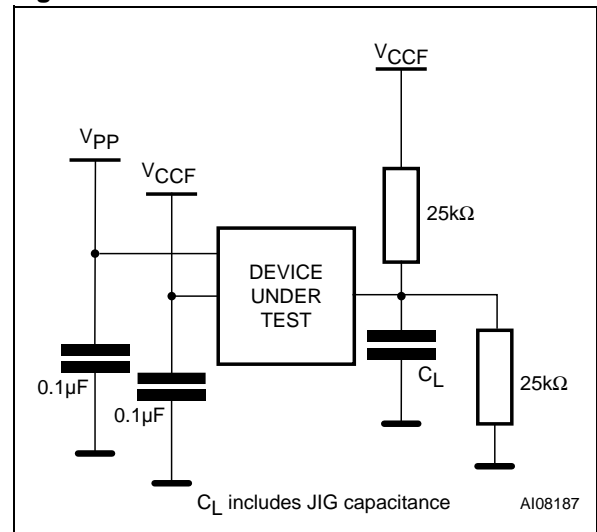
**Table 4. Operating and AC Measurement Conditions**

Parameter	Flash Memory		SRAM		Units
	Min	Max	Min	Max	
$V_{CCF}$ Supply Voltage	2.7	3.6	–	–	V
$V_{CCS}$ Supply Voltage	–	–	2.7	3.3	V
Ambient Operating Temperature	–40	85	–40	85	°C
Load Capacitance ( $C_L$ )	30		30		pF
Input Rise and Fall Times		10		3.3	ns
Input Pulse Voltages	0 to $V_{CCF}$		0 to $V_{CCF}$		V
Input and Output Timing Ref. Voltages	$V_{CCF}/2$		$V_{CCF}/2$		V

**Figure 6. AC Measurement I/O Waveform**



**Figure 7. AC Measurement Load Circuit**



**Table 5. Device Capacitance**

Symbol	Parameter	Test Condition	Typ	Max	Unit
$C_{IN}$	Input Capacitance	$V_{IN} = 0V, f=1 \text{ MHz}$		12	pF
$C_{OUT}$	Output Capacitance	$V_{OUT} = 0V, f=1 \text{ MHz}$		15	pF

Note: Sampled only, not 100% tested.

**Table 6. Flash DC Characteristics**

Symbol	Parameter	Test Condition	Min	Max	Unit
I <sub>LI</sub>	Input Leakage Current	0V ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>		±1	μA
I <sub>LO</sub>	Output Leakage Current	0V ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub>		±1	μA
I <sub>CC1</sub> <sup>(2)</sup>	Supply Current (Read)	$\bar{E}_F = V_{IL}, \bar{G} = V_{IH},$ f = 6MHz		10	mA
I <sub>CC2</sub>	Supply Current (Standby)	$\bar{E}_F = V_{CC} \pm 0.2V,$ $\overline{RP}_F = V_{CC} \pm 0.2V$		100	μA
I <sub>CC3</sub> <sup>(1,2)</sup>	Supply Current (Program/ Erase)	Program/Erase Controller active	$V_{PP}/\overline{WP} =$ V <sub>IL</sub> or V <sub>IH</sub>	20	mA
			$V_{PP}/\overline{WP} = V_{PP}$	20	mA
V <sub>IL</sub>	Input Low Voltage		-0.5	0.8	V
V <sub>IH</sub>	Input High Voltage		0.7V <sub>CC</sub>	V <sub>CC</sub> + 0.3	V
V <sub>PP</sub>	Voltage for V <sub>PP</sub> / $\overline{WP}$ Program Acceleration	V <sub>CC</sub> = 3.0V ±10%	11.5	12.5	V
I <sub>PP</sub>	Current for V <sub>PP</sub> / $\overline{WP}$ Program Acceleration	V <sub>CC</sub> = 3.0V ±10%		15	mA
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 1.8mA		0.45	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -100μA	V <sub>CC</sub> - 0.4		V
V <sub>ID</sub>	Identification Voltage		11.5	12.5	V
V <sub>LKO</sub>	Program/Erase Lockout Supply Voltage		1.8	2.3	V

Note: 1. Sampled only, not 100% tested.

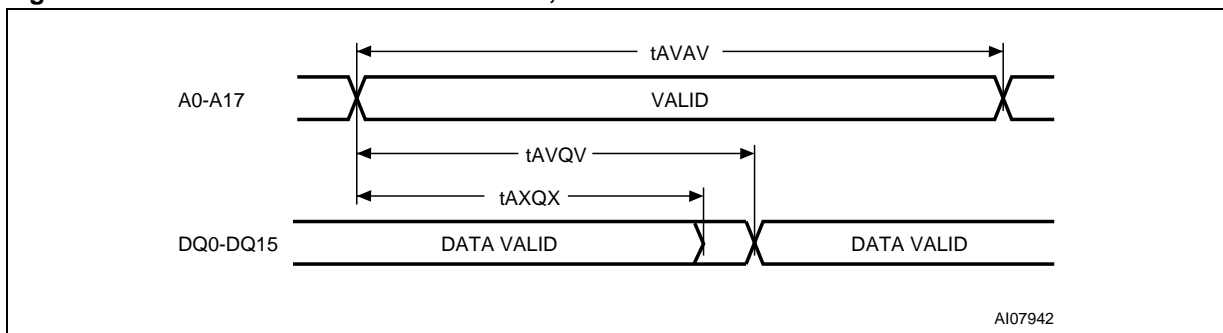
2. In Dual operations the Supply Current will be the sum of I<sub>CC1</sub>(read) and I<sub>CC3</sub> (program/erase).

Table 7. SRAM DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
$I_{LI}$	Input Leakage Current	$0V \leq V_{IN} \leq V_{CCS}$			$\pm 1$	$\mu A$
$I_{LO}$	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CCS}$ , SRAM Outputs Hi-Z			$\pm 1$	$\mu A$
$I_{CCS}$	$V_{CC}$ Standby Current	$\overline{E1S} \geq V_{CCS} - 0.2V$ $V_{IN} \geq V_{CCS} - 0.2V$ or $V_{IN} \leq 0.2V$ $f = f_{max}$ (A0-A17 and DQ0-DQ15 only) $f = 0$ ( $\overline{GS}$ , $\overline{WS}$ , $\overline{UBS}$ and $\overline{LBS}$ )		7	15	$\mu A$
		$\overline{E1S} \geq V_{CCS} - 0.2V$ $V_{IN} \geq V_{CCS} - 0.2V$ or $V_{IN} \leq 0.2V$ , $f = 0$		7	15	$\mu A$
$I_{CC}$	Supply Current	$f = f_{max} = 1/AVAV$ , $V_{CCS} = 3.3V$ , $I_{OUT} = 0$ mA		5.5	12	mA
		$f = 1MHz$ , $V_{CCS} = 3.3V$ , $I_{OUT} = 0$ mA		1.5	3	mA
$V_{IL}$	Input Low Voltage		-0.3		0.8	V
$V_{IH}$	Input High Voltage		2.2		$V_{CCS} + 0.3$	V
$V_{OL}$	Output Low Voltage	$V_{CCS} = V_{CC}$ min $I_{OL} = 2.1mA$			0.4	V
$V_{OH}$	Output High Voltage	$V_{CCS} = V_{CC}$ min $I_{OH} = -1.0mA$	2.4			V

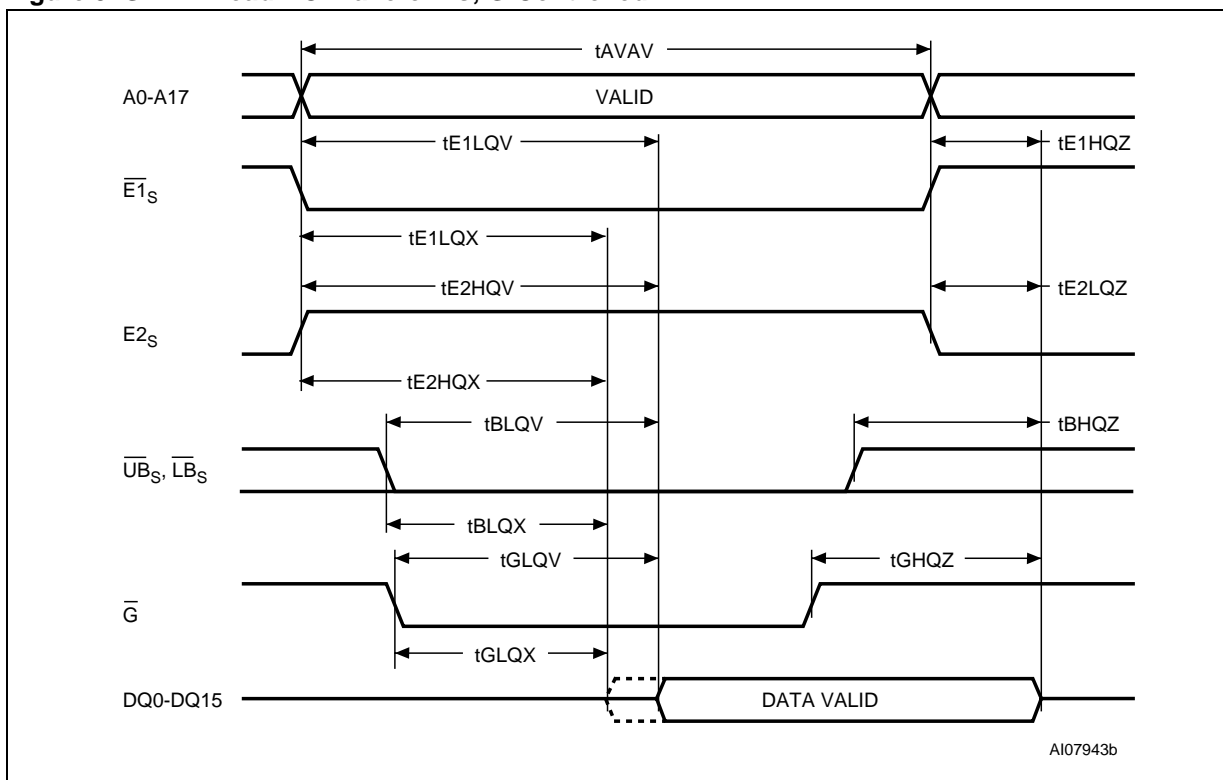
Note: 1. Sampled only, not 100% tested.

Figure 8. SRAM Read Mode AC Waveforms, Address Controlled



Note:  $\overline{E1}_S$  = Low,  $E2_S$  = High,  $\overline{G}$  = Low,  $\overline{UB}_S$  and/or  $\overline{LB}_S$  = High,  $\overline{W}$  = High.

Figure 9. SRAM Read AC Waveforms,  $\overline{G}$  Controlled



Note: Write Enable ( $\overline{W}$ ) = High. Address Valid prior to or at the same time as  $\overline{E1}_S$ ,  $\overline{UB}_S$  and  $\overline{LB}_S$  going Low.

Figure 10. SRAM Standby AC Waveforms

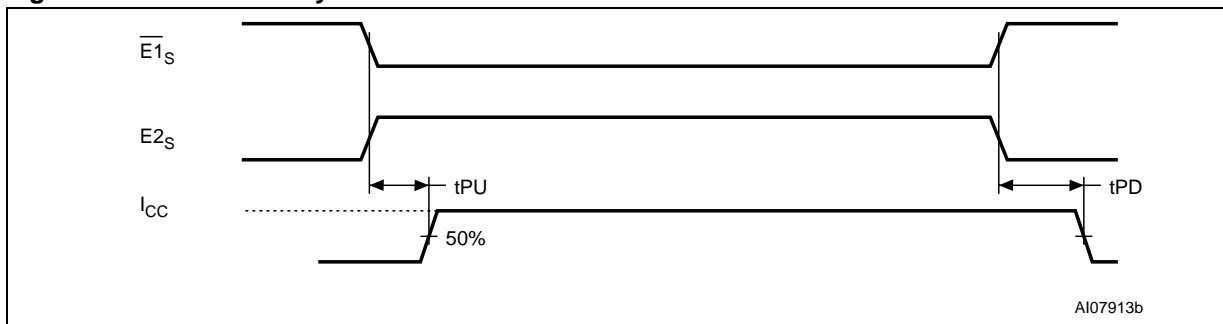


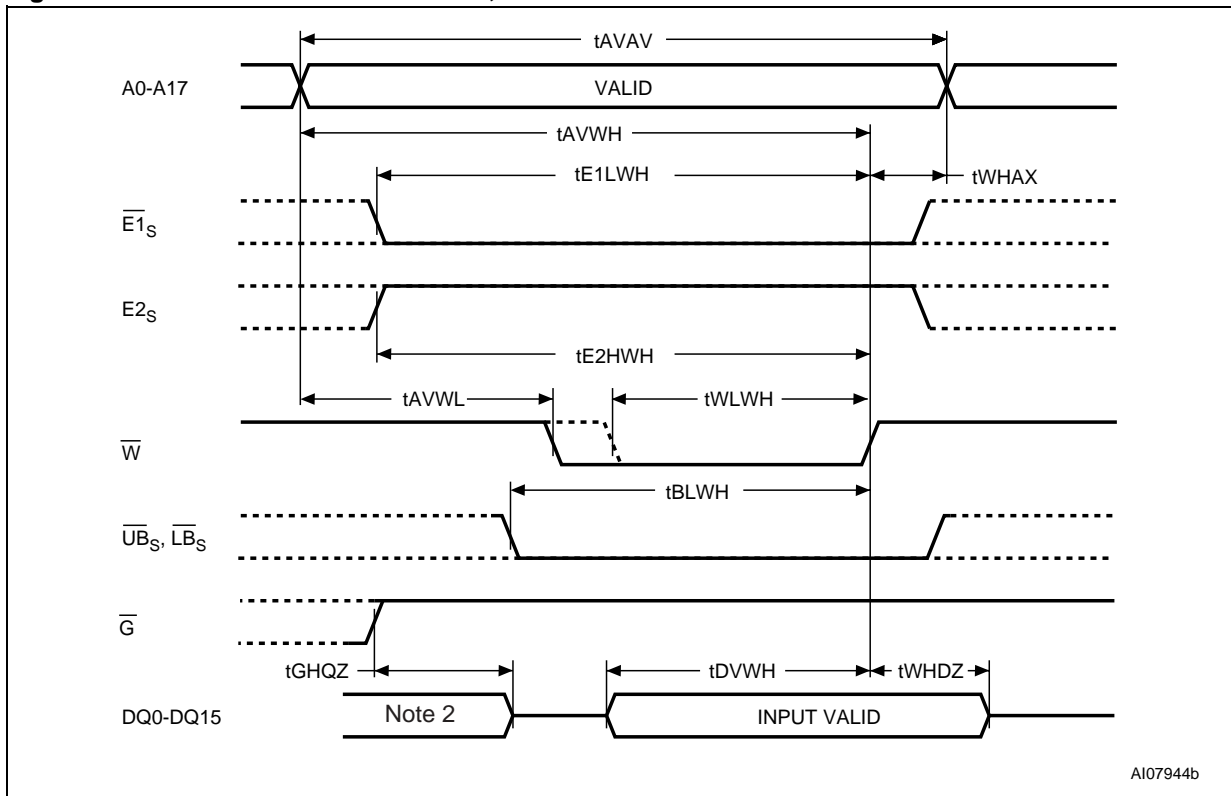


Table 8. SRAM Read AC Characteristics

Symbol	Alt	Parameter	SRAM		Unit
			Min	Max	
t <sub>AVAV</sub>	t <sub>RC</sub>	Read Cycle Time	70		ns
t <sub>AVQV</sub>	t <sub>ACC</sub>	Address Valid to Output Valid		70	ns
t <sub>AXQX</sub>	t <sub>OH</sub>	Address Transition to Output Transition	10		ns
t <sub>BHQZ</sub>	t <sub>BHZ</sub>	$\overline{UB}_S, \overline{LB}_S$ Disable to Hi-Z Output		25	ns
t <sub>BLQV</sub>	t <sub>AB</sub>	$\overline{UB}_S, \overline{LB}_S$ Access Time		70	ns
t <sub>BLQX</sub>	t <sub>BLZ</sub>	$\overline{UB}_S, \overline{LB}_S$ Enable to Low-Z Output	5		ns
t <sub>E1LQV</sub> t <sub>E2HQV</sub>	t <sub>ACS1</sub>	Chip Enable 1 Low or Chip Enable 2 High to Output Valid		70	ns
t <sub>E1LQX</sub> t <sub>E2HQX</sub>	t <sub>CLZ1</sub>	Chip Enable 1 Low or Chip Enable 2 High to Output Transition	10		ns
t <sub>E1HQZ</sub> t <sub>E2LQZ</sub>	t <sub>HZCE</sub>	Chip Enable High or Chip Enable 2 Low to Output Hi-Z		25	ns
t <sub>GHQZ</sub>	t <sub>OHZ</sub>	Output Enable High to Output Hi-Z		25	ns
t <sub>GLQV</sub>	t <sub>OE</sub>	Output Enable Low to Output Valid		35	ns
t <sub>GLQX</sub>	t <sub>OLZ</sub>	Output Enable Low to Output Transition	5		ns
t <sub>PD</sub> <sup>(1)</sup>		Chip Enable 1 High or Chip Enable 2 Low to Power Down		70	ns
t <sub>PU</sub> <sup>(1)</sup>		Chip Enable 1 Low or Chip Enable 2 High to Power Up	0		ns

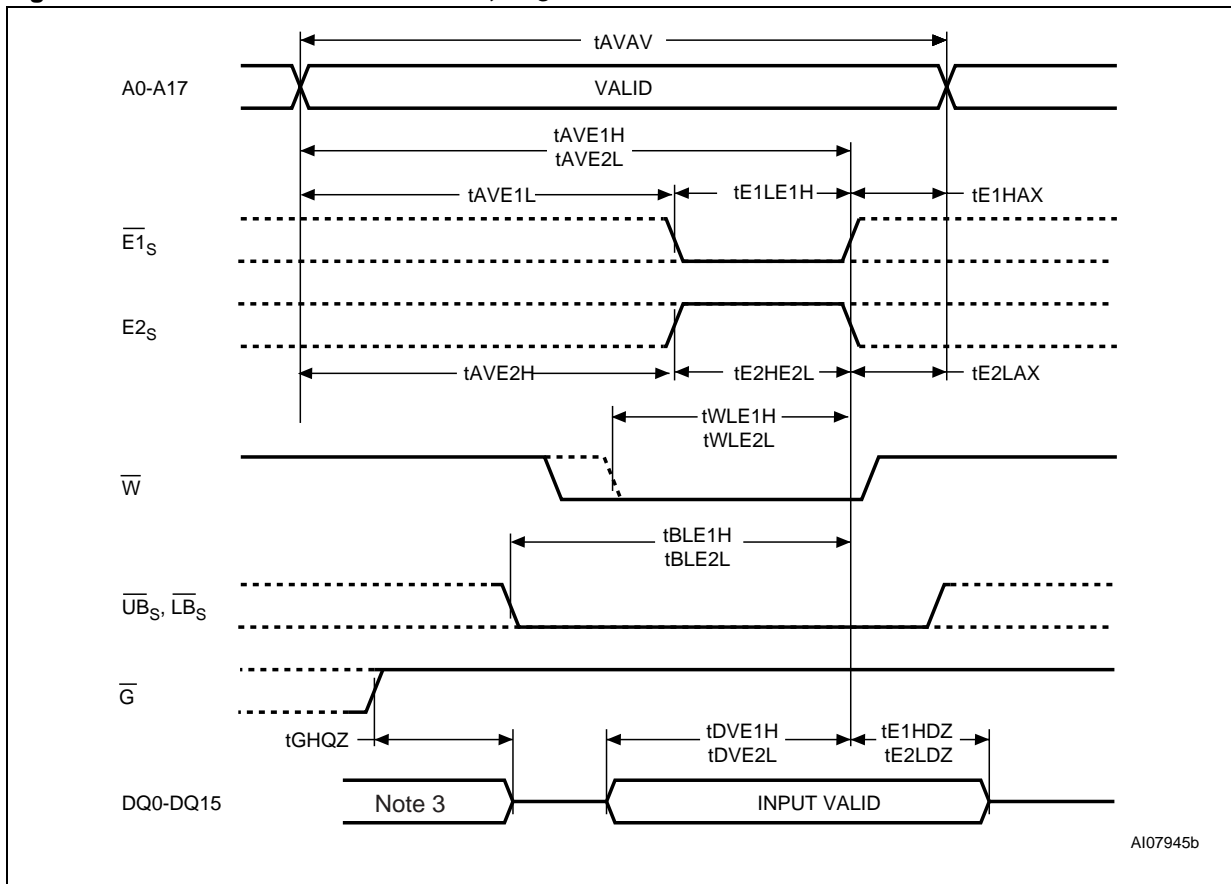
Note: 1. Sampled only. Not 100% tested.

Figure 11. SRAM Write AC Waveforms,  $\overline{W}$  Controlled



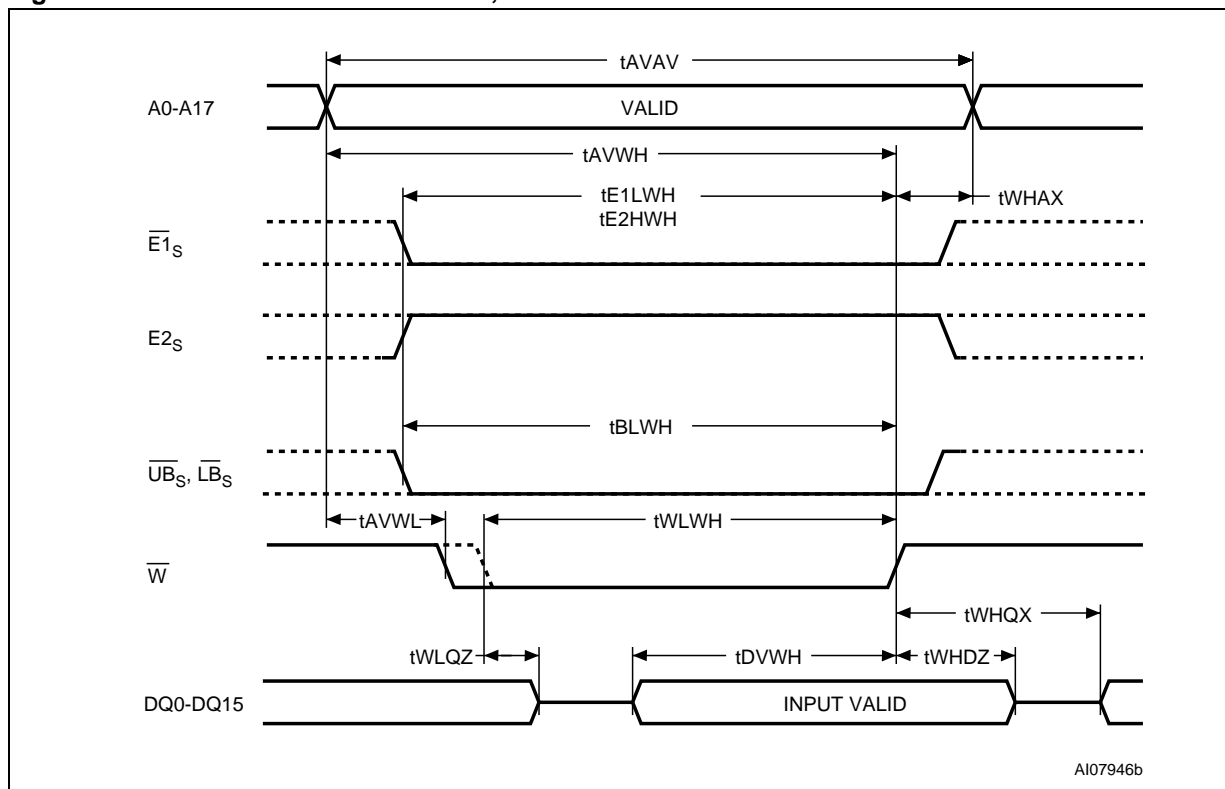
- Note: 1.  $\overline{W}$ ,  $\overline{E1s}$ ,  $E2s$ ,  $\overline{UBs}$  and/or  $\overline{LBs}$  must be asserted to initiate a write cycle. Output Enable ( $\overline{G}$ ) = Low (otherwise, DQ0-DQ15 are high impedance). If  $\overline{E1s}$ ,  $E2s$  and  $\overline{W}$  are deasserted at the same time, DQ0-DQ15 remain high impedance.
2. The I/O pins are in output mode and input signals must not be applied.

Figure 12. SRAM Write AC Waveforms,  $\overline{E1}_S$  Controlled



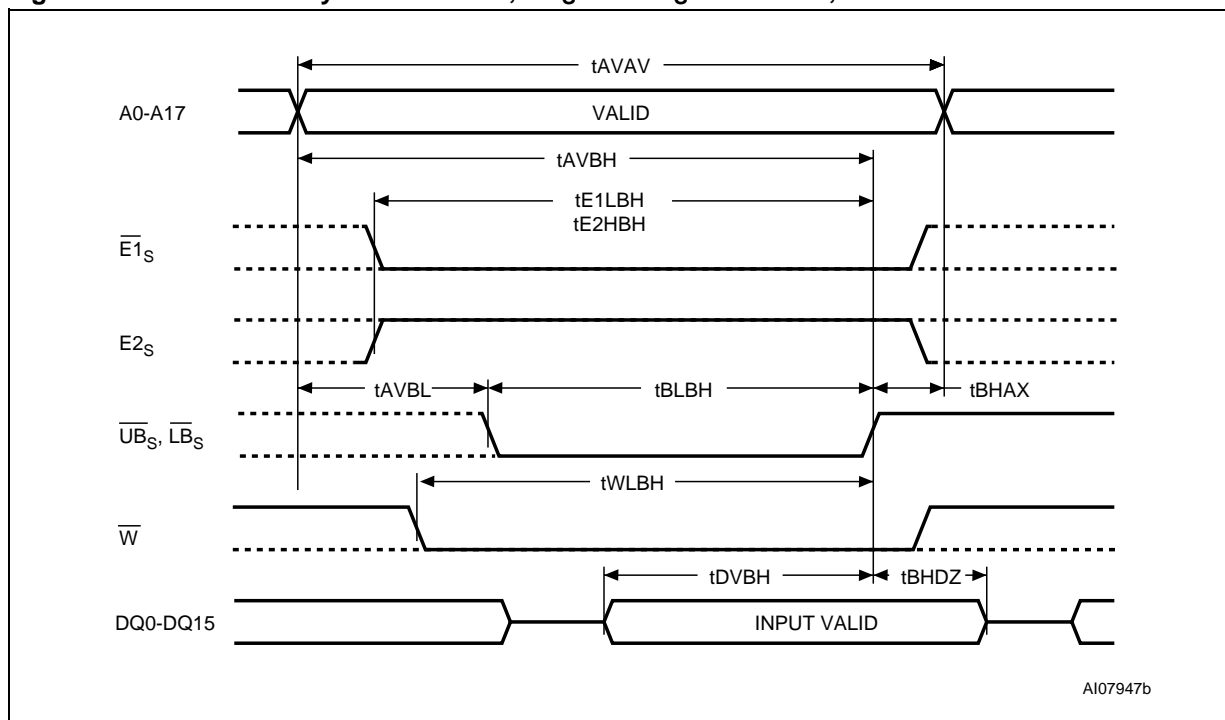
- Note: 1.  $\overline{W}_S, \overline{E1}_S, E2_S, \overline{UB}_S$  and/or  $\overline{LB}_S$  must be asserted to initiate a write cycle. Output Enable ( $\overline{G}_S$ ) = Low (otherwise, DQ0-DQ15 are high impedance). If  $\overline{E1}_S, E2_S$  and  $\overline{W}$  are deasserted at the same time, DQ0-DQ15 remain high impedance.
2. If  $\overline{E1}_S, E2_S$  and  $\overline{W}$  are deasserted at the same time, DQ0-DQ15 remain high impedance.
3. The I/O pins are in output mode and input signals must not be applied.

Figure 13. SRAM Write AC Waveforms,  $\overline{W}$  Controlled with  $\overline{G}$  Low



Note: 1. If  $\overline{E1}_s$ ,  $E2_s$  and  $\overline{W}$  are deasserted at the same time, DQ0-DQ15 remain high impedance.

Figure 14. SRAM Write Cycle Waveform,  $\overline{UB}_s$  and  $\overline{LB}_s$  Controlled,  $\overline{G}$  Low



Note: 1. If  $\overline{E1}_s$ ,  $E2_s$  and  $\overline{W}$  are deasserted at the same time, DQ0-DQ15 remain high impedance.

Table 9. SRAM Write AC Characteristics

Symbol	Alt	Parameter	SRAM		Unit
			Min	Max	
$t_{AVAV}$	$t_{WC}$	Write Cycle Time	70		ns
$t_{AVE1L}$ , $t_{AVE2H}$ , $t_{AVWL}$ , $t_{AVBL}$	$t_{AS}$	Address Valid to Beginning of Write	0		ns
$t_{AVE1H}$ , $t_{AVE2L}$	$t_{AW}$	Address Valid to Chip Enable 1 Low or Chip Enable 2 High	60		ns
$t_{AVWH}$	$t_{AW}$	Address Valid to Write Enable High	60		ns
$t_{BLWH}$ $t_{BLE1H}$ $t_{BLE2L}$ $t_{AVBH}$	$t_{BW}$	$\overline{UB}_S, \overline{LB}_S$ Valid to End of Write	60		ns
$t_{BLBH}$	$t_{BW}$	$\overline{UB}_S, \overline{LB}_S$ Low to $\overline{UB}_S, \overline{LB}_S$ High	60		ns
$t_{DVE1H}$ , $t_{DVE2L}$ , $t_{DVWH}$ $t_{DVBH}$	$t_{DW}$	Input Valid to End of Write	30		ns
$t_{E1HAX}$ , $t_{E2LAX}$ , $t_{WHAX}$ $t_{BHAX}$	$t_{WR}$	End of Write to Address Change	0		ns
$t_{E1HDZ}$ , $t_{E2LDZ}$ , $t_{WHDZ}$ $t_{BHDZ}$	$t_{HD}$	Address Transition to End of Write	0		ns
$t_{E1LE1H}$ , $t_{E1LBH}$ $t_{E1LWH}$	$t_{CW1}$	Chip Enable 1 Low to End of Write	60		ns
$t_{E2HE2L}$ , $t_{E2HBH}$ , $t_{E2HWH}$	$t_{CW2}$	Chip Enable 2 High to End of Write	60		ns
$t_{GHQZ}$	$t_{GHZ}$	Output Enable High to Output Hi-Z		25	ns
$t_{WHQX}$	$t_{DH}$	Write Enable High to Input Transition	5		ns
$t_{WLBH}$	$t_{WP}$	Write Enable Low to $\overline{UB}_S, \overline{LB}_S$ High	50		ns
$t_{WLQZ}$	$t_{WHZ}$	Write Enable Low to Output Hi-Z		25	ns
$t_{WLWH}$ $t_{WLE1H}$ $t_{WLE2L}$	$t_{WP}$	Write Enable Pulse Width	50		ns

Figure 15. SRAM Low V<sub>CCS</sub> Data Retention AC Waveforms,  $\overline{E1}_S$  or  $\overline{UB}_S / \overline{LB}_S$  Controlled

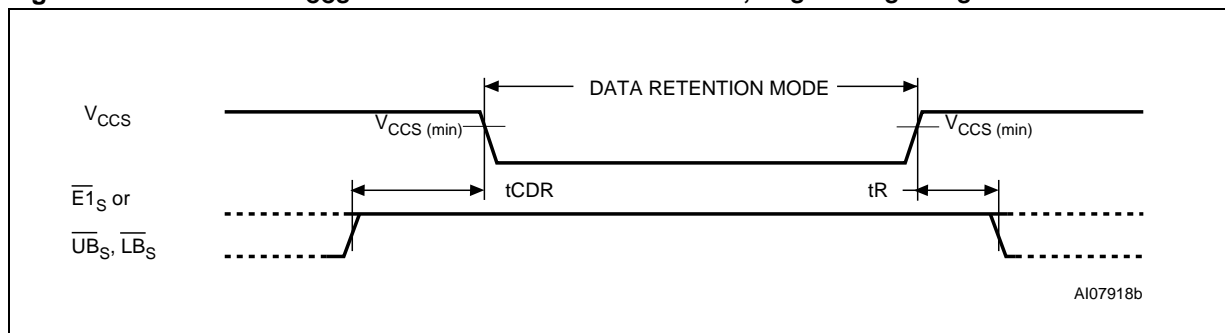


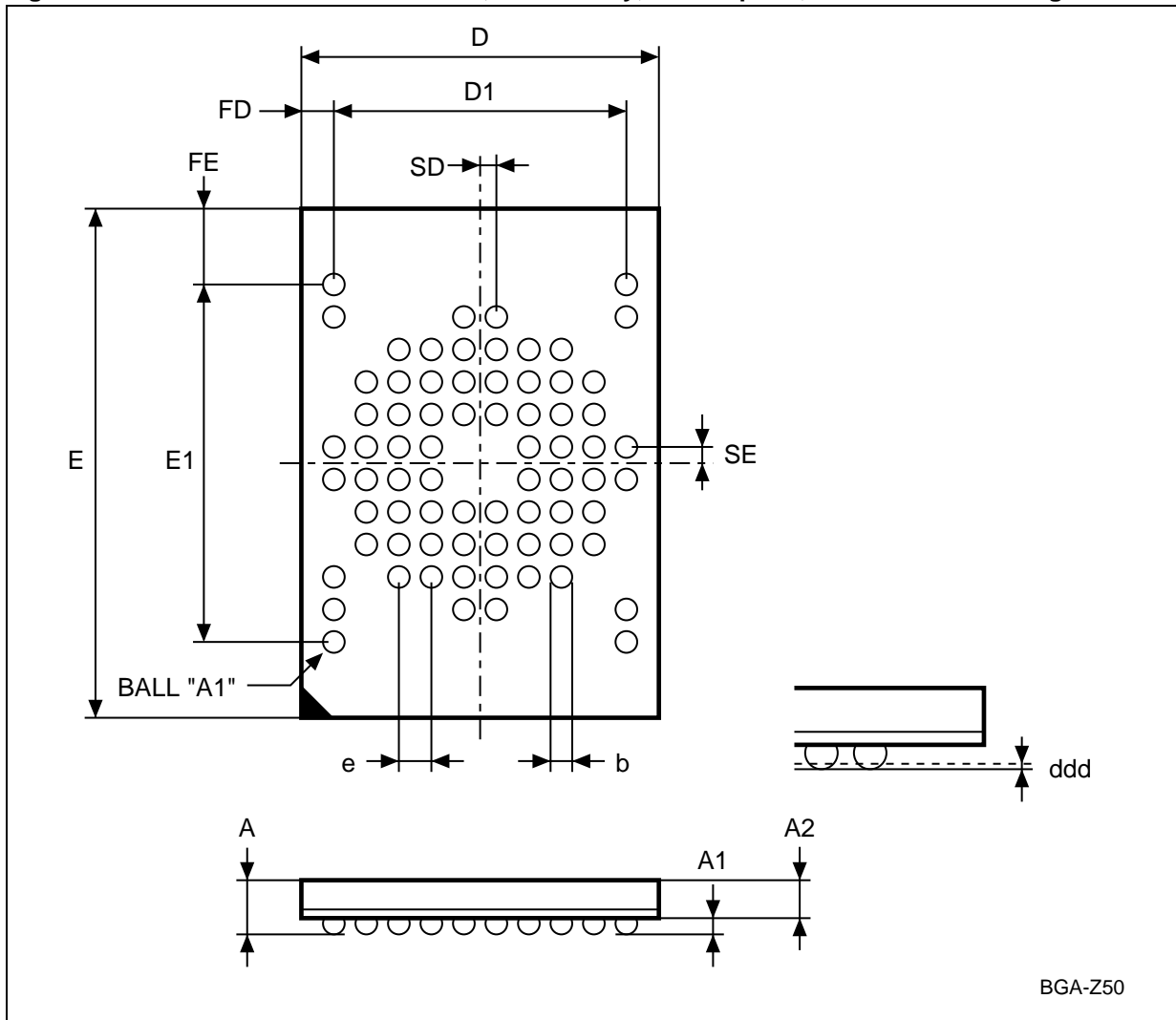
Table 10. SRAM Low V<sub>CCS</sub> Data Retention Characteristic

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I <sub>CCDR</sub>	Supply Current (Data Retention)	V <sub>CCS</sub> = 1.5V, $\overline{E1}_S \geq V_{CCS} - 0.2V$ , V <sub>IN</sub> ≥ V <sub>CCS</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V		3	10	μA
V <sub>DR</sub>	Supply Voltage (Data Retention)		1.5		3.3	V
t <sub>CDR</sub>	Chip Disable to Power Down		0			ns
t <sub>R</sub>	Operation Recovery Time		70			ns

2. Sampled only. Not 100% tested.

PACKAGE MECHANICAL

Figure 16. Stacked LFBGA73 8x11.6mm, 10x12 array, 0.8mm pitch, Bottom View Package Outline



Note: Drawing is not to scale.

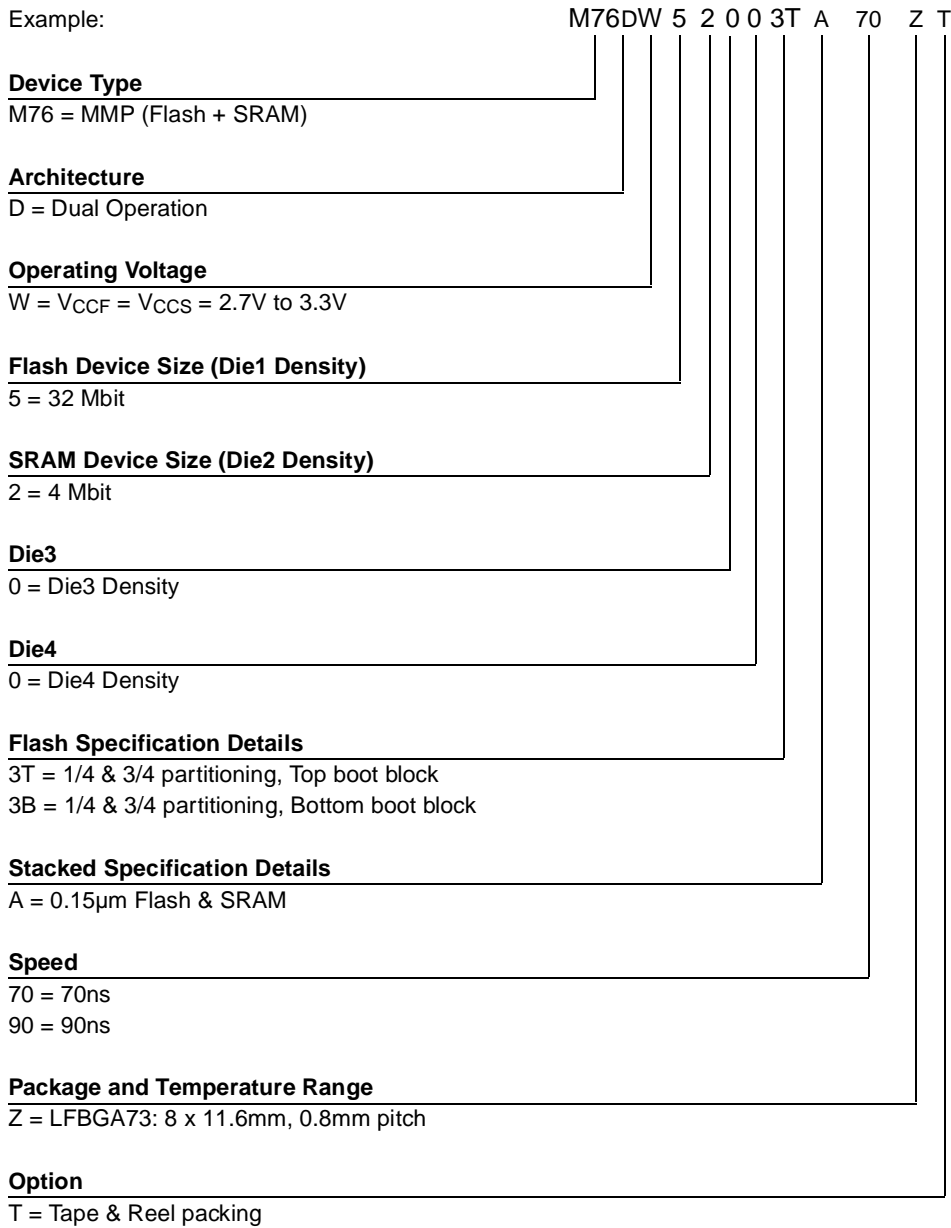
**M76DW52003TA, M76DW52003BA****Table 11. Stacked LFBGA73 8x11.6mm, 10x12 array, 0.8mm pitch, Package Mechanical Data**

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.400			0.0551
A1		0.250			0.0098	
A2	0.910			0.0358		
b	0.400	0.350	0.450	0.0157	0.0138	0.0177
D	8.000	7.900	8.100	0.3150	0.3110	0.3189
D1	7.200			0.2835		
ddd			0.100			0.0039
E	11.600	11.500	11.700	0.4567	0.4528	0.4606
E1	8.800			0.3465		
e	0.800	–	–	0.0315	–	–
FD	0.400			0.0157		
FE	1.400			0.0551		
SD	0.400	–	–	0.0157	–	–
SE	0.400	–	–	0.0157	–	–



**PART NUMBERING**

**Table 12. Ordering Information Scheme**



Devices are shipped from the factory with the memory content bits erased to '1'.

For a list of available options (Speed, Package, etc.) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

**REVISION HISTORY**

**Table 13. Document Revision History**

Date	Version	Revision Details
07-Jul-2003	1.0	First Issue
23-Sep-2003	1.1	Voltage supply range extended 2.7V working at all speed options

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