MAC97 Series

Preferred Device

Sensitive Gate Triacs

Silicon Bidirectional Thyristors

Designed for use in solid state relays, MPU interface, TTL logic and any other light industrial or consumer application. Supplied in an inexpensive TO−92 package which is readily adaptable for use in automatic insertion equipment.

Features

- One−Piece, Injection−Molded Package
- Blocking Voltage to 600 Volts
- Sensitive Gate Triggering in Four Trigger Modes (Quadrants) for all possible Combinations of Trigger Sources, and especially for Circuits that Source Gate Drives
- All Diffused and Glassivated Junctions for Maximum Uniformity of Parameters and Reliability
- Pb−Free Packages are Available*

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (T_J = −40 to +110°C) (Note 1) Sine Wave 50 to 60 Hz, Gate Open MAC97A4 MAC97A6 MAC97A8	V_{DRM}, V_{RRM}	 200 400 600	V
On-State RMS Current Full Cycle Sine Wave 50 to 60 Hz (T_C = +50°C)	$I_{T(RMS)}$	0.6	A
Peak Non−Repetitive Surge Current One Full Cycle, Sine Wave 60 Hz (T_C = 110°C)	I_{TSM}	8.0	A
Circuit Fusing Considerations (t = 8.3 ms)	I^2t	0.26	A^2s
Peak Gate Voltage ($t \le 2.0$ μs, T_C = +80°C)	V_{GM}	5.0	V
Peak Gate Power ($t \le 2.0$ μs, T_C = +80°C)	P_{GM}	5.0	W
Average Gate Power (T_C = 80°C, $t \le 8.3$ ms)	$P_{G(AV)}$	0.1	W
Peak Gate Current ($t \le 2.0$ μs, T_C = +80°C)	I_{GM}	1.0	A
Operating Junction Temperature Range	T_J	−40 to +110	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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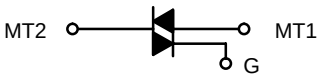
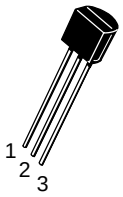
http://onsemi.com

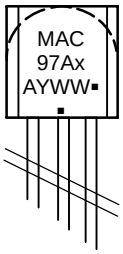
TRIACS
0.8 AMPERE RMS
200 thru 600 VOLTS



MARKING DIAGRAMS



TO−92 (TO−226AA)
CASE 029
STYLE 12



MAC97Ax = Device Code
x = 4, 6, or 8
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENT	
1	Main Terminal 1
2	Gate
3	Main Terminal 2

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

THERMAL CHARACTERISTICS

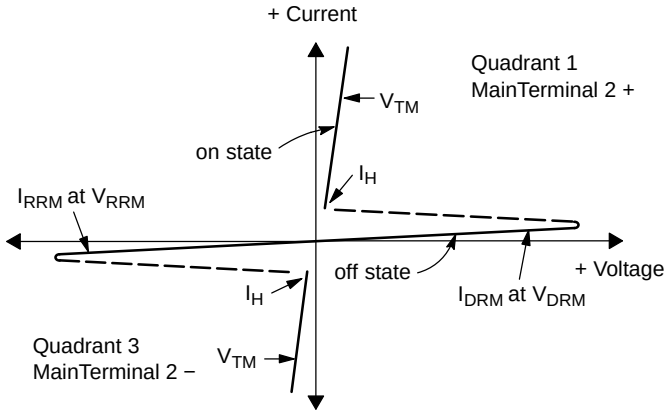
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	75	°C/W
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	200	°C/W
Maximum Lead Temperature for Soldering Purposes for 10 Seconds	T_L	260	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted; Electricals apply in both directions)

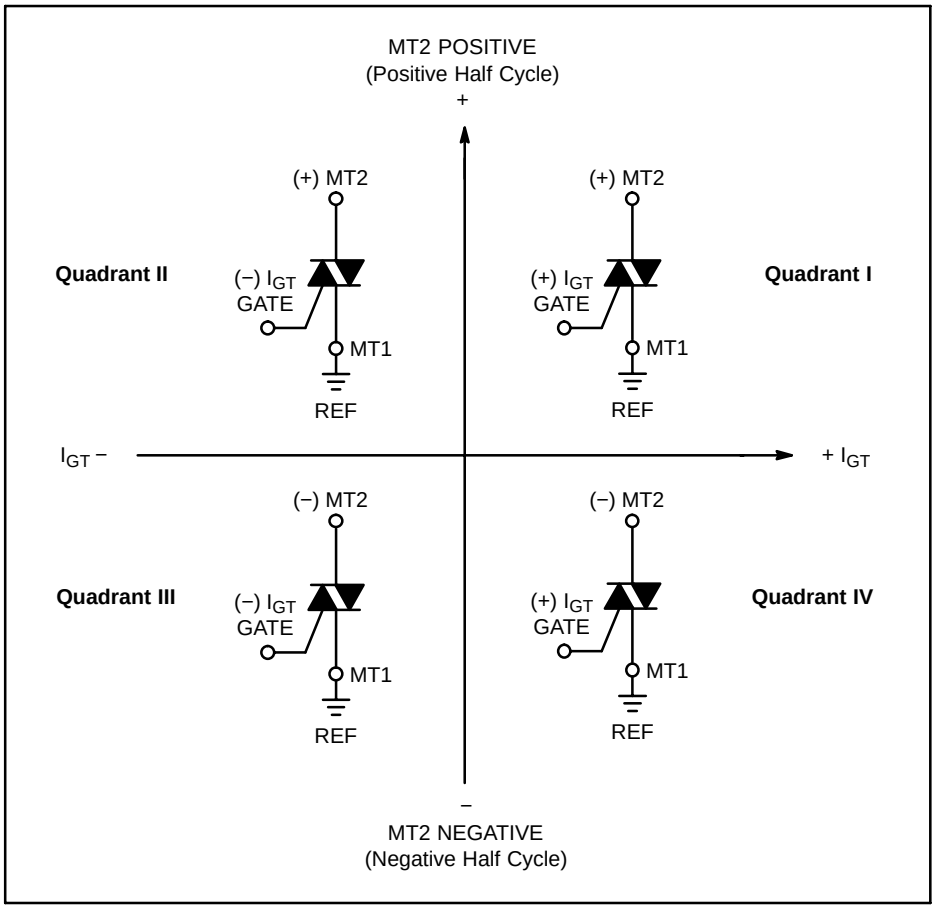
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Peak Repetitive Blocking Current (V_D = Rated V_{DRM}, V_{RRM}; Gate Open) T_J = 25°C T_J = +110°C	I_{DRM}, I_{RRM}	 − −	 − −	 10 100	 μA μA
ON CHARACTERISTICS					
Peak On−State Voltage (I_{TM} = ±.85 A Peak; Pulse Width ≤ 2.0 ms, Duty Cycle ≤ 2.0%)	V_{TM}	−	−	1.9	V
Gate Trigger Current (Continuous dc) (V_D = 12 Vdc, R_L = 100 Ω) MT2(+), G(+) MT2(+), G(−) MT2(−), G(−) MT2(−), G(+)	I_{GT}	 − − − −	 − − − −	 5.0 5.0 5.0 7.0	mA
Gate Trigger Voltage (Continuous dc) (V_D = 12 Vdc, R_L = 100 Ω) MT2(+), G(+) All Types MT2(+), G(−) All Types MT2(−), G(−) All Types MT2(−), G(+) All Types	V_{GT}	 − − − −	 .66 .77 .84 .88	 2.0 2.0 2.0 2.5	V
Gate Non−Trigger Voltage (V_D = 12 V, R_L = 100 Ω, T_J = 110°C) All Four Quadrants	V_{GD}	0.1	−	−	V
Holding Current (V_D = 12 Vdc, Initiating Current = 200 mA, Gate Open)	I_H	−	1.5	10	mA
Turn-On Time (V_D = Rated V_{DRM}, I_{TM} = 1.0 A pk, I_G = 25 mA)	t_{gt}	−	2.0	−	μs
DYNAMIC CHARACTERISTICS					
Critical Rate−of−Rise of Commutation Voltage (V_D = Rated V_{DRM}, I_{TM} = .84 A, Commutating di/dt = .3 A/ms, Gate Unenergized, T_C = 50°C)	dV/dt(c)	−	5.0	−	V/μs
Critical Rate of Rise of Off−State Voltage (V_D = Rated V_{DRM}, T_C = 110°C, Gate Open, Exponential Waveform	dv/dt	−	25	−	V/μs

Voltage Current Characteristic of Triacs (Bidirectional Device)

Symbol	Parameter
V_{DRM}	Peak Repetitive Forward Off State Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Reverse Off State Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Maximum On State Voltage
I_H	Holding Current



Quadrant Definitions for a Triac



All polarities are referenced to MT1.
With in−phase signals (using standard AC lines) quadrants I and III are used.

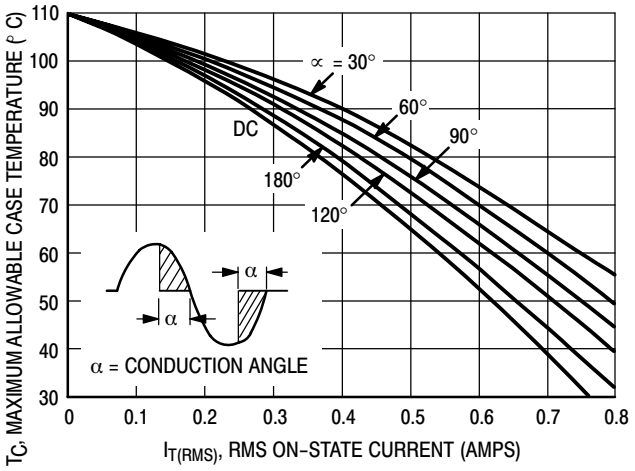


Figure 1. RMS Current Derating

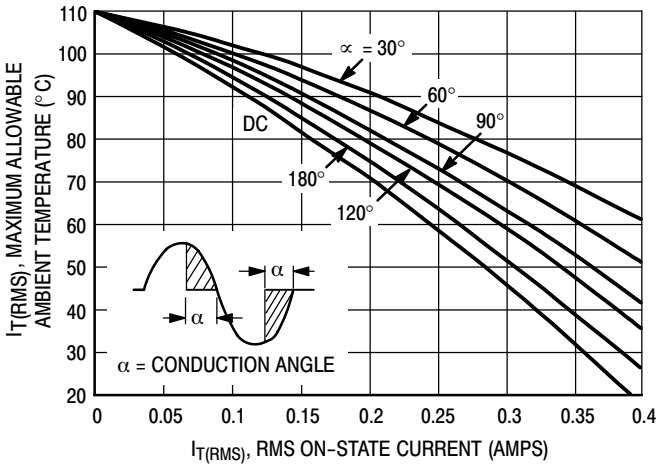


Figure 2. RMS Current Derating

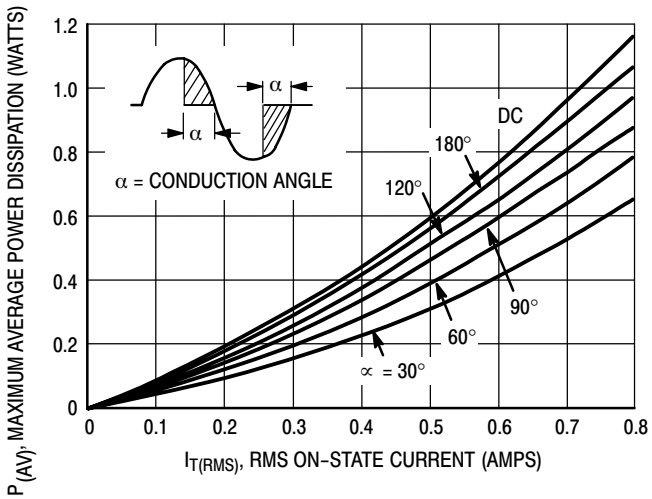


Figure 3. Power Dissipation

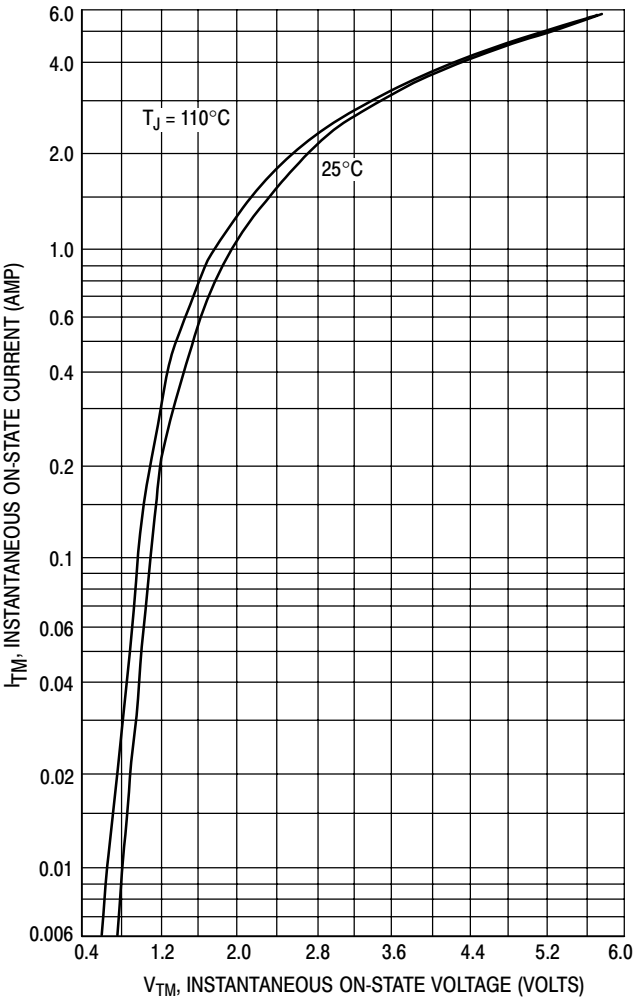


Figure 4. On−State Characteristics

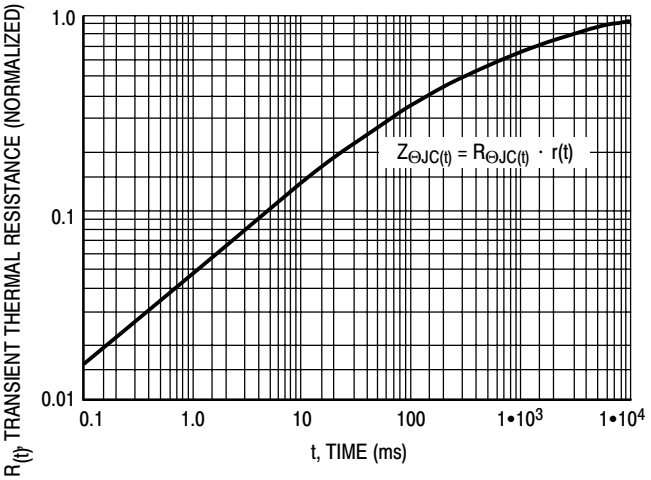


Figure 5. Transient Thermal Response

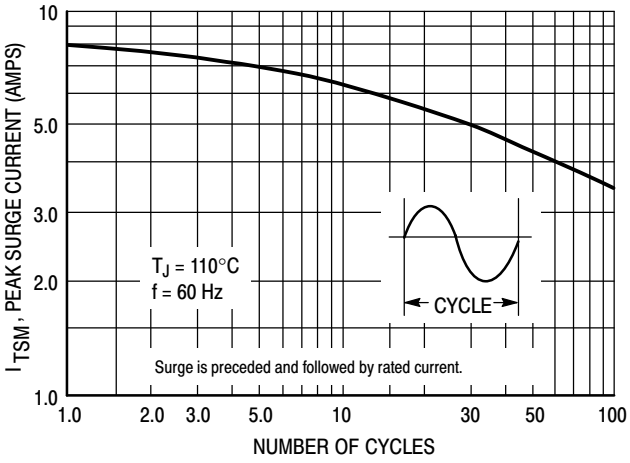


Figure 6. Maximum Allowable Surge Current

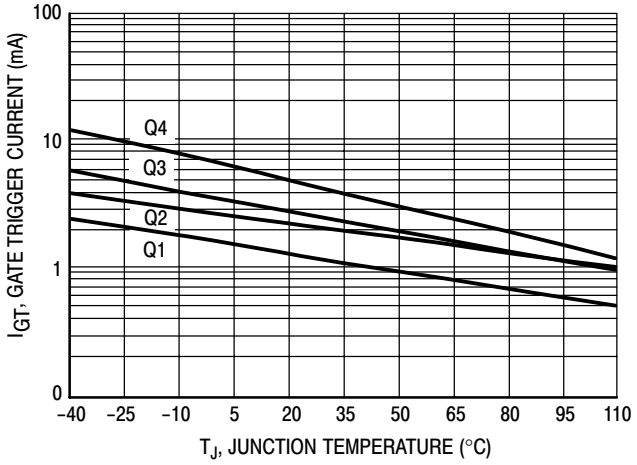


Figure 7. Typical Gate Trigger Current versus Junction Temperature

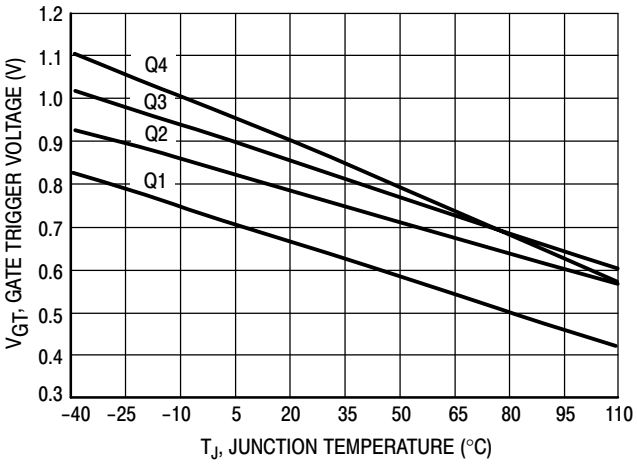


Figure 8. Typical Gate Trigger Voltage versus Junction Temperature

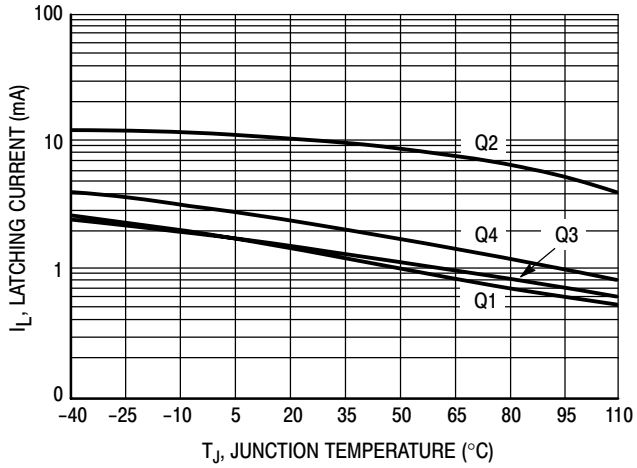


Figure 9. Typical Latching Current versus Junction Temperature

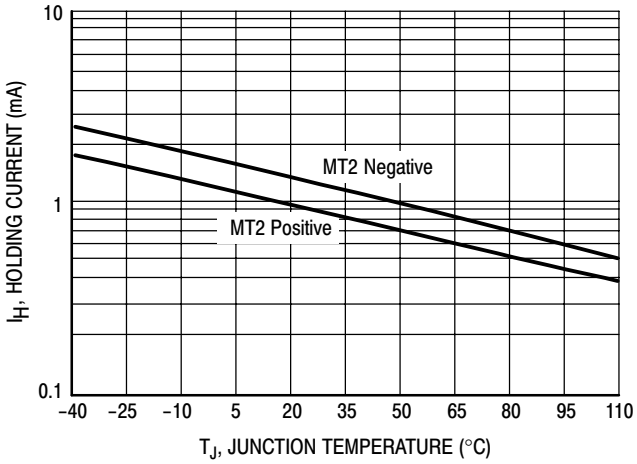
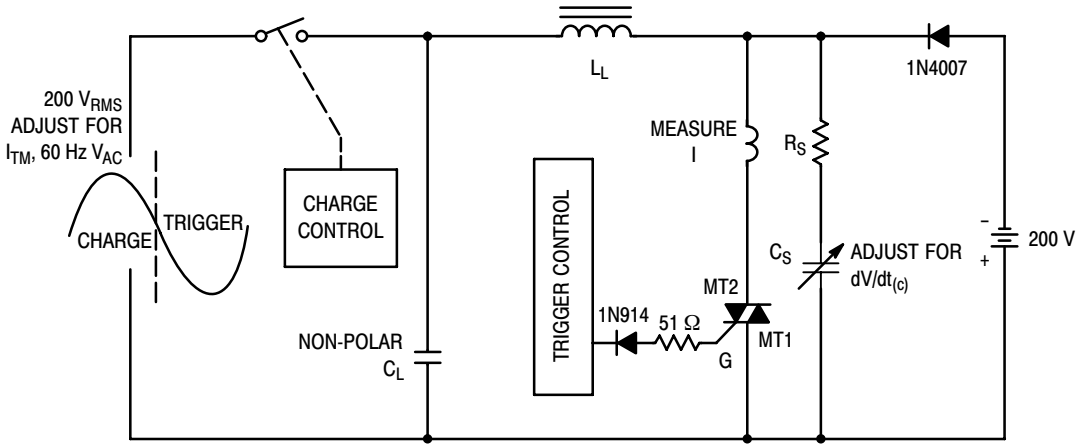


Figure 10. Typical Holding Current versus Junction Temperature



Note: Component values are for verification of rated $(dv/dt)_c$. See AN1048 for additional information.

Figure 11. Simplified Test Circuit to Measure the Critical Rate of Rise of Commutating Voltage $(dV/dt)_c$

ORDERING & SHIPPING INFORMATION

U.S.	Europe Equivalent	Shipping	Description of TO92 Tape Orientation
	MAC97A6RL1	Radial Tape & Reel (2K/Reel)	Flat side of TO92 & adhesive tape visible
	MAC97A6RL1G	Radial Tape & Reel (2K/Reel) (Pb−Free)	Flat side of TO92 & adhesive tape visible
MAC97A8RLRM	MAC97A8RL1	Radial Tape & Reel (2K/Reel)	Flat side of TO92 & adhesive tape visible
MAC97A8RLRMG	MAC97A8RL1G	Radial Tape & Reel (2K/Reel) (Pb−Free)	Flat side of TO92 & adhesive tape visible
MAC97A4		Bulk in Box (5K/Box)	N/A, Bulk
MAC97A4G		Bulk in Box (5K/Box) (Pb−Free)	N/A, Bulk
MAC97A6		Bulk in Box (5K/Box)	N/A, Bulk
MAC97A6G		Bulk in Box (5K/Box) (Pb−Free)	N/A, Bulk
MAC97A8		Bulk in Box (5K/Box)	N/A, Bulk
MAC97A8G		Bulk in Box (5K/Box) (Pb−Free)	N/A, Bulk
MAC97A6RLRF		Radial Tape & Reel (2K/Reel)	Round side of TO92 & adhesive tape on reverse side
MAC97A6RLRFG		Radial Tape & Reel (2K/Reel) (Pb−Free)	Round side of TO92 & adhesive tape on reverse side
MAC97A6RLRP		Radial Tape & Reel (2K/Reel)	Round side of TO92 & adhesive tape on reverse side
MAC97A6RLRPG		Radial Tape & Reel (2K/Reel) (Pb−Free)	Round side of TO92 & adhesive tape on reverse side
MAC97A8RLRP		Radial Tape / Fan Fold Box (2K/Box)	Round side of TO92 & adhesive tape visible
MAC97A8RLRPG		Radial Tape / Fan Fold Box (2K/Box) (Pb−Free)	Round side of TO92 & adhesive tape visible

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TO−92 EIA RADIAL TAPE IN FAN FOLD BOX OR ON REEL

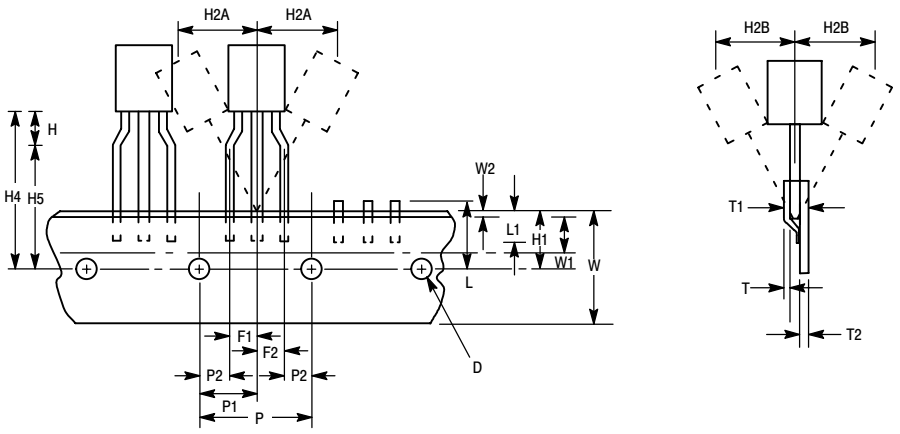


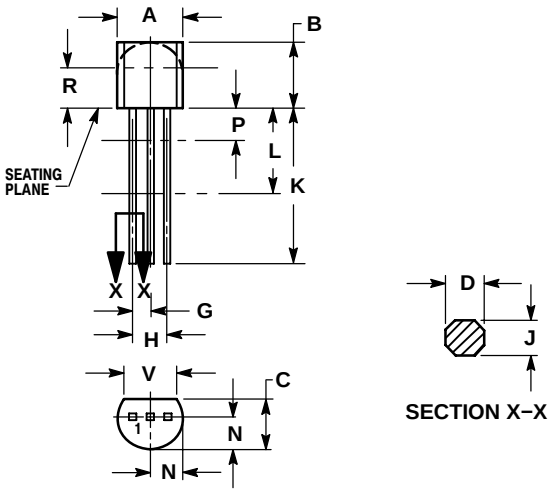
Figure 12. Device Positioning on Tape

Symbol	Item	Specification			
		Inches		Millimeter	
		Min	Max	Min	Max
D	Tape Feedhole Diameter	0.1496	0.1653	3.8	4.2
D2	Component Lead Thickness Dimension	0.015	0.020	0.38	0.51
F1, F2	Component Lead Pitch	0.0945	0.110	2.4	2.8
H	Bottom of Component to Seating Plane	.059	0.156	1.5	4.0
H1	Feedhole Location	0.3346	0.3741	8.5	9.5
H2A	Deflection Left or Right	0	0.039	0	1.0
H2B	Deflection Front or Rear	0	0.051	0	1.0
H4	Feedhole to Bottom of Component	0.7086	0.768	18	19.5
H5	Feedhole to Seating Plane	0.610	0.649	15.5	16.5
L	Defective Unit Clipped Dimension	0.3346	0.433	8.5	11
L1	Lead Wire Enclosure	0.09842	−	2.5	−
P	Feedhole Pitch	0.4921	0.5079	12.5	12.9
P1	Feedhole Center to Center Lead	0.2342	0.2658	5.95	6.75
P2	First Lead Spacing Dimension	0.1397	0.1556	3.55	3.95
T	Adhesive Tape Thickness	0.06	0.08	0.15	0.20
T1	Overall Taped Package Thickness	−	0.0567	−	1.44
T2	Carrier Strip Thickness	0.014	0.027	0.35	0.65
W	Carrier Strip Width	0.6889	0.7481	17.5	19
W1	Adhesive Tape Width	0.2165	0.2841	5.5	6.3
W2	Adhesive Tape Position	0.0059	0.01968	0.15	0.5

NOTES:
2. Maximum alignment deviation between leads not to be greater than 0.2 mm.
3. Defective components shall be clipped from the carrier tape such that the remaining protrusion (L) does not exceed a maximum of 11 mm.
4. Component lead to tape adhesion must meet the pull test requirements.
5. Maximum non−cumulative variation between tape feed holes shall not exceed 1 mm in 20 pitches.
6. Holddown tape not to extend beyond the edge(s) of carrier tape and there shall be no exposure of adhesive.
7. No more than 1 consecutive missing component is permitted.
8. A tape trailer and leader, having at least three feed holes is required before the first and after the last component.
9. Splices will not interfere with the sprocket feed holes.

PACKAGE DIMENSIONS

TO−92 (TO−226AA)
CASE 029−11
ISSUE AL



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.021	0.407	0.533
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.115	---	2.93	---
V	0.135	---	3.43	---

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082−1312 USA
Phone: 480−829−7710 or 800−344−3860 Toll Free USA/Canada
Fax: 480−829−7709 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

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2−9−1 Kamimeguro, Meguro−ku, Tokyo, Japan 153−0051
Phone: 81−3−5773−3850

ON Semiconductor Website: http://onsemi.com

Order Literature: http://www.onsemi.com/litorder

For additional information, please contact your local Sales Representative.

MAC97/D