



Dual SPDT Analog Switches with Over-Rail Signal Handling

General Description

The MAX4850/MAX4850H/MAX4852/MAX4852H family of dual SPDT (single-pole/double-throw) switches operate from a single +2V to +5.5V supply and can handle signals greater than the supply rail. These switches feature low 3.5Ω or 3.5Ω/7Ω on-resistance with low on-capacitance, making them ideal for switching audio and data signals.

The MAX4850/MAX4850H are configured with two SPDT switches and feature two comparators for headphone detection or mute/send key functions. The MAX4852 has two SPDT switches with no comparators for low 1μA supply current.

For over-rail applications, these devices offer either the pass-through or high-impedance option. For the MAX4850/MAX4852, the signal (up to 5.5V) passes through the switch without distortion even when the positive supply rail is exceeded. For the MAX4850H/MAX4852H, the switch input becomes high impedance when the input signal exceeds the supply rail.

The MAX4850/MAX4850H/MAX4852/MAX4852H are available in the space-saving (3mm x 3mm), 16-pin TQFN package and operate over the extended temperature range of -40°C to +85°C.

Applications

- USB Switching
- Audio-Signal Routing
- Cellular Phones
- Notebook Computers
- PDA's and Other Handheld Devices

Features

- ◆ USB 2.0 Full Speed (12MB) and USB 1.1 Signal Switching Compliant
- ◆ Switch Signals Greater than V_{CC}
- ◆ 0.1ns Differential Skew
- ◆ 3.5Ω/7Ω On-Resistance
- ◆ 135MHz -3dB Bandwidth
- ◆ +2V to +5.5V Supply Range
- ◆ 1.8V Logic Compatible
- ◆ Low Supply Current
1μA (MAX4852)
5μA (MAX4850)
10μA (MAX4850H/MAX4852H)
- ◆ Available in a Space-Saving (3mm x 3mm), 16-Pin TQFN Package

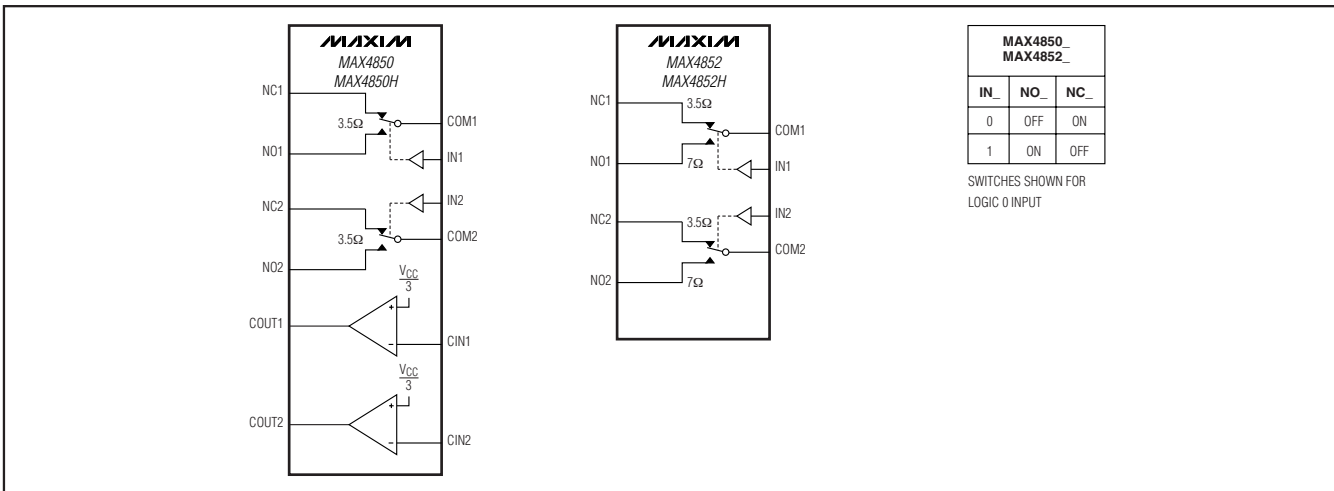
Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE | TOP MARK |
|-------------|----------------|-------------|----------|
| MAX4850ETE | -40°C to +85°C | 16 TQFN-EP* | ABU |
| MAX4850HETE | -40°C to +85°C | 16 TQFN-EP* | ABV |
| MAX4852ETE | -40°C to +85°C | 16 TQFN-EP* | ABZ |
| MAX4852HETE | -40°C to +85°C | 16 TQFN-EP* | ACA |

*EP = Exposed paddle.

Pin Configurations and Selector Guide appear at end of data sheet.

Block Diagrams/Truth Table



Dual SPDT Analog Switches with Over-Rail Signal Handling

ABSOLUTE MAXIMUM RATINGS

| | |
|---|-----------------------------|
| V_{CC} , IN_, CIN_, COM_, NO_, NC_ to GND (Note 1)..... | -0.3V to +6.0V |
| COU_..... | -0.3V to (V_{CC} + 0.3V) |
| COU_ Continuous Current..... | ±20mA |
| Closed Switch Continuous Current COM_, NO_, NC_ 3.5Ω Switch | ±100mA |
| 7Ω Switch | ±50mA |
| Peak Current COM_, NO_, NC_ (pulsed at 1ms, 50% duty cycle) 3.5Ω Switch | ±200mA |
| 7Ω Switch | ±100mA |

| | |
|---|-----------------|
| Peak Current COM_, NO_, NC_ (pulsed at 1ms, 10% duty cycle) 3.5Ω Switch | ±240mA |
| 7Ω Switch | ±120mA |
| Continuous Power Dissipation (T_A = +70°C) 16-Pin TQFN (derate 20.8mW/°C above +70°C)..... | 1667mW |
| Operating Temperature Range | -40°C to +85°C |
| Junction Temperature | +150°C |
| Storage Temperature Range | -65°C to +150°C |
| Lead Temperature (soldering, 10s) | +300°C |

Note 1: Signals on IN, NO, NC, or COM below GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.0V, T_A = +25°C, unless otherwise noted.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---------------------------------------|--|------------------------|-------|-------|-------|
| Supply Voltage | V_{CC} | | 2.0 | | 5.5 | V |
| Supply Current | I_{CC} | V_{CC} = 5.5V, V_{IN_+} = 0V or V_{CC} | MAX4850 | 5 | 10 | μA |
| | | | MAX4850H/ MAX4852H | 10 | 20 | |
| | | | MAX4852 | | 1 | |
| ANALOG SWITCH (3.5Ω Switch) | | | | | | |
| Analog Signal Range | V_{NO_-} , V_{NC_-} , V_{COM_-} | | 0 | | 5.5 | V |
| On-Resistance (Note 3) | R_{ON} | V_{CC} = 3V, I_{COM_-} = 10mA, V_{NC_-} or V_{NO_-} = 0 to 5.5V (MAX485_) or V_{CC} (MAX485_H) | T_A = +25°C | 3.5 | 4.5 | Ω |
| | | | T_A = -40°C to +85°C | | 5 | |
| On-Resistance Match Between Channels (Notes 3, 4) | ΔR_{ON} | V_{CC} = 3V, I_{COM_-} = 10mA, V_{NC_-} or V_{NO_-} = 1.5V | T_A = +25°C | 0.1 | 0.2 | Ω |
| | | | T_A = -40°C to +85°C | | 0.25 | |
| On-Resistance Flatness (Note 5) | R_{FLAT} | V_{CC} = 3V, I_{COM_-} = 10mA, V_{NC_-} or V_{NO_-} = 1V, 2V, 3V | T_A = +25°C | 1.2 | 1.8 | Ω |
| | | | T_A = -40°C to +85°C | | 2 | |
| NO_/NC_ Off-Leakage Current | I_{OFF} | V_{CC} = 5.5V, V_{NC_-} or V_{NO_-} = 1V or 4.5V, V_{COM_-} = 4.5V or 1V | T_A = +25°C | -2 | +2 | nA |
| | | | T_A = -40°C to +85°C | -10 | +10 | |
| COM_ On-Leakage Current | I_{ON} | V_{CC} = 5.5V; V_{NC_-} or V_{NO_-} = 1V, 4.5V, or floating; V_{COM_-} = 1V, 4.5V, or floating | T_A = +25°C | -2 | +2 | nA |
| | | | T_A = -40°C to +85°C | -12.5 | +12.5 | |
| -3dB Bandwidth | BW | Signal = 0dBm, R_L = 50Ω, C_L = 5pF (Figure 5) | | 100 | | MHz |
| NO_/NC_ Off-Capacitance | C_{OFF} | f = 1MHz (Figure 6) | | 20 | | pF |

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MAX4850/MAX4850H/MAX4852/MAX4852H

ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +2.7V$ to $+5.5V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Typical values are at $V_{CC} = +3.0V$, $T_A = +25^{\circ}C$, unless otherwise noted.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|--|--|--|-------|-------|----------|
| COM On-Capacitance | C_{ON} | $f = 1MHz$ (Figure 6) | | 60 | | pF |
| ANALOG SWITCH (7Ω Switch) | | | | | | |
| Analog Signal Range | $V_{NO_}$, $V_{NC_}$, $V_{COM_}$ | | 0 | | 5.5 | V |
| On-Resistance | R_{ON} | $V_{CC} = 3V$, $I_{COM_} = 10mA$, $V_{NC_}$ or $V_{NO_} = 0$ to $5.5V$ (MAX4852) or V_{CC} (MAX4852H) | $T_A = +25^{\circ}C$ | 7 | 9 | Ω |
| | | | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ | | 10 | |
| On-Resistance Match Between Channels (Notes 3, 4) | ΔR_{ON} | $V_{CC} = 3V$, $I_{COM_} = 10mA$, $V_{NC_}$ or $V_{NO_} = 1.5V$ | $T_A = +25^{\circ}C$ | 0.2 | 0.4 | Ω |
| | | | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ | | 0.5 | |
| On-Resistance Flatness (Note 5) | R_{FLAT} | $V_{CC} = 3V$, $I_{COM_} = 10mA$, $V_{NC_}$ or $V_{NO_} = 1V, 2V, 3V$ | $T_A = +25^{\circ}C$ | 2.5 | 3.75 | Ω |
| | | | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ | | 4.0 | |
| NO_/NC_ Off-Leakage Current | I_{OFF} | $V_{CC} = 5.5V$, $V_{NC_}$ or $V_{NO_} = 1V$ or $4.5V$, $V_{COM_} = 4.5V$ or $1V$ | $T_A = +25^{\circ}C$ | -2 | +2 | nA |
| | | | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ | -10 | +10 | |
| COM_ On-Leakage Current | I_{ON} | $V_{CC} = 5.5V$; $V_{NC_}$ or $V_{NO_} = 1V, 4.5V$, or floating; $V_{COM_} = 1V, 4.5V$, or floating | $T_A = +25^{\circ}C$ | -2 | +2 | nA |
| | | | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ | -12.5 | +12.5 | |
| -3dB Bandwidth | BW | Signal = 0dBm, $R_L = 50\Omega$, $C_L = 5pF$ (Figure 5) | | 135 | | MHz |
| NO_/NC_ Off-Capacitance | C_{OFF} | $f = 1MHz$ (Figure 6) | | 12 | | pF |
| COM On-Capacitance | C_{ON} | $f = 1MHz$ (Figure 6) | | 50 | | pF |
| DYNAMIC CHARACTERISTICS | | | | | | |
| Signal Over-Rail to High-Z Switching Time | t_{HIZ} | MAX4850H/MAX4852H, $V_{NO_}$ or $V_{NC_} = V_{CC}$ to $(V_{CC} + 0.5V)$, $V_{CC} < 5V$ (Figure 1) | | 0.5 | 1 | μs |
| High-Z to Low-Z Switching Time | t_{HIZB} | MAX4850H/MAX4852H, $V_{NO_}$ or $V_{NC_} = (V_{CC} + 0.5V)$ to V_{CC} , $V_{CC} < 5V$ (Figure 1) | | 0.5 | 1 | μs |
| Skew (Note 3) | t_{SKEW} | $R_S = 39\Omega$, $C_L = 50pF$ (Figure 2) | | 0.1 | 1 | ns |
| Propagation Delay (Note 3) | t_{PD} | $R_S = 39\Omega$, $C_L = 50pF$ (Figure 2) | | 0.9 | 2 | ns |
| Turn-On Time | t_{ON} | $V_{CC} = 3V$, $V_{NO_}$ or $V_{NC_} = 1.5V$, $R_L = 300\Omega$, $C_L = 50pF$ (Figure 1) | $T_A = +25^{\circ}C$ | 40 | 60 | ns |
| | | | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ | | 100 | |
| Turn-Off Time | t_{OFF} | $V_{CC} = 3V$, $V_{NO_}$ or $V_{NC_} = 1.5V$, $R_L = 300\Omega$, $C_L = 50pF$ (Figure 1) | $T_A = +25^{\circ}C$ | 30 | 40 | ns |
| | | | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ | | 60 | |

Dual SPDT Analog Switches with Over-Rail Signal Handling

ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +2.7V$ to $+5.5V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Typical values are at $V_{CC} = +3.0V$, $T_A = +25^{\circ}C$, unless otherwise noted.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------------------|-----------|---|--|----------------------|----------------------|---------|
| Break-Before-Make Time Delay (Note 3) | t_D | $V_{CC} = 3V$, $V_{NO_}$ or $V_{NC_} = 1.5V$, $R_L = 300\Omega$, $C_L = 50pF$ (Figure 3) | $T_A = +25^{\circ}C$ | 15 | | ns |
| | | | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ | 2 | | |
| Charge Injection | Q | $V_{COM_} = 1.5V$, $R_S = 0\Omega$, $C_L = 1nF$ (Figure 4) | 8 | | pC | |
| Off-Isolation (Note 6) | V_{ISO} | $f = 100kHz$, $V_{COM_} = 1V_{RMS}$, $R_L = 50\Omega$, $C_L = 5pF$ (Figure 5) | -80 | | dB | |
| Crosstalk | V_{CT} | $f = 1MHz$, $V_{COM_} = 1V_{RMS}$, $R_L = 50\Omega$, $C_L = 5pF$ (Figure 5) | -95 | | dB | |
| Total Harmonic Distortion | THD | $f = 20Hz$ to $20kHz$, $V_{COM_} = 1V + 2V_{P-P}$, $R_L = 600\Omega$ | 0.04 | | % | |
| DIGITAL I/O (IN_) | | | | | | |
| Input-Logic High Voltage | V_{IH} | $V_{CC} = 2V$ to $3.6V$ | 1.4 | | V | |
| | | $V_{CC} = 3.6V$ to $5.5V$ | 1.8 | | | |
| Input-Logic Low Voltage | V_{IL} | $V_{CC} = 2V$ to $3.6V$ | 0.5 | | V | |
| | | $V_{CC} = 3.6V$ to $5.5V$ | 0.8 | | | |
| Input Leakage Current | I_{IN} | $V_{IN_} = 0$ or $5.5V$ | -0.5 | +0.5 | | μA |
| COMPARATOR | | | | | | |
| Comparator Range | | | 0 | 5.5 | | V |
| Comparator Threshold | V_{TH} | $V_{CC} = 2V$ to $5.5V$, falling input | $0.3 \times V_{CC}$ | $0.33 \times V_{CC}$ | $0.36 \times V_{CC}$ | V |
| Comparator Hysteresis | | $V_{CC} = 2V$ to $5.5V$ | 50 | | mV | |
| Comparator Output High Voltage | | $I_{SOURCE} = 1mA$ | $V_{CC} - 0.4V$ | | V | |
| Comparator Output Low Voltage | | $I_{SINK} = 1mA$ | 0.4 | | V | |
| Comparator Switching Time | | Rising input (Figure 7) | 2.5 | | μs | |
| | | Falling input (Figure 7) | 0.5 | | | |

Note 2: Specifications are 100% tested at $T_A = +85^{\circ}C$ only, and guaranteed by design and characterization over the specified temperature range.

Note 3: Guaranteed by design and characterization; not production tested.

Note 4: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.

Note 5: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

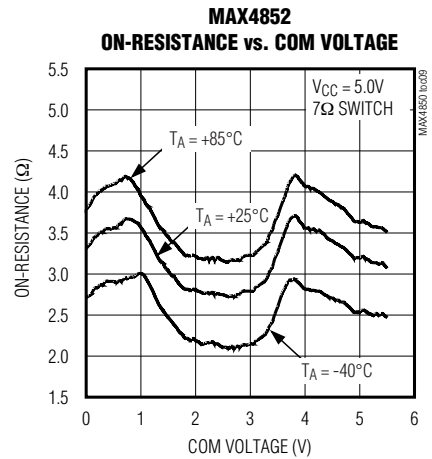
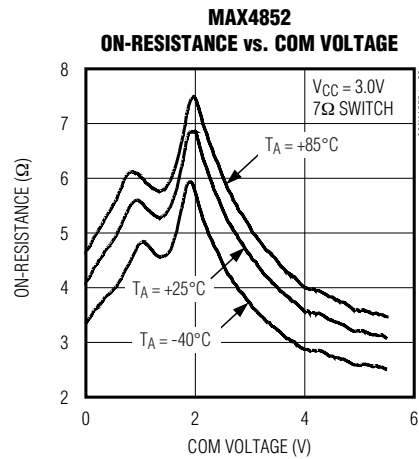
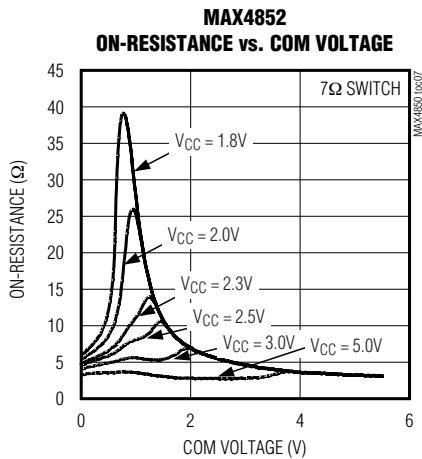
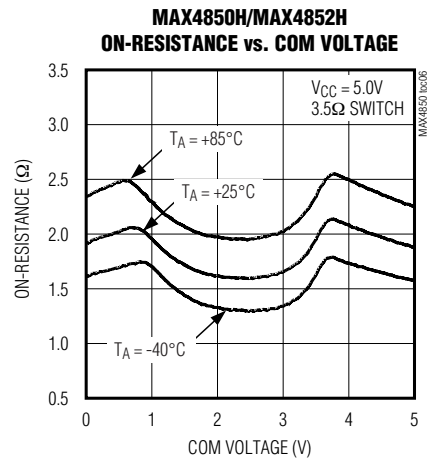
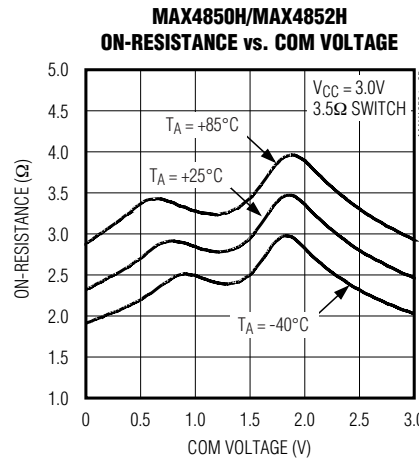
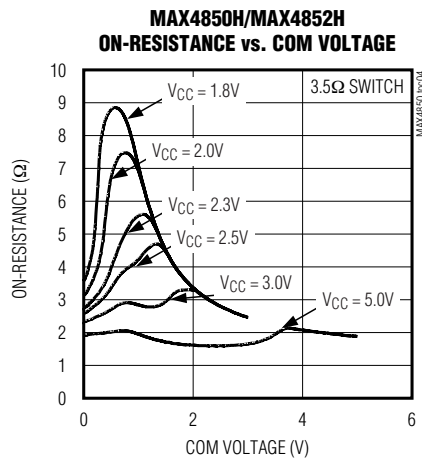
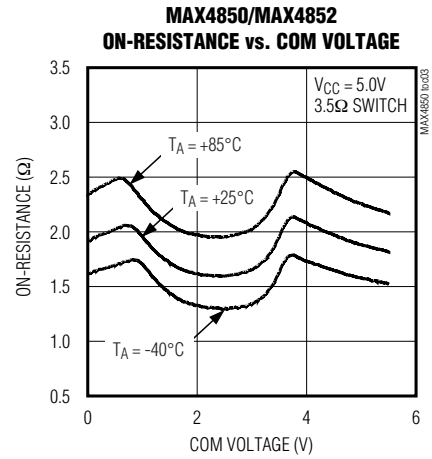
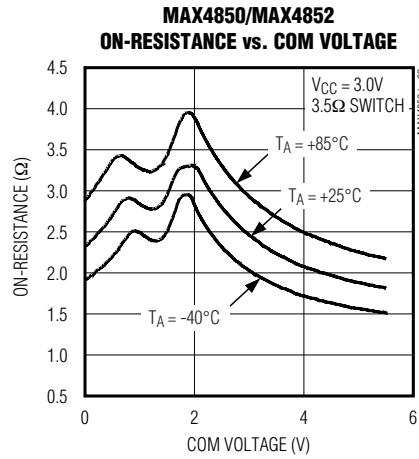
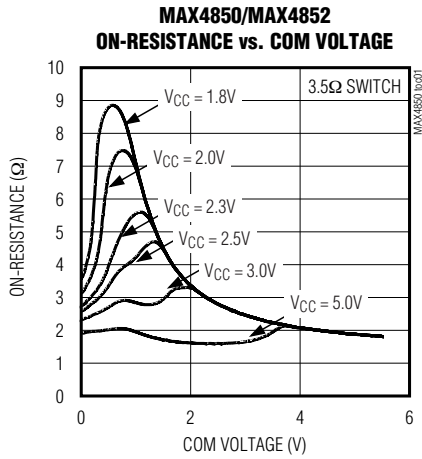
Note 6: Off-isolation = $20\log_{10}(V_{COM_} / V_{NO_})$, $V_{COM_}$ = output, $V_{NO_}$ = input to off switch.

Dual SPDT Analog Switches with Over-Rail Signal Handling

Typical Operating Characteristics

($V_{CC} = 3.0V$, $T_A = +25^\circ C$, unless otherwise noted.)

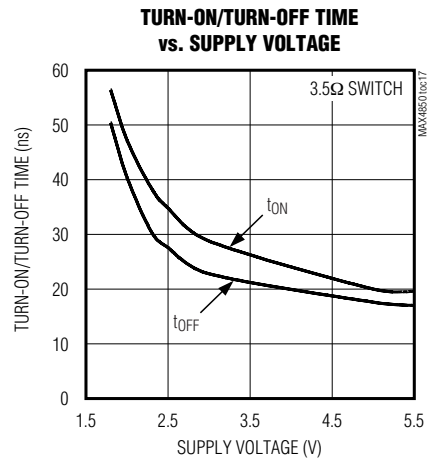
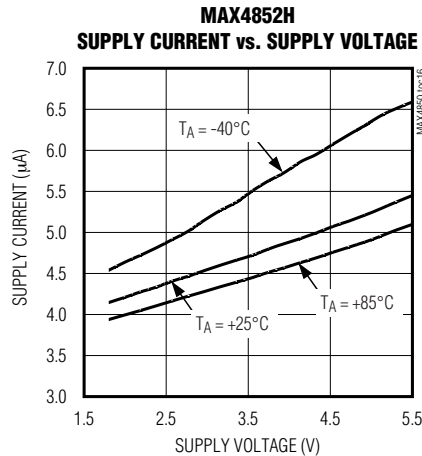
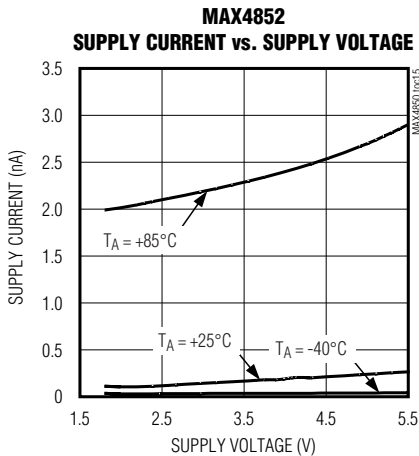
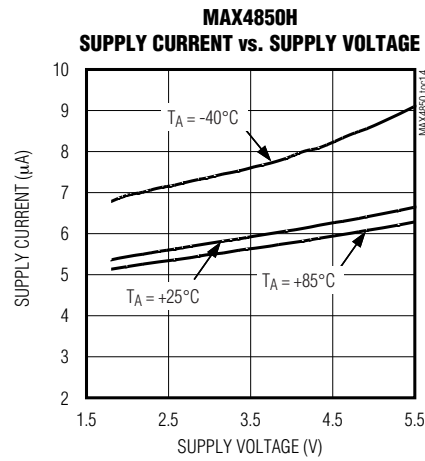
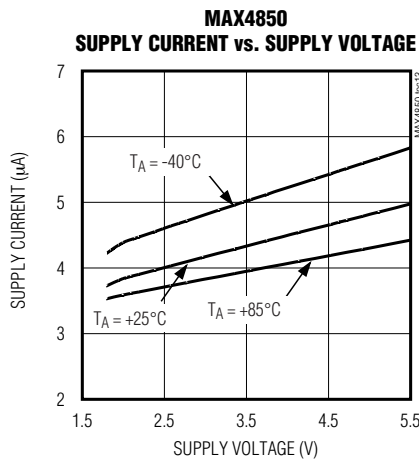
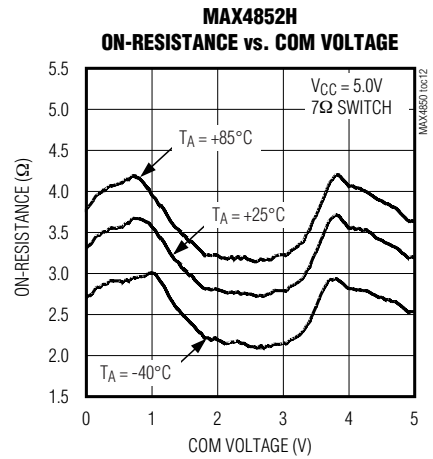
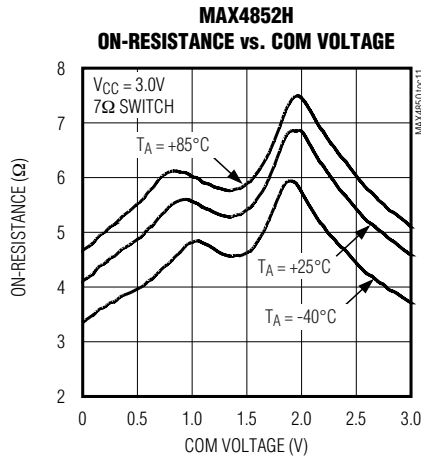
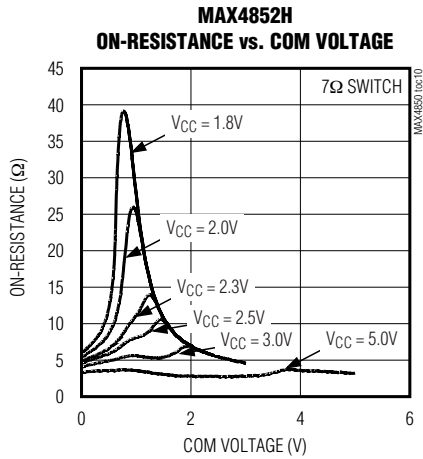
MAX4850/MAX4850H/MAX4852/MAX4852H



Dual SPDT Analog Switches with Over-Rail Signal Handling

Typical Operating Characteristics (continued)

($V_{CC} = 3.0V$, $T_A = +25^\circ C$, unless otherwise noted.)

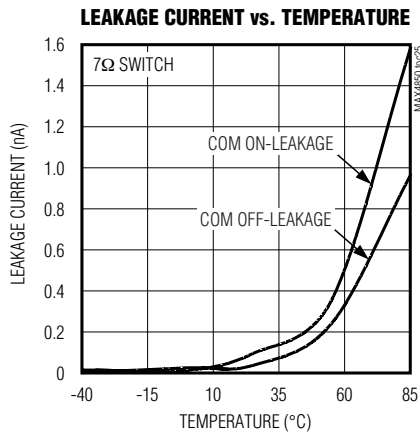
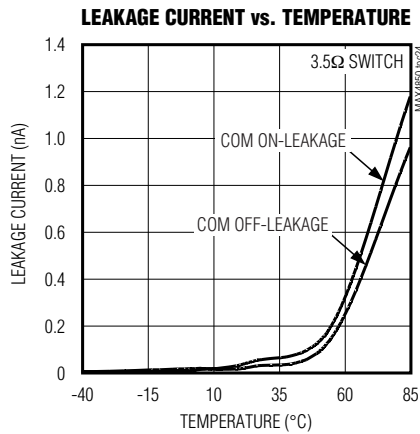
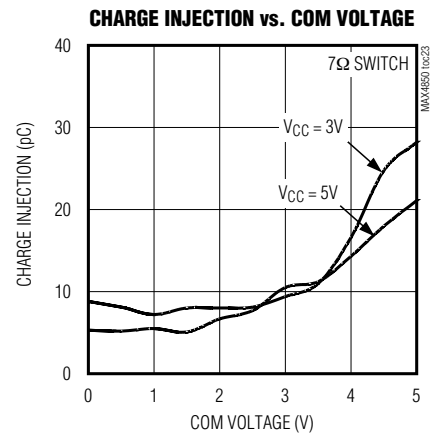
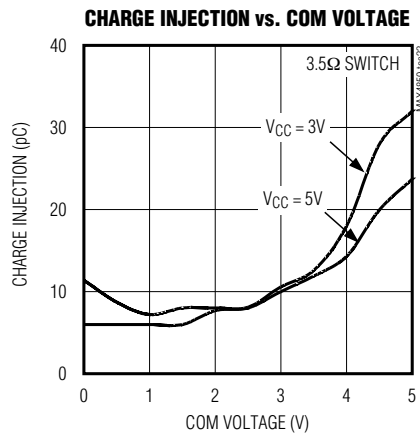
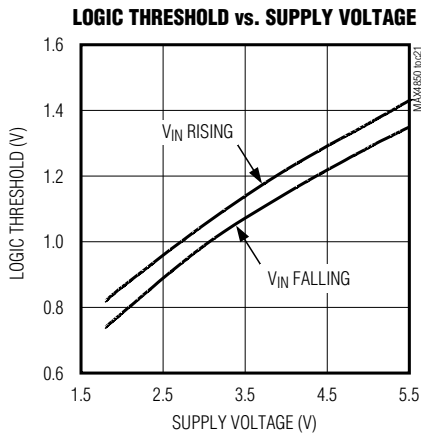
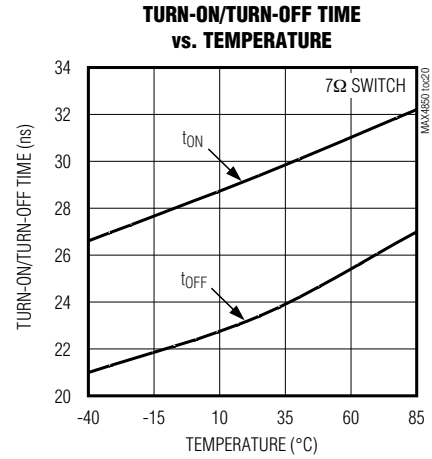
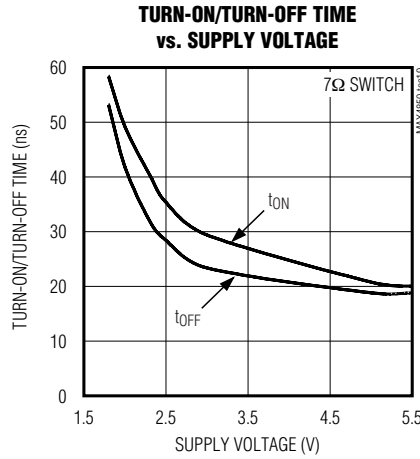
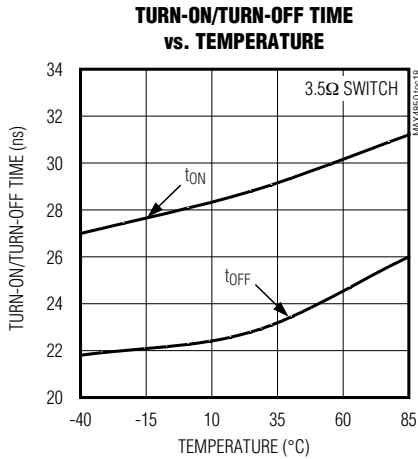


Dual SPDT Analog Switches with Over-Rail Signal Handling

Typical Operating Characteristics (continued)

($V_{CC} = 3.0V$, $T_A = +25^\circ C$, unless otherwise noted.)

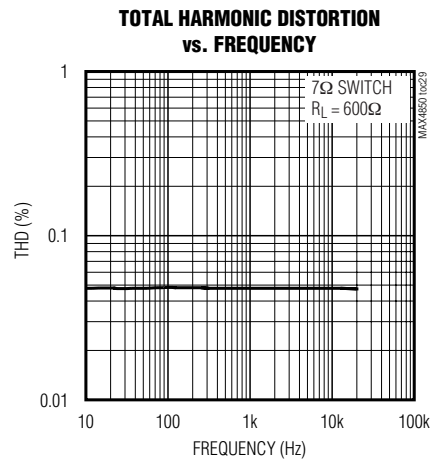
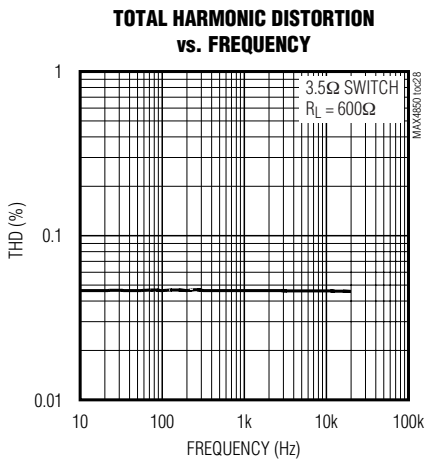
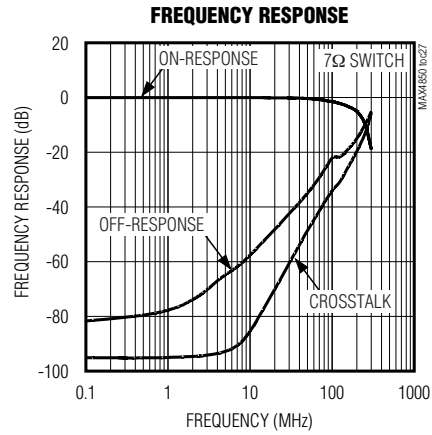
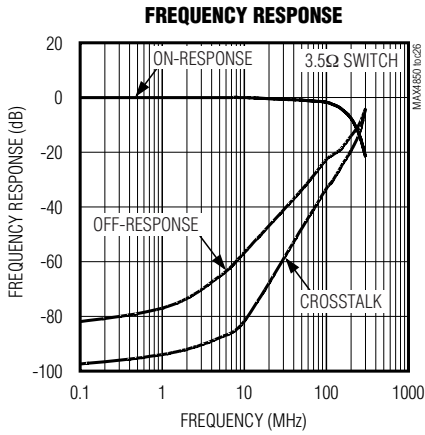
MAX4850/MAX4850H/MAX4852/MAX4852H



Dual SPDT Analog Switches with Over-Rail Signal Handling

Typical Operating Characteristics (continued)

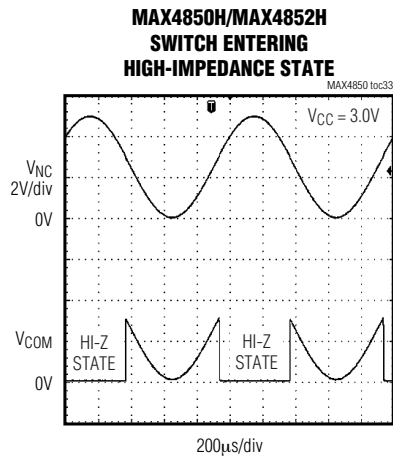
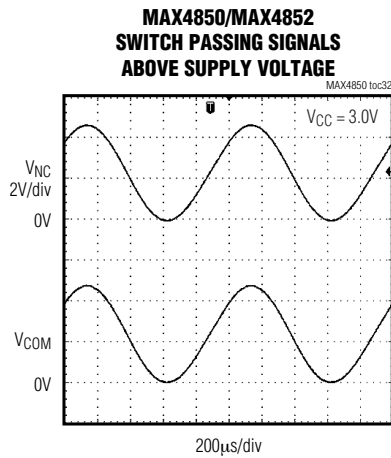
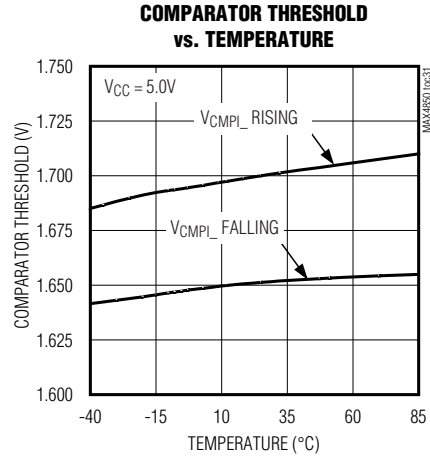
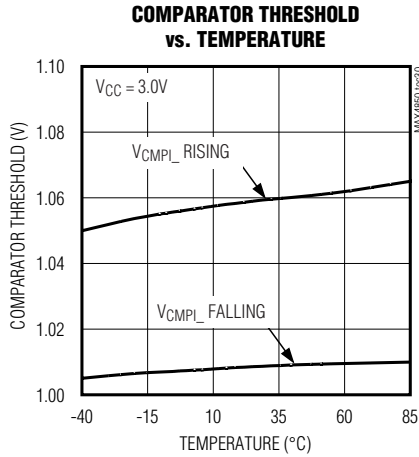
(VCC = 3.0V, TA = +25°C, unless otherwise noted.)



Dual SPDT Analog Switches with Over-Rail Signal Handling

Typical Operating Characteristics (continued)

($V_{CC} = 3.0V$, $T_A = +25^\circ C$, unless otherwise noted.)



MAX4850/MAX4850H/MAX4852/MAX4852H

Dual SPDT Analog Switches with Over-Rail Signal Handling

Pin Descriptions

MAX4850/MAX4850H

| PIN | NAME | FUNCTION |
|------|-----------------|---|
| 1, 8 | N.C. | No Connection. Not internally connected. |
| 2 | CIN1 | Inverting Input for Comparator 1 |
| 3 | CIN2 | Inverting Input for Comparator 2 |
| 4 | COM1 | Common Terminal for Analog Switch 1 |
| 5 | NO1 | Normally Open Terminal for Analog Switch 1 |
| 6 | GND | Ground |
| 7 | NC2 | Normally Closed Terminal for Analog Switch 2 |
| 9 | IN2 | Digital Control Input for Analog Switch 2. A logic LOW on IN2 connects COM2 to NC2 and a logic HIGH connects COM2 to NO2. |
| 10 | COM2 | Common Terminal for Analog Switch 2 |
| 11 | COU1 | Output for Comparator 1 |
| 12 | NO2 | Normally Open Terminal for Analog Switch 2 |
| 13 | COU2 | Output for Comparator 2 |
| 14 | V _{CC} | Supply Voltage. Bypass to GND with a 0.01 μ F capacitor as close to the pin as possible. |
| 15 | IN1 | Digital Control Input for Analog Switch 1. A logic LOW on IN1 connects COM1 to NC1 and a logic HIGH connects COM1 to NO1. |
| 16 | NC1 | Normally Closed Terminal for Analog Switch 1 |
| EP | — | Exposed Paddle. Connect to PC board ground plane. |

MAX4852/MAX4852H

| PIN | NAME | FUNCTION |
|--------------------|-----------------|---|
| 1, 2, 3, 8, 11, 13 | N.C. | No Connection. Not internally connected. |
| 4 | COM1 | Common Terminal for Analog Switch 1 |
| 5 | NO1 | Normally Open Terminal for Analog Switch 1 |
| 6 | GND | Ground |
| 7 | NC2 | Normally Closed Terminal for Analog Switch 2 |
| 9 | IN2 | Digital Control Input for Analog Switch 2. A logic LOW on IN2 connects COM2 to NC2 and a logic HIGH connects COM2 to NO2. |
| 10 | COM2 | Common Terminal for Analog Switch 2 |
| 12 | NO2 | Normally Open Terminal for Analog Switch 2 |
| 14 | V _{CC} | Supply Voltage. Bypass to GND with a 0.01 μ F capacitor as close to the pin as possible. |
| 15 | IN1 | Digital Control Input for Analog Switch 1. A logic LOW on IN1 connects COM1 to NC1 and a logic HIGH connects COM1 to NO1. |
| 16 | NC1 | Normally Closed Terminal for Analog Switch 1 |
| EP | — | Exposed Paddle. Connect to PC board ground plane. |

Dual SPDT Analog Switches with Over-Rail Signal Handling

Detailed Description

The MAX4850/MAX4850H/MAX4852/MAX4852H are low on-resistance, low-voltage, analog switches that operate from a +2V to +5.5V single supply and are fully specified for nominal 3.0V applications. These devices feature over-rail signal capability that allows signals up to 5.5V with supply voltages down to 2.0V. These devices are configured as dual SPDT switches.

These switches have low 50pF on-channel capacitance, which allows for 12Mbps switching of the data signals for USB 2.0 full speed/1.1 applications. The MAX485__ are designed to switch D+ and D- USB signals with a guaranteed skew of less than 1ns (see Figure 1), as measured from 50% of the input signal to 50% of the output signal.

The MAX4850_ features a comparator that can be used for headphone or mute detection. The comparator threshold is internally generated to be approximately 1/3 of V_{CC} .

Applications Information

Digital Control Inputs

The logic inputs (IN_) accept up to +5.5V even if the supply voltages are below this level. For example, with a +3.3V V_{CC} supply, IN_ can be driven low to GND and high to +5.5V, allowing for mixing of logic levels in a system. Driving IN_ rail-to-rail minimizes power con-

sumption. For a +2V supply voltage, the logic thresholds are 0.5V (low) and 1.4V (high); for a +5V supply voltage, the logic thresholds are 0.8V (low) and 1.8V (high).

Analog Signal Levels

The on-resistance of these switches changes very little for analog input signals across the entire supply voltage range (see *Typical Operating Characteristics*). The switches are bidirectional, so NO_, NC_, and COM_ can be either inputs or outputs.

Comparator

The positive terminal of the comparator is internally set to $V_{CC}/3$. When the negative terminal (CIN_) is below the threshold ($V_{CC}/3$), the comparator output (COUT_) goes high. When CIN_ rises above $V_{CC}/3$, COUT_ goes low.

The comparator threshold allows for detection of headphones since headphone audio signals are typically biased to $V_{CC}/2$.

Power-Supply Sequencing

Caution: Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to the device.

Proper power-supply sequencing is recommended for all CMOS devices. Always apply V_{CC} before applying analog signals, especially if the analog signal is not current-limited.

MAX4850/MAX4850H/MAX4852/MAX4852H

Dual SPDT Analog Switches with Over-Rail Signal Handling

MAX4850/MAX4850H/MAX4852/MAX4852H

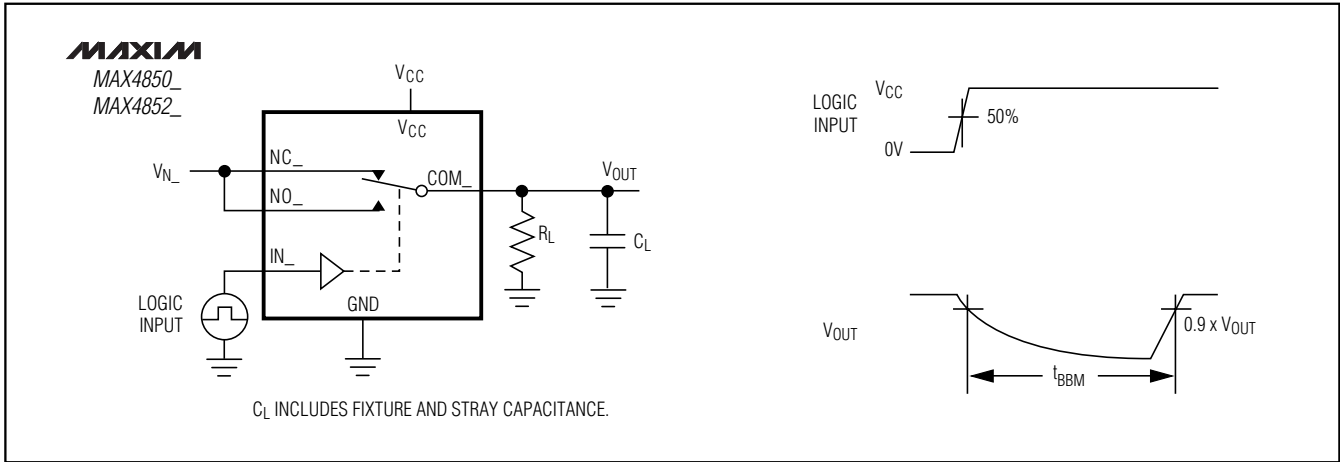


Figure 3. Break-Before-Make Interval

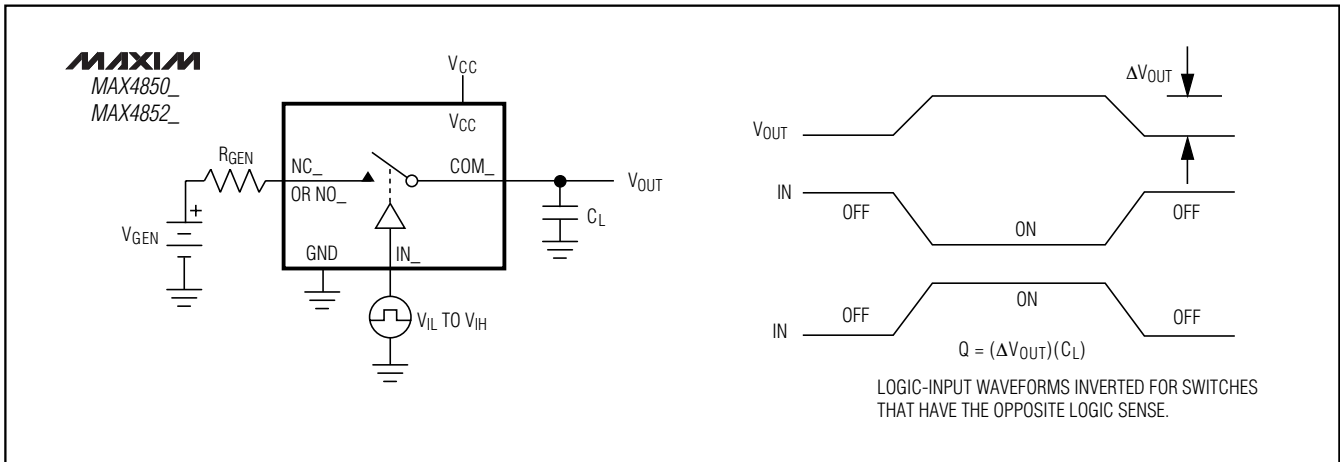


Figure 4. Charge Injection

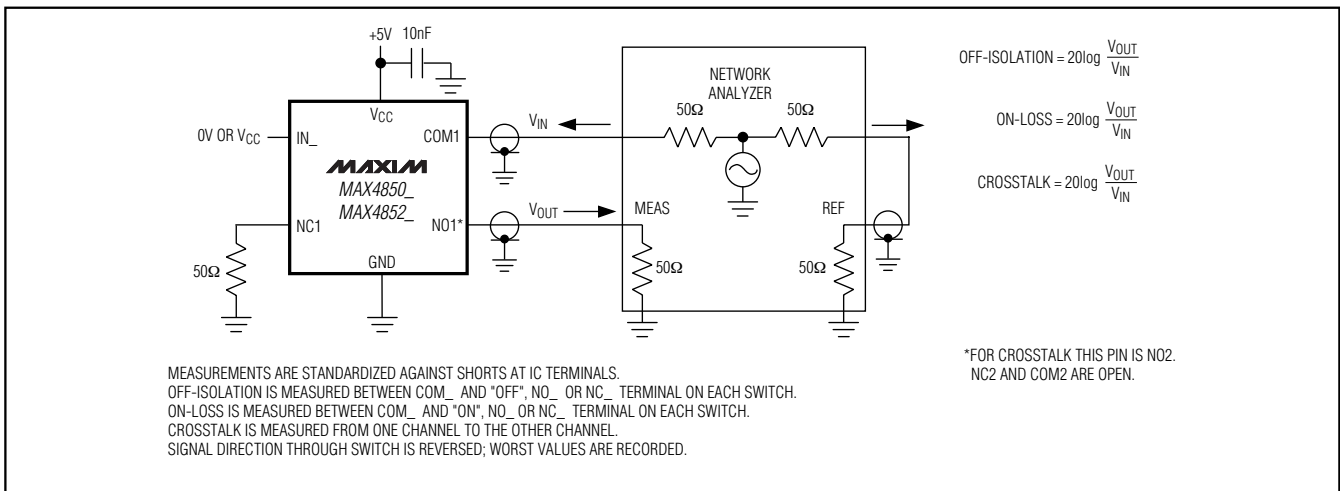


Figure 5. On-Loss, Off-Isolation, and Crosstalk

Dual SPDT Analog Switches with Over-Rail Signal Handling

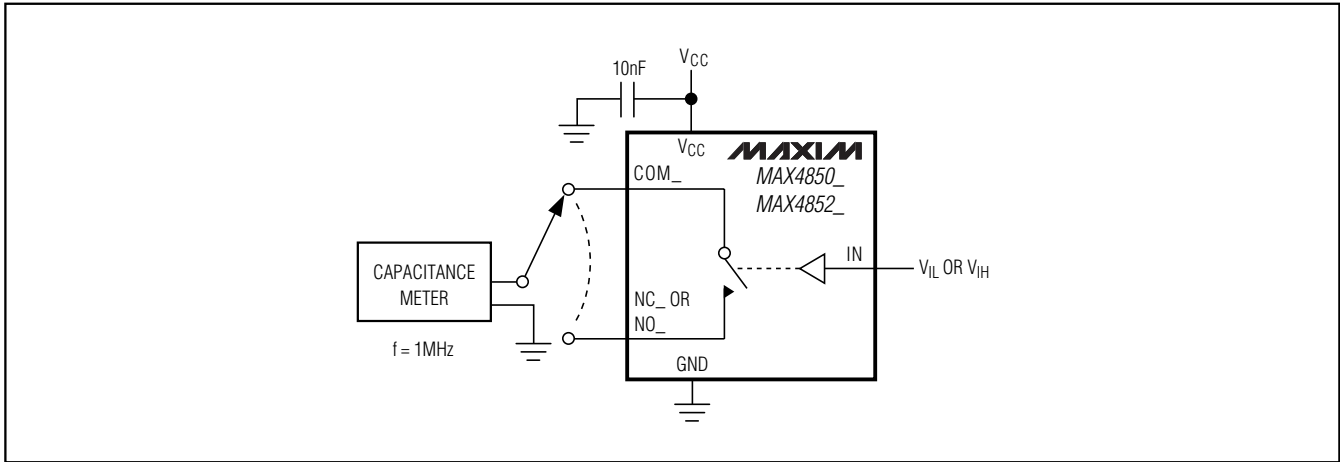


Figure 6. Channel Off-/On-Capacitance

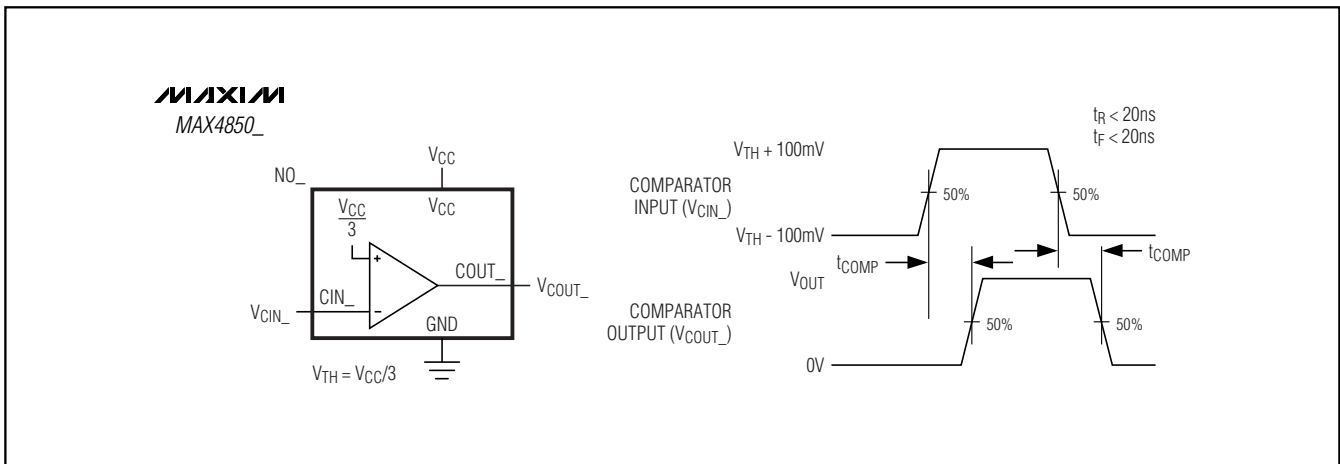
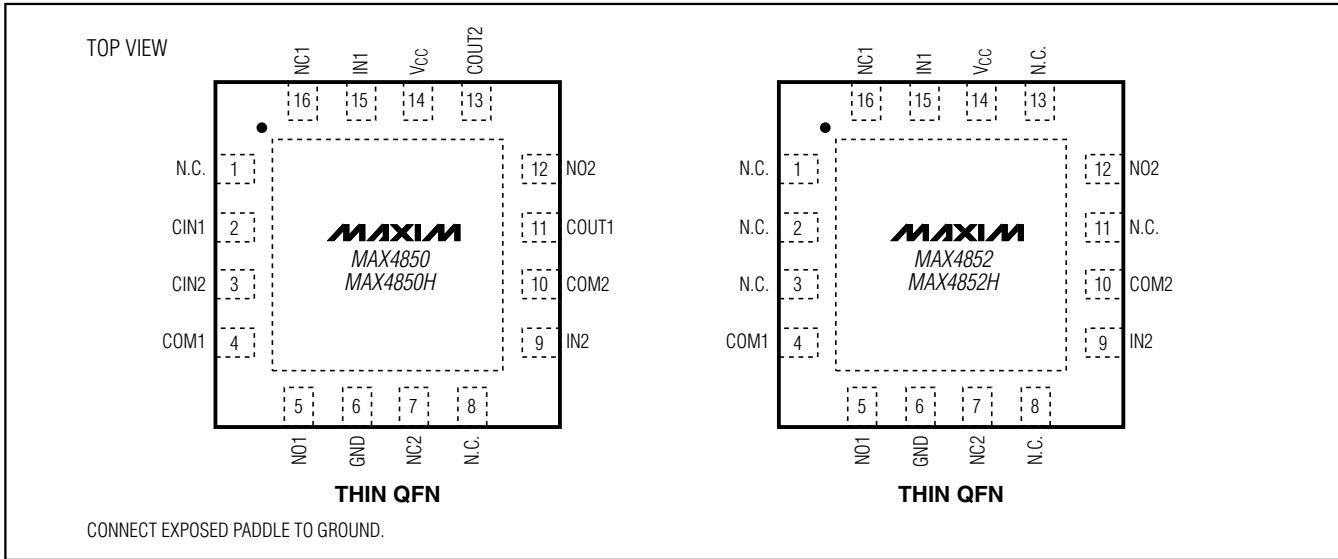


Figure 7. Comparator Switching Time

Dual SPDT Analog Switches with Over-Rail Signal Handling

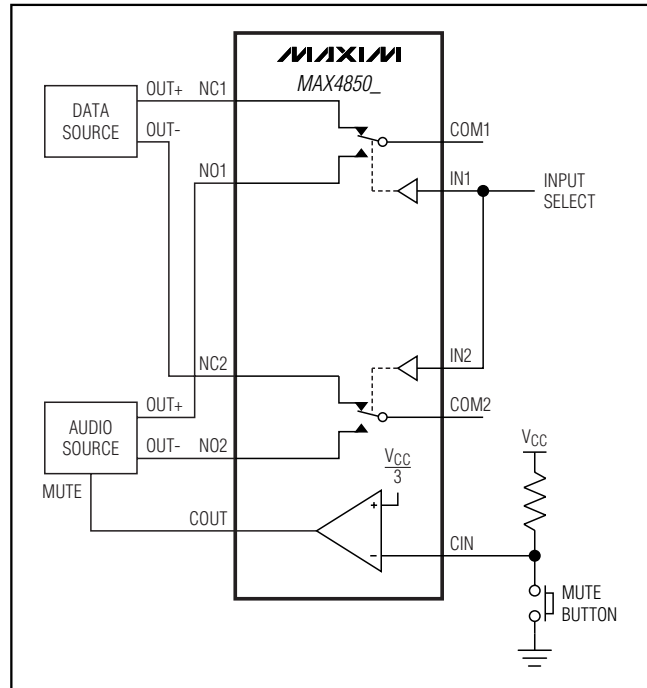
Pin Configurations



Selector Guide

| PART | R _{ON} NC_/NO_ (Ω) | COMPARATORS | OVER-RAIL HANDLING |
|----------|-----------------------------------|-------------|--|
| MAX4850 | 3.5/3.5 | 2 | Input signal passes through the switch |
| MAX4850H | 3.5/3.5 | 2 | High-impedance switch input |
| MAX4852 | 3.5/7 | — | Input signal passes through the switch |
| MAX4852H | 3.5/7 | — | High-impedance switch input |

Typical Operating Circuit



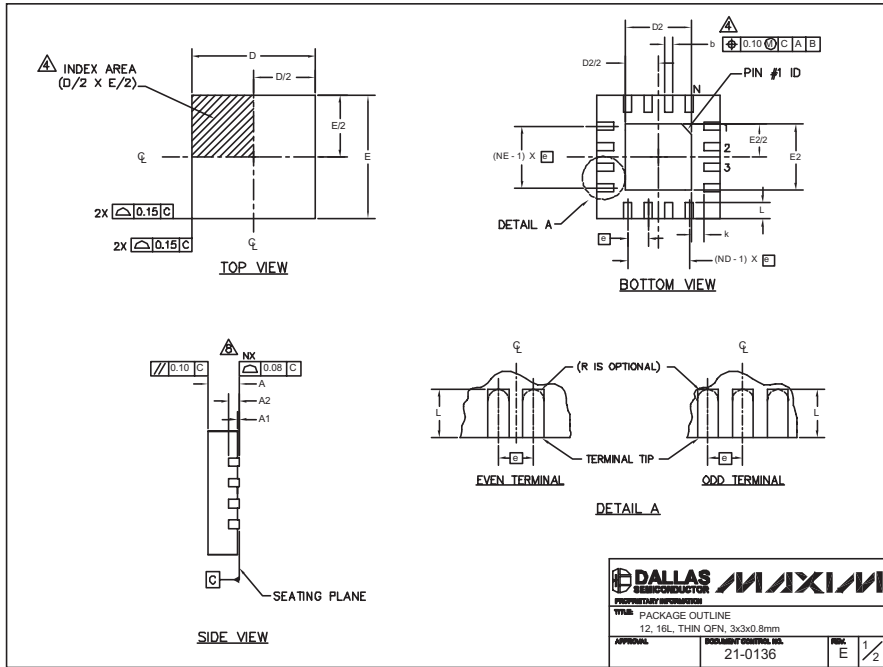
Chip Information

TRANSISTOR COUNT: 735
PROCESS: CMOS

Dual SPDT Analog Switches with Over-Rail Signal Handling

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)



| PKG | 12L 3x3 | | | 16L 3x3 | | |
|------|-----------|------|------|-----------|------|------|
| REF. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 |
| b | 0.20 | 0.25 | 0.30 | 0.20 | 0.25 | 0.30 |
| D | 2.90 | 3.00 | 3.10 | 2.90 | 3.00 | 3.10 |
| E | 2.90 | 3.00 | 3.10 | 2.90 | 3.00 | 3.10 |
| e | 0.50 BSC. | | | 0.50 BSC. | | |
| L | 0.45 | 0.55 | 0.65 | 0.30 | 0.40 | 0.50 |
| N | 12 | | | 16 | | |
| ND | 3 | | | 4 | | |
| NE | 3 | | | 4 | | |
| A1 | 0 | 0.02 | 0.05 | 0 | 0.02 | 0.05 |
| A2 | 0.20 REF | | | 0.20 REF | | |
| k | 0.25 | - | - | 0.25 | - | - |

| PKG CODES | D2 | | | E2 | | | PIN ID | JEDEC | DOWN BONDS ALLOWED |
|-----------|------|------|------|------|------|------|-------------|--------|--------------------|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | | | |
| T1233-1 | 0.95 | 1.10 | 1.25 | 0.95 | 1.10 | 1.25 | 0.35 x 45° | WEED-1 | NO |
| T1233-3 | 0.95 | 1.10 | 1.25 | 0.95 | 1.10 | 1.25 | 0.35 x 45° | WEED-1 | YES |
| T1633-1 | 0.95 | 1.10 | 1.25 | 0.95 | 1.10 | 1.25 | 0.35 x 45° | WEED-2 | NO |
| T1633-2 | 0.95 | 1.10 | 1.25 | 0.95 | 1.10 | 1.25 | 0.35 x 45° | WEED-2 | YES |
| T1633F-3 | 0.85 | 0.80 | 0.85 | 0.85 | 0.80 | 0.85 | 0.225 x 45° | WEED-2 | N/A |
| T1633-4 | 0.95 | 1.10 | 1.25 | 0.95 | 1.10 | 1.25 | 0.35 x 45° | WEED-2 | NO |

NOTES:

- DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
- N IS THE TOTAL NUMBER OF TERMINALS.
- THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
- DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.20 mm AND 0.25 mm FROM TERMINAL TIP.
- ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
- DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
- COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
- DRAWING CONFORMS TO JEDEC MO220 REVISION C.

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