FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-16304-1E

32-bit RISC Microcontroller

CMOS

FR Family MB91F109

MB91F109

■ DESCRIPTION

The MB91F109 is a standard single-chip microcontroller constructed around the 32-bit RISC CPU (FR* family) core with abundant I/O resources and bus control functions optimized for high-performance/high-speed CPU processing for embedded controller applications. To carry out hi-speed performance of CPU instructions, instruction/data Flash memory of 254 Kbytes and RAM of 2 Kbytes + 2 Kbytes are embedded in the MB91F109.

The MB91F109 is optimized for applications requiring high-performance CPU processing such as navigation systems, high-performance FAXs and printer controllers.

*: FR Family stands for FUJITSU RISC controller.

■ FEATURES

FR CPU

- 32-bit RISC, load/store architecture, 5-stage pipeline
- Operating clock frequency: Internal 25 MHz/external 25 MHz (PLL used at source oscillation 12.5 MHz)
- General purpose registers: 32 bits $\times$ 16
- 16-bit fixed length instructions (basic instructions), 1 instruction/1 cycle
- Memory to memory transfer, bit processing, barrel shifter processing: Optimized for embedded applications
- Function entrance/exit instructions, multiple load/store instructions of register contents, instruction systems supporting high level languages
- Register interlock functions, efficient assembly language coding
- Branch instructions with delay slots: Reduced overhead time in branch executions

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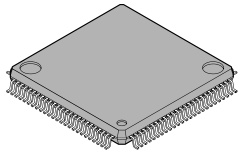
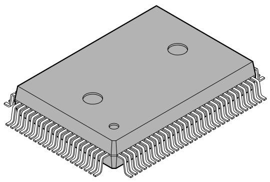
■ PACKAGES

100-pin Plastic LQFP



(FPT-100P-M05)

100-pin Plastic QFP



(FPT-100P-M06)

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- Internal multiplier/supported at instruction level
  Signed 32-bit multiplication: 5 cycles
  Signed 16-bit multiplication: 3 cycles
- Interrupt (push PC and PS): 6 cycles, 16 priority levels

External bus interface

- Without Clock doubler: Maximum internal bus 25 MHz, maximum external bus 25 MHz operation
- 25-bit address bus (32 Mbytes memory space)
- 8/16-bit data bus
- Basic external bus cycle: 2 clock cycles
- Chip select outputs for setting down to a minimum memory block size of 64 Kbytes: 6
- Interface supported for various memory technologies
  DRAM interface (area 4 and 5)
- Automatic wait cycle insertion: Flexible setting, from 0 to 7 for each area
- Unused data/address pins can be configured us input/output ports
- Little endian mode supported (Select 1 area from area 1 to 5)

DRAM interface

- 2 banks independent control (area 4 and 5)
- Normal mode (double CAS DRAM)/high-speed page mode (single CAS DRAM)/Hyper DRAM
- Basic bus cycle: Normally 5 cycles, 2-cycle access possible in high-speed page mode
- Programmable waveform: Automatic 1-cycle wait insertion to RAS and CAS cycles
- DRAM refresh
  CBR refresh (interval time configurable by 6-bit timer)
  Self-refresh mode
- Supports 8/9/10/12-bit column address width
- 2CAS/1WE, 2WE/1CAS selective

DMA controller (DMAC)

- 8 channels
- Transfer incident/external pins/internal resource interrupt requests
- Transfer sequence: Step transfer/block transfer/burst transfer/continuous transfer
- Transfer data length: 8 bits/16 bits/32 bits selective
- NMI/interrupt request enables temporary stop operation

UART

- 3 independent channels
- Full-duplex double buffer
- Data length: 7 bits to 9 bits (non-parity), 6 bits to 8 bits (parity)
- Asynchronous (start-stop system), CLK-synchronized communication selective
- Multi-processor mode
- Internal 16-bit timer (U-TIMER) operating as a proprietary baud rate generator: Generates any given baud rate
- Use external clock can be used as a transfer clock
- Error detection: Parity, frame, overrun

10-bit A/D converter (successive approximation conversion type)

- 10-bit resolution, 4 channels
- Successive approximation type: Conversion time of 5.6 µs at 25 MHz
- Internal sample and hold circuit
- Conversion mode: Single conversion/scanning conversion/repeated conversion/stop conversion selective
- Start: Software/external trigger/internal timer selective

(Continued)

16-bit reload timer

- 3 channels
- Internal clock: 2 clock cycle resolution, divide by 2/8/32 selective

Other interval timers

- 16-bit timer: 3 channels (U-TIMER)
- PWM timer: 4 channels
- Watchdog timer: 1 channel

Bit search module

First bit transition “1” or “0” from MSB can be detected in 1 cycle

Interrupt controller

- External interrupt input: Non-maskable interrupt ($\overline{\text{NMI}}$), normal interrupt $\times$ 4 (INT0 to INT3)
- Internal interrupt incident:UART, DMA controller (DMAC), 10-bit A/D converter, 16-bit reload-timer, PWM timer, U-TIMER and delayed interrupt module
- Priority levels of interrupts are programmable except for non-maskable interrupt (in 16 steps)

Others

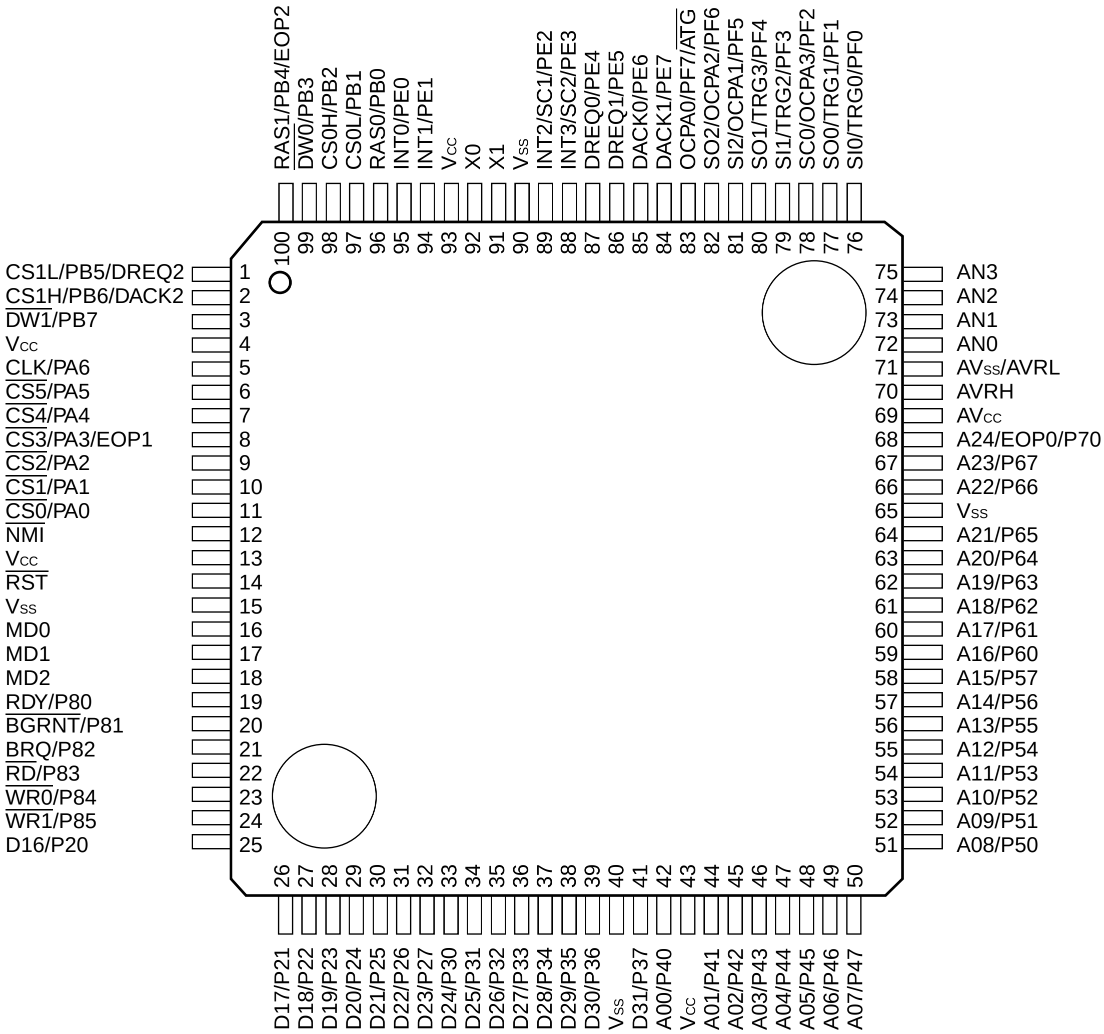
- Reset cause: Power-on reset/software reset/external reset
- Low-power consumption mode: Sleep mode/stop mode
- Clock control
  Gear function: Operating clocks for CPU and peripherals are independently selective
  Gear clock can be selected from 1/1, 1/2, 1/4 and 1/8 (or 1/2, 1/4, 1/8 and 1/16)
  (However, operating frequency for peripherals is less than 25 MHz.)
- Packages: LQFP-100 and QFP-100
- CMOS technology (0.5 µm)
- Power supply voltage: 3.15 V ~ 3.6 V

■ PRODUCT LINEUP

Parameter \ Part number	MB91F109
Classification	Mass production products Flash (mask ROM products)
Flash size	254 Kbytes
IRAM size	—
CROM size	—
CRAM size	2 Kbytes
RAM size	2 Kbytes
I $	—
Other	Under trial manufacture

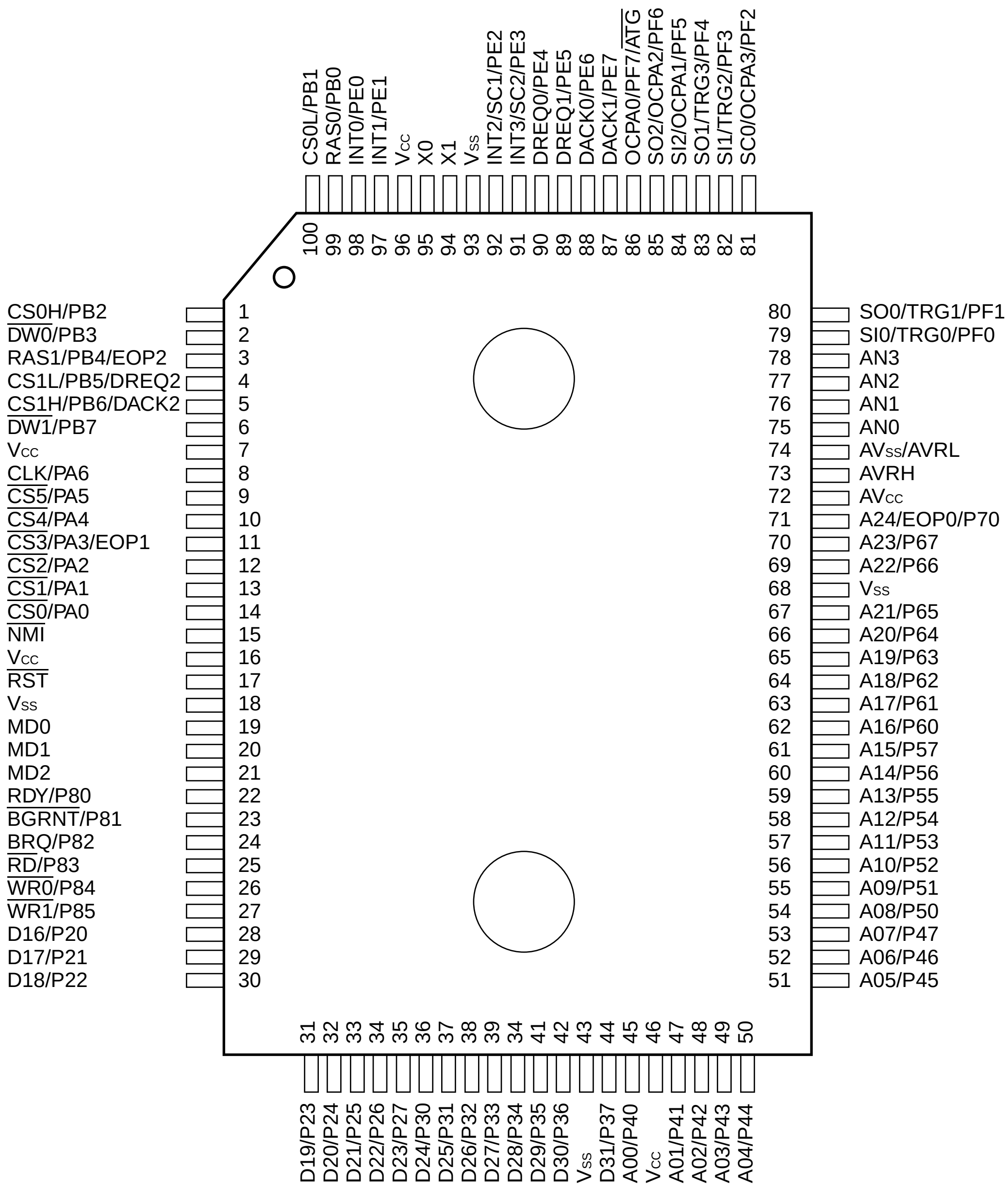
■ PIN ASSIGNMENT

(Top view)



(FPT-100P-M05)

(Top view)



(FPT-100P-M06)

■ PIN DESCRIPTION

Pin no.		Pin name	Circuit type	Function
LQFP*1	QFP*2			
25 to 32	28 to 35	D16 to D23	C	Bit 16 to bit 23 of external data bus
		P20 to P27		Can be configured as general purpose I/O port when external data bus width is set to 8-bit or in single chip mode.
33 to 39, 41	36 to 42, 44	D24 to D30, D31	C	Bit 24 to bit 31 of external data bus
		P30 to P36, P37		Can be configured as general purpose I/O ports when not used as address bus.
42, 44 to 50, 51 to 58	45, 47 to 53, 54 to 61	A00, A01 to A07, A08 to A15	E	Bit 00 to bit 15 of external address bus
		P40, P41 to P47, P50 to P57		Can be configured as general purpose I/O ports when not used as address bus.
59 to 64, 66, 67	62 to 67, 69, 70	A16 to A21, A22, A23	E	Bit 16 to bit 23 of external address bus
		P60 to P65, P66, P67		Can be configured as general purpose I/O ports when not used as address bus.
68	71	A24	E	Bit 24 of external address bus
		EOP0		Can be configured as DMAC EOP output (ch. 0) when DMAC EOP output is enabled.
		P70		Can be configured as general purpose I/O port when A24 and EOP0 are not used.
19	22	RDY	C	External ready input Inputs “0” when bus cycle is being executed and not completed.
		P80		Can be configured as general purpose I/O port when RDY is not used.
20	23	$\overline{\text{BGRNT}}$	E	External bus release acknowledge output Outputs “L” level when external bus is released.
		P81		Can be configured as general purpose I/O port when $\overline{\text{BGRNT}}$ is not used.
21	24	BRQ	C	External bus release request input Inputs “1” when release of external bus is required.
		P82		Can be configured as general purpose I/O port when BRQ is not used.
22	25	$\overline{\text{RD}}$	E	Read strobe output pin for external bus
		P83		Can be configured as general purpose I/O port when $\overline{\text{RD}}$ is not used.

*1: FPT-100P-M05
*2: FPT-100P-M06

(Continued)

<table>
<tr><th colspan="2">Pin no.</th><th rowspan="2">Pin name</th><th rowspan="2">Circuit type</th><th rowspan="2">Function</th></tr>
<tr><th>LQFP*1</th><th>QFP*2</th></tr>
<tr><td rowspan="2">23</td><td rowspan="2">26</td><td>P84</td><td rowspan="2">E</td><td>Can be configured as general purpose I/O port when $\overline{\text{WR0}}$ is not used.</td></tr>
<tr><td>$\overline{\text{WR0}}$</td><td rowspan="3">Write strobe output pin for external bus
Relation between control signals and effective byte locations is as follows:
<table><tr><th></th><th>16-bit bus width</th><th>8-bit bus width</th><th>Single chip mode</th></tr><tr><td>D31 to D24</td><td>$\overline{\text{WR0}}$</td><td>$\overline{\text{WR0}}$</td><td>(I/O port enabled)</td></tr><tr><td>D23 to D16</td><td>$\overline{\text{WR1}}$</td><td>(I/O port enabled)</td><td>(I/O port enabled)</td></tr></table>
Note : $\overline{\text{WR1}}$ is Hi-Z during resetting.
Attach an external pull-up resister when using at 16-bit bus width.</td></tr>
<tr><td rowspan="2">24</td><td rowspan="2">27</td><td>$\overline{\text{WR1}}$</td><td rowspan="2">E</td></tr>
<tr><td>P85</td></tr>
<tr><td></td><td></td><td></td><td></td><td>Can be configured as general purpose I/O port when $\overline{\text{WR1}}$ is not used.</td></tr>
<tr><td rowspan="2">11</td><td rowspan="2">14</td><td>$\overline{\text{CS0}}$</td><td rowspan="2">E</td><td>Chip select 0 output (“L” active)</td></tr>
<tr><td>PA0</td><td>Can be configured as general purpose I/O port when $\overline{\text{CS0}}$ is not used.</td></tr>
<tr><td rowspan="2">10</td><td rowspan="2">13</td><td>$\overline{\text{CS1}}$</td><td rowspan="2">E</td><td>Chip select 1 output (“L” active)</td></tr>
<tr><td>PA1</td><td>Can be configured as general purpose I/O port when $\overline{\text{CS1}}$ is not used.</td></tr>
<tr><td rowspan="2">9</td><td rowspan="2">12</td><td>$\overline{\text{CS2}}$</td><td rowspan="2">E</td><td>Chip select 2 output (“L” active)</td></tr>
<tr><td>PA2</td><td>Can be configured as a port when $\overline{\text{CS2}}$ is not used.</td></tr>
<tr><td rowspan="3">8</td><td rowspan="3">11</td><td>$\overline{\text{CS3}}$</td><td rowspan="3">E</td><td>Chip select 3 output (“L” active)</td></tr>
<tr><td>PA3</td><td>Can be configured as a port when $\overline{\text{CS3}}$ and EOP1 are not used.</td></tr>
<tr><td>EOP1</td><td>EOP output pin for DMAC (ch. 1)
This function is available when EOP output for DMAC is enabled.</td></tr>
<tr><td rowspan="2">7</td><td rowspan="2">10</td><td>$\overline{\text{CS4}}$</td><td rowspan="2">E</td><td>Chip select 4 output (“L” active)</td></tr>
<tr><td>PA4</td><td>Can be configured as general purpose I/O port when $\overline{\text{CS4}}$ is not used.</td></tr>
<tr><td rowspan="2">6</td><td rowspan="2">9</td><td>$\overline{\text{CS5}}$</td><td rowspan="2">E</td><td>Chip select 5 output (“L” active)</td></tr>
<tr><td>PA5</td><td>Can be configured as general purpose I/O port when $\overline{\text{CS5}}$ is not used.</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">8</td><td>CLK</td><td rowspan="2">E</td><td>System clock output
Outputs clock signal of external bus operating frequency.</td></tr>
<tr><td>PA6</td><td>Can be configured as general purpose I/O port when CLK is not used.</td></tr>
</table>

*1: FPT-100P-M05
*2: FPT-100P-M06

(Continued)

Pin no.		Pin name	Circuit type	Function
LQFP*1	QFP*2			
96	99	RAS0	E	RAS output for DRAM bank 0
		PB0		Can be configured as general purpose I/O port when RAS0 is not used.
97	100	CS0L	E	CASL output for DRAM bank 0
		PB1		Can be configured as general purpose I/O port when CS0L is not used.
98	1	CS0H	E	CASH output for DRAM bank 0
		PB2		Can be configured as general purpose I/O port when CS0H is not used.
99	2	$\overline{\text{DW0}}$	E	$\overline{\text{WE}}$ output for DRAM bank 0 (“L” active)
		PB3		Can be configured as general purpose I/O port when $\overline{\text{DW0}}$ is not used.
100	3	RAS1	E	RAS output for DRAM bank 1
		PB4		Can be configured as general purpose I/O port when RAS1 and EOP2 are not used.
		EOP2		DMAC EOP output (ch. 2) This function is available when DMAC EOP output is enabled.
1	4	CS1L	E	CASL output for DRAM bank 1
		PB5		Can be configured as general purpose I/O port when CS1L and DREQ are not used.
		DREQ2		External transfer request input pin for DMA This pin is used for input when external trigger is selected to cause DMAC operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
2	5	CS1H	E	CASH output for DRAM bank 1
		PB6		Can be configured as general purpose I/O port when CS1H and DACK2 are not used.
		DACK2		External transfer request accept output pin for DMAC (ch. 2) This function is available when transfer request output for DMAC is enabled.
3	6	$\overline{\text{DW1}}$	E	$\overline{\text{WE}}$ output for DRAM bank 1 (“L” active)
		PB7		Can be configured as general purpose I/O port when $\overline{\text{DW1}}$ is not used.
16 to 18	19 to 21	MD0 to MD2	F	Mode pins 0 to 2 MCU basic operation mode is set by these pins. Directly connect these pins with V_{CC} or V_{SS} for use.
92	95	X0	A	Clock (oscillator) input
91	94	X1	A	Clock (oscillator) output
14	17	$\overline{\text{RST}}$	B	External reset input
12	15	$\overline{\text{NMI}}$	G	NMI (non-maskable interrupt pin) input (“L” active)

*1: FPT-100P-M05
*2: FPT-100P-M06

(Continued)

Pin no.		Pin name	Circuit type	Function
LQFP*1	QFP*2			
95, 94	98, 97	INT0, INT1	E	External interrupt request input pins These pins are used for input during corresponding interrupt is enabled, and it is necessary to disable output for other functions from these pins unless such output is made intentionally.
		PE0, PE1		Can be configured as general purpose I/O ports when INT0 and INT1 are not used.
89	92	INT2	E	External interrupt request input pin This pin is used for input during corresponding interrupt is enabled, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
		SC1		Clock I/O pin for UART1 Clock output is available when clock output of UART1 is enabled.
		PE2		Can be configured as general purpose I/O port when INT2 and SC1 are not used. This function is available when UART1 clock output is disabled.
88	91	INT3	E	External interrupt request input pin This pin is used for input during corresponding interrupt is enabled, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
		SC2		UART2 clock I/O pin Clock output is available when UART2 clock output is enabled.
		PE3		Can be configured as general purpose I/O port when INT3 and SC2 are not used. This function is available when UART2 clock output is disabled.
87, 86	90, 89	DREQ0, DREQ1	E	External transfer request input pins for DMA These pins are used for input when external trigger is selected to cause DMAC operation, and it is necessary to disable output for other functions from these pins unless such output is made intentionally.
		PE4, PE5		Can be configured as general purpose I/O ports when DREQ0 and DREQ1 are not used.
85	88	DACK0	E	External transfer request acknowledge output pin for DMAC (ch. 0) This function is available when transfer request output for DMAC is enabled.
		PE6		Can be configured as general purpose I/O port when DACK0 is not used. This function is available when transfer request acknowledge output for DMAC or DACK0 output is disabled.

*1: FPT-100P-M05
*2: FPT-100P-M06

(Continued)

Pin no.		Pin name	Circuit type	Function
LQFP*1	QFP*2			
84	87	DACK1	E	External transfer request acknowledge output pin for DMAC (ch. 1) This function is available when transfer request output for DMAC is enabled.
		PE7		Can be configured as general purpose I/O port when DACK1 is not used. This function is available when transfer request output for DMAC or DACK1 output is disabled.
76	79	SI0	E	UART0 data input pin This pin is used for input during UART0 is in input operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
		TRG0		PWM timer external trigger input pin (ch.0) This pin is used for input during PWM timer external trigger is in input operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
		PF0		Can be configured as general purpose I/O port when SI0 and TRG0 are not used.
77	80	SO0	E	UART0 data output pin This function is available when UART0 data output is enabled.
		TRG1		PWM timer external trigger input pin This function is available when serial data output of PF1, UART0 are disabled.
		PF1		Can be configured as general purpose I/O port when SO0 and TRG1 are not used. This function is available when serial data output of UART0 is disabled.
78	81	SC0	E	UART0 clock I/O pin Clock output is available when UART0 clock output is enabled.
		OCPA3		PWM timer output pin This function is available when PWM timer output is enabled.
		PF2		Can be configured as general purpose I/O port when SC0 and OCPA3 are not used. This function is available when UART0 clock output is disabled.
79	82	SI1	E	UART1 data input pin This pin is used for input during UART1 is in input operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
		TRG2		PWM timer external trigger input pin This pin is used for input during PWM timer external trigger is in input operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
		PF3		Can be configured as general purpose I/O port when SI1 and TRG2 are not used.

*1: FPT-100P-M05
*2: FPT-100P-M06

(Continued)

Pin no.		Pin name	Circuit type	Function
LQFP*1	QFP*2			
80	83	SO1	E	UART1 data output pin This function is available when UART1 data output is enabled.
		TRG3		PWM timer external trigger input pin This function is available when PF4, UART1 data outputs are disabled.
		PF4		Can be configured as general purpose I/O port when SO1 and TRG3 are not used. This function is available when UART1 data output is disabled.
81	84	SI2	E	UART2 data input pin This pin is used for input during UART2 is in input operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
		OCPA1		PWM timer output pin This function is available when PWM timer output is enabled.
		PF5		Can be configured as general purpose I/O port when SI2 and OCPA2 are not used.
82	85	SO2	E	UART2 data output pin This function is available when UART2 data output is enabled.
		OCPA2		PWM timer output pin This function is available when PWM timer output is enabled.
		PF6		Can be configured as general purpose I/O port when SO2 and OCPA2 are not used. This function is available when UART2 data output is disabled.
83	86	OCPA0	E	PWM timer output pin This function is available when PWM timer output is enabled.
		PF7		Can be configured as a port when OCPA0 and $\overline{\text{ATG}}$ are not used. This function is available when PWM timer output is disabled.
		$\overline{\text{ATG}}$		External trigger input pin for A/D converter This pin is used for input when external trigger is selected to cause A/D converter operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
72 to 75	75 to 78	AN0 to AN3	D	Analog input pins of A/D converter
69	72	AVcc	—	Power supply pin (Vcc) for A/D converter
70	73	AVRH	—	Reference voltage input (high) for A/D converter Make sure to turn on and off this pin with potential of AVRH or more applied to Vcc.
71	74	AVss, AVRL	—	Power supply pin (Vss) for A/D converter and reference voltage input pin (low)

*1: FPT-100P-M05
*2: FPT-100P-M06

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Pin no.		Pin name	Circuit type	Function
LQFP*1	QFP*2			
4, 13, 43, 93	7, 16, 46, 96	V_{CC}	—	Power supply pin (V_{CC}) for digital circuit Always power supply pin (V_{CC}) must be connected to the power supply
15, 40, 65, 90	18, 43, 68, 93	V_{SS}	—	Earth level (V_{SS}) for digital circuit

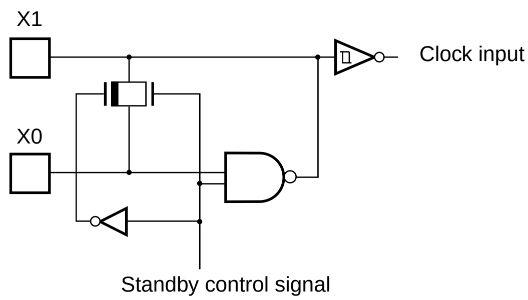
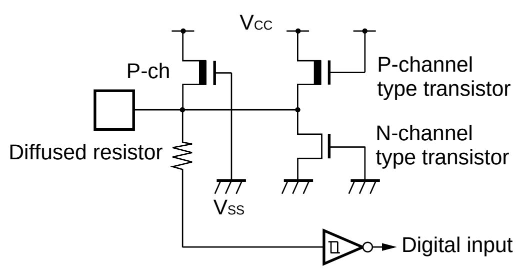
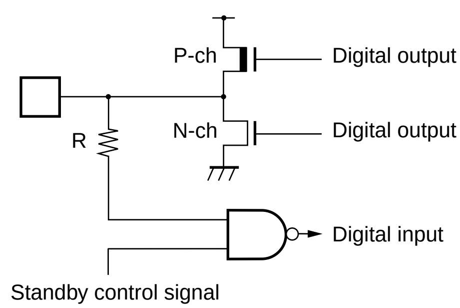
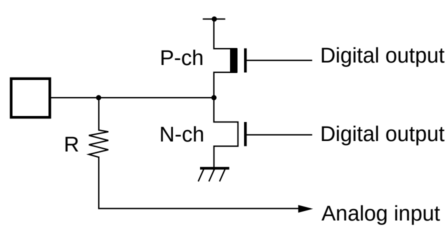
*1: FPT-100P-M05
*2: FPT-100P-M06

Note : In most of the above pins, I/O port and resource I/O are multiplexed e.g. xxx/Pxxx. In case of conflict between output of I/O port and resource I/O, priority is always given to the output of resource I/O.

■ DRAM CONTROL PIN

Pin name	Data bus 16-bit mode		Data bus 8-bit mode	Remarks
	2CAS/1WR mode	1CAS/2WR mode		
RAS0	Area 4 RAS	Area 4 RAS	Area 4 RAS	Correspondence of “L” “H” to lower address 1 bit (A0) in data bus 16-bit mode “L”: “0” “H”: “1” CASL: CAS which A0 corresponds to “0” area CASH: CAS which A0 corresponds to “1” area $\overline{\text{WEL}}$: $\overline{\text{WE}}$ which A0 corresponds to “0” area $\overline{\text{WEH}}$: $\overline{\text{WE}}$ which A0 corresponds to “1” area
RAS1	Area 5 RAS	Area 5 RAS	Area 5 RAS	
CS0L	Area 4 CASL	Area 4 CAS	Area 4 CAS	
CS0H	Area 4 CASH	Area 4 $\overline{\text{WEL}}$	Area 4 CAS	
CS1L	Area 5 CASL	Area 5 CAS	Area 5 CAS	
CS1H	Area 5 CASH	Area 5 $\overline{\text{WEL}}$	Area 5 CAS	
$\overline{\text{DW0}}$	Area 4 $\overline{\text{WE}}$	Area 4 $\overline{\text{WEH}}$	Area 4 $\overline{\text{WE}}$	
$\overline{\text{DW1}}$	Area 5 $\overline{\text{WE}}$	Area 5 $\overline{\text{WEH}}$	Area 5 $\overline{\text{WE}}$	

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• Oscillation feedback resistance 1 MΩ approx. With standby control
B		• CMOS level hysteresis input Without standby control With pull-up resistance
C		• CMOS level I/O With standby control
D		• Analog input

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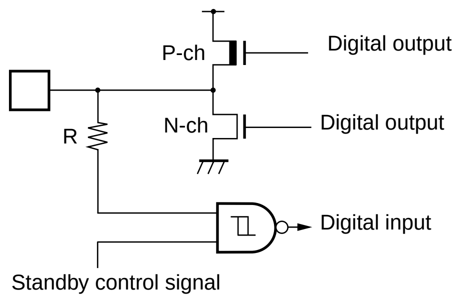
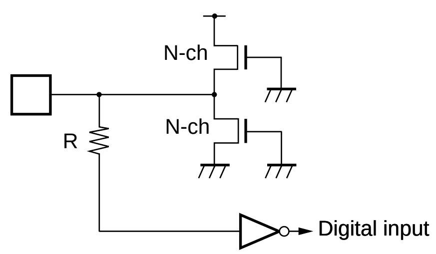
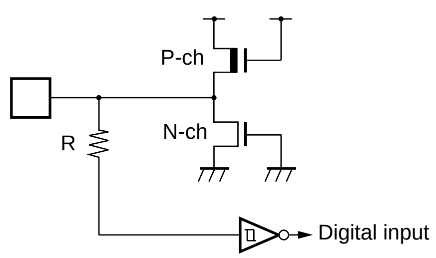
Type	Circuit	Remarks
E		• CMOS level output • CMOS level hysteresis input With standby control
F		• CMOS level input Without standby control
G		• CMOS level hysteresis input Without standby control

■ HANDLING DEVICES

1. Preventing Latchup

In CMOS ICs, applying voltage higher than V_{CC} or lower than V_{SS} to input/output pin or applying voltage over rating across V_{CC} and V_{SS} may cause latchup.

This phenomenon rapidly increases the power supply current, which may result in thermal breakdown of the device. Make sure to prevent the voltage from exceeding the maximum rating.

Take care that the analog power supply (AV_{CC}, AVRH) and the analog input do not exceed the digital power supply (V_{CC}) when the analog power supply turned on or off.

2. Treatment of Unused Pins

Unused pins left open may cause malfunctions. Make sure to connect them to pull-up or pull-down resistors.

3. External Reset Input

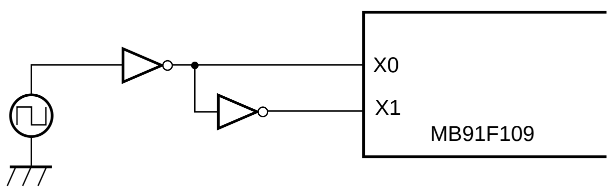
It takes at least 5 machine cycle to input “L” level to the $\overline{\text{RST}}$ pin and to ensure inner reset operation properly.

4. Remarks for External Clock Operation

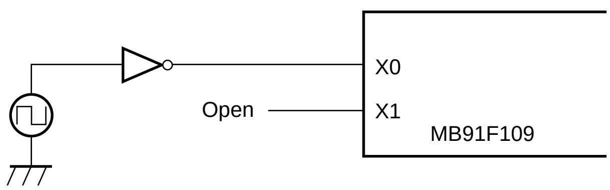
When external clock is selected, supply it to X0 pin generally, and simultaneously the opposite phase clock to X0 must be supplied to X1 pin. However, in this case the stop mode must not be used (because X1 pin stops at “H” output in stop mode).

And can be used to supply only to X0 pin with 5 V power supply at 12.5 MHz and less than.

- **Using an external clock**



Using an external clock (normal)
Note: Can not be used stop mode (oscillation stop mode).



Using an external clock (can be used at 12.5 MHz and less than.)
(3.3 V power supply only)

5. Power Supply Pins

When there are several V_{CC} and V_{SS} pins, each of them is equipotentially connected to its counterpart inside of the device, minimizing the risk of malfunctions such as latch up. To further reduce the risk of malfunctions, to prevent EMI radiation, to prevent strobe signal malfunction resulting from creeping-up of ground level and to observe the total output current standard, connect all V_{CC} and V_{SS} pins to the power supply or GND.

It is preferred to connect V_{CC} and V_{SS} of MB91F109 to power supply with minimal impedance possible.

It is also recommended to connect a ceramic capacitor as a bypass capacitor of about 0.1 µF between V_{CC} and V_{SS} at a position as close as possible to MB91F109.

6. Crystal Oscillator Circuit

Noises around X0 and X1 pins may cause malfunctions of MB91F109. In designing the PC board, layout X0, X1 and crystal oscillator (or ceramic oscillator) and bypass capacitor for grounding as close as possible.

It is strongly recommended to design PC board so that X1 and X0 pins are surrounded by grounding area for stable operation.

7. Turning-on Sequence of A/D Converter Power Supply and Analog Input

Make sure to turn on the digital power supply (V_{CC}) before turning on the A/D converter (AV_{CC}, AVRH) and applying voltage to analog input (AN0 to AN3).

Make sure to turn off digital power supply after power supply to A/D converters and analog inputs have been switched off. (There are no such limitations in turning on power supplies. Analog and digital power supplies may be turned on simultaneously.) Make sure that AVRH never exceeds AV_{CC} when turning on/off power supplies.

8. Treatment of N.C. Pins

Make sure to leave N.C. pins open.

9. Fluctuation of Power Supply Voltage

Warranty range for normal operation against fluctuation of power supply voltage V_{CC} is as given in rating. However, sudden fluctuation of power supply voltage within the warranty range may cause malfunctions. It is recommended to make every effort to stabilize the power supply voltage to IC. It is also recommended that by controlling power supply as a reference of stabilizing, V_{CC} ripple fluctuation (P-P value) at the commercial frequency (50 Hz to 60 Hz) should be less than 10% of the standard V_{CC} value and the transient regulation should be less than 0.1 V/ms at instantaneous deviation like turning off the power supply.

10. Mode Setting Pins (MD0 to MD2)

Connect mode setting pins (MD0 to MD2) directly to V_{CC} or V_{SS}.

Arrange each mode setting pin and V_{CC} or V_{SS} patterns on the printed circuit board as close as possible and make the impedance between them minimal to prevent mistaken entrance to the test mode caused by noises.

11. Turning on the Power Supply

When turning on the power supply, never fail to start from setting the $\overline{RST}$ pin to “L” level. And after the power supply voltage goes to V_{CC} level, at least after ensuring the time for 5 machine cycle, then set to “H” level.

12. Pin Condition at Turning on the Power Supply

The pin condition at turning on the power supply is unstable. The circuit starts being initialized after turning on the power supply and then starting oscillation and then the operation of the internal regulator becomes stable. So it takes about 42 ms for the pin to be initialized from the oscillation starting at the source oscillation 12.5 MHz. Take care that the pin condition may be output condition at initial unstable condition.

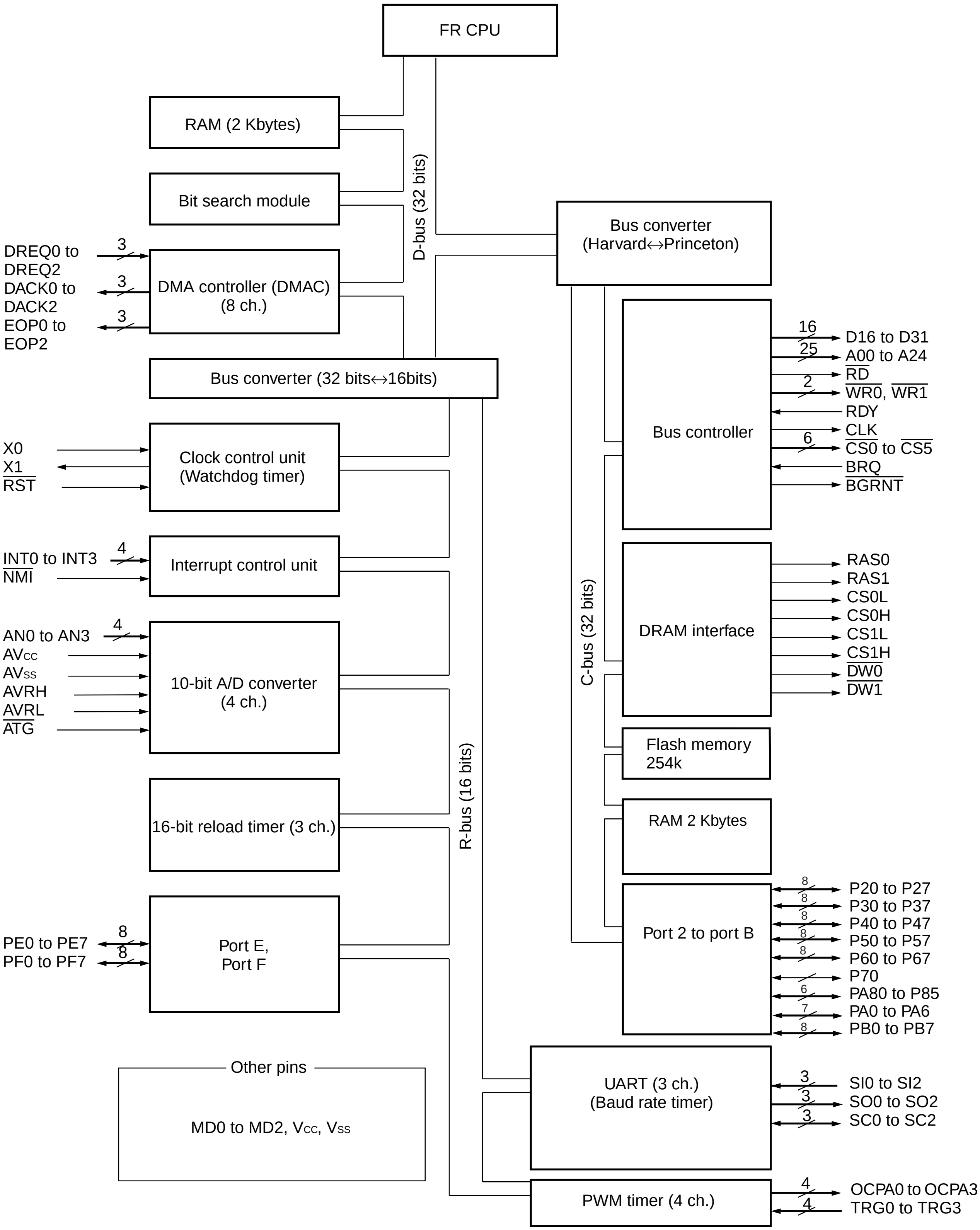
13. Source Oscillation Input at Turning on the Power Supply

At turning on the power supply, never fail to input the clock before cancellation of the oscillation stabilizing waiting.

14. Initialization

Some internal resistors initialized only via power on reset are embedded in the device. To initialize these resistors, run power on reset by returning on the power supply or to set $\overline{\text{RST}}$ pin to “H” level.

■ BLOCK DIAGRAM



Note : Pins are display for functions (Actually some pins are multiplexer).
When using REALOS, time control should be done by using external interrupt or inner timer.

■ CPU CORE

1. Memory Space

The FR family has a logical address space of 4 Gbytes (2^{32} bytes) and the CPU linearly accesses the memory space.

• **Memory space**

• Memory Space

Address	Single chip mode	Internal ROM/ external bus mode	External ROM/ external bus mode		
0000 0000$_H$	I/O Area	I/O Area	I/O Area	Direct addressing area*	See “■I/O MAP”
0000 0400$_H$	I/O Area	I/O Area	I/O Area		
0000 0800$_H$	Access inhibited	Access inhibited	Access inhibited		
0000 1000$_H$	RAM 2 Kbytes	RAM 2 Kbytes	RAM 2 Kbytes		
0000 1800$_H$	Access inhibited	Access inhibited	Access inhibited		
0001 0000$_H$	Access inhibited	External area	External area		
0008 0000$_H$	Access inhibited	Access inhibited			
000C 0000$_H$	RAM 2 Kbytes	RAM 2 Kbytes			
000C 0800$_H$	FLASH ROM 254 Kbytes	FLASH ROM 254 Kbytes			
0010 0000$_H$	Access inhibited	External area			
FFFF FFFF$_H$					

***: Direct addressing area**

The following areas on the memory space are assigned to direct addressing area for I/O. In these areas, an address can be specified in a direct operand of a code.

Direct areas consists of the following areas dependent on accessible data sizes.
Byte data access: 000$_H$ to 0FF$_H$
Half word data access: 000$_H$ to 1FF$_H$
Word data access: 000$_H$ to 3FF$_H$

Notes: Access to the external area can be execute in the single chip mode.
To access to the external area, select internal ROM external bus mode via mode resistor.
Never execute data access to the instruction ROM area.

2. Registers

The FR family has two types of registers; dedicated registers embedded on the CPU and general-purpose registers on memory.

- **Dedicated registers**

Program counter (PC): 32-bit length, indicates the location of the instruction to be executed.
Program status (PS): 32-bit length, register for storing register pointer or condition codes
Table base register (TBR): Holds top address of vector table used in EIT (Exceptional/Interrupt/Trap) processing.
Return pointer (RP): Holds address to resume operation after returning from a subroutine.
System stack pointer (SSP): Indicates system stack space.
User's stack pointer (USP): Indicates user's stack space.
Multiplication/division result register (MDH/MDL): 32-bit length, register for multiplication/division

32 bits		Initial value	
PC	Program counter	XXXX XXXXH	Indeterminate
PS	Program status		
TBR	Table base register	000F FC00H	
RP	Return pointer	XXXX XXXXH	Indeterminate
SSP	System stack pointer	0000 0000H	
USP	User's stack pointer	XXXX XXXXH	Indeterminate
MDH	Multiplication/division result register	XXXX XXXXH	Indeterminate
MDL		XXXX XXXXH	Indeterminate

- **Program status (PS)**

The PS register is for holding program status and consists of a condition code register (CCR), a system condition code register (SCR) and a interrupt level mask register (ILM).

	31	20	19	18	17	16		10	9	8	7	6	5	4	3	2	1	0
PS	—	ILM4	ILM3	ILM2	ILM1	ILM0	—	D1	D0	T	—	—	S	I	N	Z	V	C
		ILM						SCR			CCR							

- **Condition code register (CCR)**

S-flag: Specifies a stack pointer used as R15.
I-flag: Controls user interrupt request enable/disable.
N-flag: Indicates sign bit when division result is assumed to be in the 2's complement format.
Z-flag: Indicates whether or not the result of division was "0".
V-flag: Assumes the operand used in calculation in the 2's complement format and indicates whether or not overflow has occurred.
C-flag: Indicates if a carry or borrow from the MSB has occurred.

- **System condition code register (SCR)**

T-flag: Specifies whether or not to enable step trace trap.

- **Interrupt level mask register (ILM)**

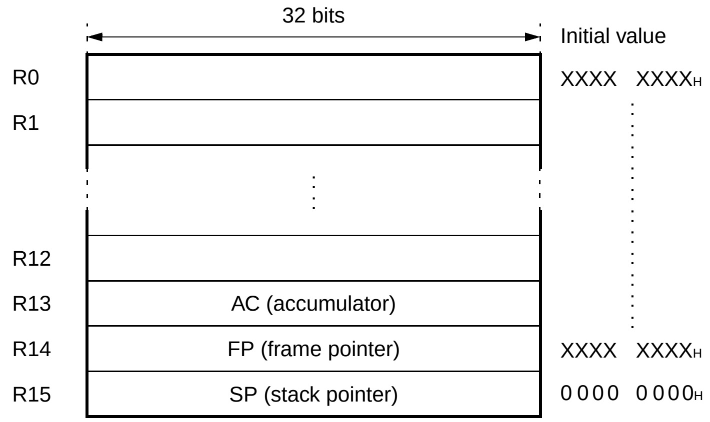
ILM4 to ILM0: Register for holding interrupt level mask value. The value held by this register is used as a level mask. When an interrupt request issued to the CPU is higher than the level held by ILM, the interrupt request is accepted.

ILM4	ILM3	ILM2	ILM1	ILM0	Interrupt level	High-low
0	0	0	0	0	0	High
		⋮			⋮	↑
0	1	0	0	0	15	
		⋮			⋮	↓
1	1	1	1	1	31	Low

■ GENERAL-PURPOSE REGISTERS

R0 to R15 are general-purpose registers embedded on the CPU. These registers functions as an accumulator and a memory access pointer (field for indicating address).

- **Register bank structure**



Of the above 16 registers, following registers have special functions. To support the special functions, part of the instruction set has been sophisticated to have enhanced functions.

R13: Virtual accumulator (AC)
R14: Frame pointer (FP)
R15: Stack pointer (SP)

Upon reset, values in R0 to R14 are not fixed. Value in R15 is initialized to be 0000 0000_H (SSP value).

■ SETTING MODE

1. Pin

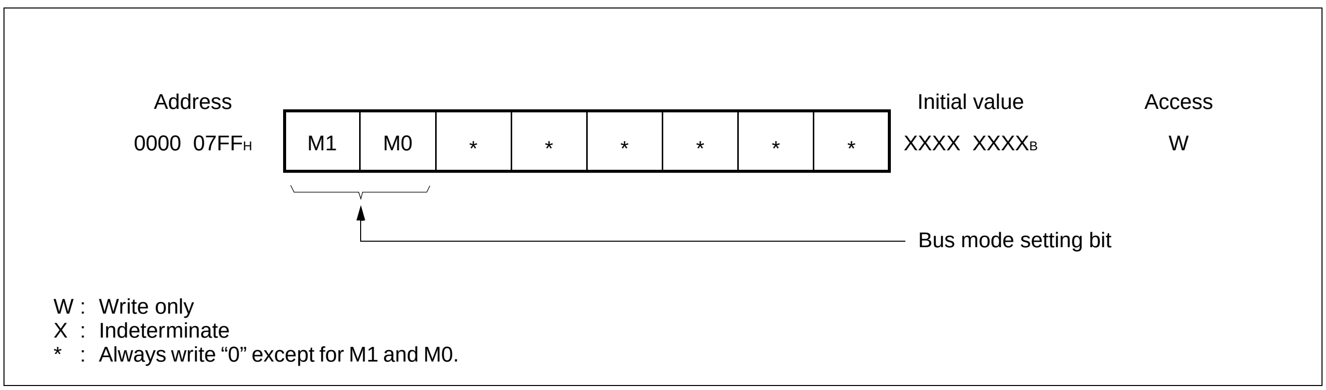
- **Mode setting pins and modes**

Mode setting pins			Mode name	Reset vector access area	External data bus width	Bus mode
MD2	MD1	MD0				
0	0	0	External vector mode 0	External	8 bits	External ROM/external bus mode
0	0	1	External vector mode 1	External	16 bits	
0	1	0	—	—	—	Inhibited
0	1	1	Internal vector mode	Internal	(Mode register)	Single-chip mode*
1	—	—	—	—	—	Not use

*: MB91F109 support single-chip mode.

2. Registers

- **Mode setting registers (MODR) and modes**



- **Bus mode setting bits and functions**

M1	M0	Functions	Note
0	0	Single-chip mode	
0	1	Internal ROM/external bus mode	
1	0	External ROM/external bus mode	
1	1	—	Inhibited

■ I/O MAP

Address	Register name (abbreviated)	Register name	Read/write	Resources name	Initial value
000000H	PDR3	Port 3 data register	R/W	Port 3	XXXXXXXXB
000001H	PDR2	Port 2 data register	R/W	Port 2	XXXXXXXXB
000002H	(Vacancy)				
000003H					
000004H	PDR7	Port 7 data register	R/W	Port 7	– – – – – – – XB
000005H	PDR6	Port 6 data register	R/W	Port 6	XXXXXXXXB
000006H	PDR5	Port 5 data register	R/W	Port 5	XXXXXXXXB
000007H	PDR4	Port 4 data register	R/W	Port 4	XXXXXXXXB
000008H	PDRB	Port B data register	R/W	Port B	XXXXXXXXB
000009H	PDRA	Port A data register	R/W	Port A	– XXXXXXXB
00000AH	(Vacancy)				
00000BH	PDR8	Port 8 data register	R/W	Port 8	– – XXXXXXB
00000CH to 000011H	(Vacancy)				
000012H	PDRE	Port E data register	R/W	Port E	XXXXXXXXB
000013H	PDRF	Port F data register	R/W	Port F	XXXXXXXXB
000014H to 00001BH	(Vacancy)				
00001CH	SSR0	Serial status register 0	R/W	UART0	00001 – 00B
00001DH	SIDR0/SODR0	Serial input data register 0/serial output data register 0	R/W		XXXXXXXXB
00001EH	SCR0	Serial control register 0	R/W		00000100B
00001FH	SMR0	Serial mode register 0	R/W		00 – – 0 – 00B
000020H	SSR1	Serial status register 1	R/W	UART1	00001 – 00B
000021H	SIDR1/SODR1	Serial input data register 1/serial output data register 1	R/W		XXXXXXXXB
000022H	SCR1	Serial control register 1	R/W		00000100B
000023H	SMR1	Serial mode register 1	R/W		00 – – 0 – 00B
000024H	SSR2	Serial status register 2	R/W	UART2	00001 – 00B
000025H	SIDR2/SODR2	Serial input data register 2/serial output data register 2	R/W		XXXXXXXXB
000026H	SCR2	Serial control register 2	R/W		00000100B
000027H	SMR2	Serial mode register 2	R/W		00 – – 0 – 00B

(Continued)

Address	Register name (abbreviated)	Register name	Read/write	Resources name	Initial value
000028H	TMRLR0	16-bit reload register 0	W	16-bit reload timer 0	XXXXXXXXB
000029H					XXXXXXXXB
00002AH	TMR0	16-bit timer register 0	R		XXXXXXXXB
00002BH					XXXXXXXXB
00002CH	(Vacancy)				
00002DH					
00002EH	TMCSR0	16-bit reload timer control status register 0	R/W	16-bit reload timer 0	––––0000B
00002FH					00000000B
000030H	TMRLR1	16-bit reload register 1	W	16-bit reload timer 1	XXXXXXXXB
000031H					XXXXXXXXB
000032H	TMR1	16-bit timer register 1	R		XXXXXXXXB
000033H					XXXXXXXXB
000034H	(Vacancy)				
000035H					
000036H	TMCSR1	16-bit reload timer control status register 1	R/W	16-bit reload timer 1	––––0000B
000037H					00000000B
000038H	ADCR	A/D converter data register	R	10-bit A/D converter	000000XXB
000039H					XXXXXXXXB
00003AH	ADCS	A/D converter control status register	R/W		00000000B
00003BH					00000000B
00003CH	TMRLR2	16-bit reload register 2	W	16-bit reload timer 2	XXXXXXXXB
00003DH					XXXXXXXXB
00003EH	TMR2	16-bit timer register 2	R		XXXXXXXXB
00003FH					XXXXXXXXB
000040H	(Vacancy)				
000041H					
000042H	TMCSR2	16-bit reload timer control status register 2	R/W	16-bit reload timer 2	––––0000B
000043H					00000000B
000044H to 000077H	(Vacancy)				

(Continued)

Address	Register name (abbreviated)	Register name	Read/write	Resources name	Initial value
000078_H	UTIM0/UTIMR0	U-TIMER register ch. 0 /U-TIMER reload register ch. 0	R/W	U-TIMER 0	00000000_B
000079_H					00000000_B
$00007A_H$	(Vacancy)				
$00007B_H$	UTIMC0	U-TIMER control register ch. 0	R/W	U-TIMER 0	0 – – 0 0 0 0 1_B
$00007C_H$	UTIM1/UTIMR1	U-TIMER register ch. 1/reload register ch. 1	R/W	U-TIMER 1	00000000_B
$00007D_H$					00000000_B
$00007E_H$	(Vacancy)				
$00007F_H$	UTIMC1	U-TIMER control register ch. 1	R/W	U-TIMER 1	0 – – 0 0 0 0 1_B
000080_H	UTIM2/UTIMR2	U-TIMER register ch. 2/U-TIMER reload register ch. 2	R/W	U-TIMER 2	00000000_B
000081_H					00000000_B
000082_H	(Vacancy)				
000083_H	UTIMC2	U-TIMER control register ch. 2	R/W	U-TIMER 2	0 – – 0 0 0 0 1_B
000084_H to 000093_H	(Vacancy)				
000094_H	EIRR	External interrupt cause register	R/W	External interrupt/ NMI	00000000_B
000095_H	ENIR	Interrupt enable register	R/W		00000000_B
000096_H to 000098_H	(Vacancy)				
000099_H	ELVR	External interrupt request level setting register	R/W	External interrupt/ NMI	00000000_B
$00009A_H$ to $0000D1_H$	(Vacancy)				
$0000D2_H$	DDRE	Port E data direction register	W	Port E	00000000_B
$0000D3_H$	DDRF	Port F data direction register	W	Port F	00000000_B
$0000D4_H$ to $0000DB_H$	(Vacancy)				
$0000DC_H$	GCN1	General control register 1	R/W	PWM timer 1	00110010_B
$0000DD_H$					00010000_B
$0000DE_H$	(Vacancy)				
$0000DF_H$	GCN2	General control register 2	R/W	PWM timer 2	00000000_B

(Continued)

Address	Register name (abbreviated)	Register name	Read/write	Resources name	Initial value
0000E0H	PTMR0	PWM timer register 0	R	PWM timer 0	1 1 1 1 1 1 1 1 B
0000E1H					1 1 1 1 1 1 1 1 B
0000E2H	PCSR0	PWM cycle setting register 0	W		X X X X X X X X B
0000E3H					X X X X X X X X B
0000E4H	PDUT0	PWM duty setting register 0	W		X X X X X X X X B
0000E5H					X X X X X X X X B
0000E6H	PCNH0	Control status register H 0	R/W		0 0 0 0 0 0 0 – B
0000E7H	PCNL0	Control status register L 0	R/W		0 0 0 0 0 0 0 0 B
0000E8H	PTMR1	PWM timer register 1	R	PWM timer 1	1 1 1 1 1 1 1 1 B
0000E9H					1 1 1 1 1 1 1 1 B
0000EAH	PCSR1	PWM cycle setting register 1	W		X X X X X X X X B
0000EBH					X X X X X X X X B
0000ECH	PDUT1	PWM duty setting register 1	W		X X X X X X X X B
0000EDH					X X X X X X X X B
0000EEH	PCNH1	Control status register H 1	R/W		0 0 0 0 0 0 0 – B
0000EFH	PCNL1	Control status register L 1	R/W		0 0 0 0 0 0 0 0 B
0000F0H	PTMR2	PWM timer register 2	R	PWM timer 2	1 1 1 1 1 1 1 1 B
0000F1H					1 1 1 1 1 1 1 1 B
0000F2H	PCSR2	PWM cycle setting register 2	W		X X X X X X X X B
0000F3H					X X X X X X X X B
0000F4H	PDUT2	PWM duty setting register 2	W		X X X X X X X X B
0000F5H					X X X X X X X X B
0000F6H	PCNH2	Control status register H 2	R/W		0 0 0 0 0 0 0 – B
0000F7H	PCNL2	Control status register L 2	R/W		0 0 0 0 0 0 0 0 B
0000F8H	PTMR3	PWM timer register 3	R	PWM timer 3	1 1 1 1 1 1 1 1 B
0000F9H					1 1 1 1 1 1 1 1 B
0000FAH	PCSR3	PWM cycle setting register 3	W		X X X X X X X X B
0000FBH					X X X X X X X X B
0000FCH	PDUT3	PWM duty setting register 3	W		X X X X X X X X B
0000FDH					X X X X X X X X B
0000FEH	PCNH3	Control status register H 3	R/W		0 0 0 0 0 0 0 – B
0000FFH	PCNL3	Control status register L 3	R/W		0 0 0 0 0 0 0 0 B

(Continued)

Address	Register name (abbreviated)	Register name	Read/write	Resources name	Initial value
000100H to 0001FFH	(Vacancy)				
000200H	DPDP	DMAC parameter descriptor pointer	R/W	DMA controller (DMAC)	XXXXXXXXB
000201H					XXXXXXXXB
000202H					XXXXXXXXB
000203H					X0000000B
000204H	DACSR	DMAC control status register	R/W		00000000B
000205H					00000000B
000206H					00000000B
000207H					00000000B
000208H	DATCR	DMAC pin control register	R/W		XXXXXXXXB
000209H					XX000000B
00020AH					XX000000B
00020BH					XX000000B
00020CH to 0003EFH	(Vacancy)				
0003F0H	BSD0	Bit search module 0-detection data register	R/W	Bit search module	XXXXXXXXB
0003F1H					XXXXXXXXB
0003F2H					XXXXXXXXB
0003F3H					XXXXXXXXB
0003F4H	BSD1	Bit search module 1-detection data register	R/W		XXXXXXXXB
0003F5H					XXXXXXXXB
0003F6H					XXXXXXXXB
0003F7H					XXXXXXXXB
0003F8H	BSDC	Bit search module transition-detection data register	W		XXXXXXXXB
0003F9H					XXXXXXXXB
0003FAH					XXXXXXXXB
0003FBH					XXXXXXXXB
0003FCH	BSRR	Bit search module detection result register	R		XXXXXXXXB
0003FDH					XXXXXXXXB
0003FEH					XXXXXXXXB
0003FFH					XXXXXXXXB

(Continued)

Address	Register name (abbreviated)	Register name	Read/write	Resources name	Initial value
000400H	ICR00	Interrupt control register 0	R/W	Interrupt controller	– – – 1 1 1 1 1 B
000401H	ICR01	Interrupt control register 1	R/W		– – – 1 1 1 1 1 B
000402H	ICR02	Interrupt control register 2	R/W		– – – 1 1 1 1 1 B
000403H	ICR03	Interrupt control register 3	R/W		– – – 1 1 1 1 1 B
000404H	ICR04	Interrupt control register 4	R/W		– – – 1 1 1 1 1 B
000405H	ICR05	Interrupt control register 5	R/W		– – – 1 1 1 1 1 B
000406H	ICR06	Interrupt control register 6	R/W		– – – 1 1 1 1 1 B
000407H	ICR07	Interrupt control register 7	R/W		– – – 1 1 1 1 1 B
000408H	ICR08	Interrupt control register 8	R/W		– – – 1 1 1 1 1 B
000409H	ICR09	Interrupt control register 9	R/W		– – – 1 1 1 1 1 B
00040AH	ICR10	Interrupt control register 10	R/W		– – – 1 1 1 1 1 B
00040BH	ICR11	Interrupt control register 11	R/W		– – – 1 1 1 1 1 B
00040CH	ICR12	Interrupt control register 12	R/W		– – – 1 1 1 1 1 B
00040DH	ICR13	Interrupt control register 13	R/W		– – – 1 1 1 1 1 B
00040EH	ICR14	Interrupt control register 14	R/W		– – – 1 1 1 1 1 B
00040FH	ICR15	Interrupt control register 15	R/W		– – – 1 1 1 1 1 B
000410H	ICR16	Interrupt control register 16	R/W		– – – 1 1 1 1 1 B
000411H	ICR17	Interrupt control register 17	R/W		– – – 1 1 1 1 1 B
000412H	ICR18	Interrupt control register 18	R/W		– – – 1 1 1 1 1 B
000413H	ICR19	Interrupt control register 19	R/W		– – – 1 1 1 1 1 B
000414H	ICR20	Interrupt control register 20	R/W		– – – 1 1 1 1 1 B
000415H	ICR21	Interrupt control register 21	R/W		– – – 1 1 1 1 1 B
000416H	ICR22	Interrupt control register 22	R/W		– – – 1 1 1 1 1 B
000417H	ICR23	Interrupt control register 23	R/W		– – – 1 1 1 1 1 B
000418H	ICR24	Interrupt control register 24	R/W		– – – 1 1 1 1 1 B
000419H	ICR25	Interrupt control register 25	R/W		– – – 1 1 1 1 1 B
00041AH	ICR26	Interrupt control register 26	R/W		– – – 1 1 1 1 1 B
00041BH	ICR27	Interrupt control register 27	R/W		– – – 1 1 1 1 1 B
00041CH	ICR28	Interrupt control register 28	R/W		– – – 1 1 1 1 1 B
00041DH	ICR29	Interrupt control register 29	R/W		– – – 1 1 1 1 1 B
00041EH	ICR30	Interrupt control register 30	R/W		– – – 1 1 1 1 1 B
00041FH	ICR31	Interrupt control register 31	R/W		– – – 1 1 1 1 1 B

(Continued)

Address	Register name (abbreviated)	Register name	Read/write	Resources name	Initial value
000420H to 00042EH	(Vacancy)				
00042FH	ICR47	Interrupt control register 47	R/W	Interrupt controller	– – – 1 1 1 1 1 B
000430H	DICR	Delayed interrupt control register	R/W		– – – – – – – 0 B
000431H	HRCL	Hold request cancel request level setting register	R/W		– – – 1 1 1 1 1 B
000432H to 00047FH	(Vacancy)				
000480H	RSRR/WTCR	Reset cause register/ watchdog cycle control register	R/W	Clock generator	1X X X X – 0 0 B
000481H	STCR	Standby control register	R/W		0 0 0 1 1 1 – – B
000482H	PDRR	DMA controller request squelch register	R/W		– – – – 0 0 0 0 B
000483H	CTBR	Timebase timer clear register	W		X X X X X X X X B
000484H	GCR	Gear control register	R/W		1 1 0 0 1 1 – 1 B
000485H	WPR	Watchdog reset occurrence postpone register	W		X X X X X X X X B
000486H	(Vacancy)				
000487H					
000488H	PCTR	PLL control register	R/W	PLL control	0 0 – – 0 – – – B
000489H to 0005FFH	(Vacancy)				
000600H	DDR3	Port 3 data direction register	W	Port 3	0 0 0 0 0 0 0 0 B
000601H	DDR2	Port 2 data direction register	W	Port 2	0 0 0 0 0 0 0 0 B
000602H 000603H	(Vacancy)				
000604H	DDR7	Port 7 data direction register	W	Port 7	– – – – – – – 0 B
000605H	DDR6	Port 6 data direction register	W	Port 6	0 0 0 0 0 0 0 0 B
000606H	DDR5	Port 5 data direction register	W	Port 5	0 0 0 0 0 0 0 0 B
000607H	DDR4	Port 4 data direction register	W	Port 4	0 0 0 0 0 0 0 0 B
000608H	DDRB	Port B data direction register	W	Port B	0 0 0 0 0 0 0 0 B
000609H	DDRA	Port A data direction register	W	Port A	– 0 0 0 0 0 0 0 B
00060AH	(Vacancy)				
00060BH	DDR8	Port 8 data direction register	W	Port 8	– – 0 0 0 0 0 0 B

(Continued)

Address	Register name (abbreviated)	Register name	Read/write	Resources name	Initial value
00060CH	ASR1	Area select register 1	W	External bus interface	0 0 0 0 0 0 0 0 B
00060DH					0 0 0 0 0 0 0 1 B
00060EH	AMR1	Area mask register 1	W		0 0 0 0 0 0 0 0 B
00060FH					0 0 0 0 0 0 0 0 B
000610H	ASR2	Area select register 2	W		0 0 0 0 0 0 0 0 B
000611H					0 0 0 0 0 0 1 0 B
000612H	AMR2	Area mask register 2	W		0 0 0 0 0 0 0 0 B
000613H					0 0 0 0 0 0 0 0 B
000614H	ASR3	Area select register 3	W		0 0 0 0 0 0 0 0 B
000615H					0 0 0 0 0 0 1 1 B
000616H	AMR3	Area mask register 3	W		0 0 0 0 0 0 0 0 B
000617H					0 0 0 0 0 0 0 0 B
000618H	ASR4	Area select register 4	W		0 0 0 0 0 0 0 0 B
000619H					0 0 0 0 0 1 0 0 B
00061AH	AMR4	Area mask register 4	W		0 0 0 0 0 0 0 0 B
00061BH					0 0 0 0 0 0 0 0 B
00061CH	ASR5	Area select register 5	W		0 0 0 0 0 0 0 0 B
00061DH					0 0 0 0 0 1 0 1 B
00061EH	AMR5	Area mask register 5	W		0 0 0 0 0 0 0 0 B
00061FH					0 0 0 0 0 0 0 0 B
000620H	AMD0	Area mode register 0	R/W		– – – 0 0 1 1 1 B
000621H	AMD1	Area mode register 1	R/W		0 – – 0 0 0 0 0 B
000622H	AMD32	Area mode register 32	R/W		0 0 0 0 0 0 0 0 B
000623H	AMD4	Area mode register 4	R/W		0 – – 0 0 0 0 0 B
000624H	AMD5	Area mode register 5	R/W		0 – – 0 0 0 0 0 B
000625H	DSCR	DRAM signal control register	W		0 0 0 0 0 0 0 0 B
000626H	RFCR	Refresh control register	R/W		– – X X X X X X B
000627H					0 0 – – – 0 0 0 B
000628H	EPCR0	External pin control register 0	W		– – – – 1 1 0 0 B
000629H					– 1 1 1 1 1 1 1 B
00062AH	EPCR1	External pin control register 1	W		– – – – – – – 1 B
00062BH					1 1 1 1 1 1 1 1 B
00062CH	DMCR4	DRAM control register 4	R/W		0 0 0 0 0 0 0 0 B
00062DH					0 0 0 0 0 0 0 – B
00062EH	DMCR5	DRAM control register 5	R/W		0 0 0 0 0 0 0 0 B
00062FH					0 0 0 0 0 0 0 – B

(Continued)

(Continued)

Address	Register name (abbreviated)	Register name	Read/write	Resources name	Initial value
000630H to 0007BFH	(Vacancy)				
0007C0H	FSTR	FLASH memory status register	R/W	FLASH memory	0 0 0 X X X X 0 B
0007C1H to 0007FDH	(Vacancy)				
0007FEH	LER	Little endian register	W	External bus interface	– – – – – 0 0 0 B
0007FFH	MODR	Mode register	W		X X X X X X X X B

About Programming

R/W: Readable and writable
R: Read only
W: Write only

Explanation of initial values

0: The initial value of this bit is “0”.
1: The initial value of this bit is “1”.
X: The initial value of this bit is undefined.
–: This bit is not used. The initial value of this bit is undefined.

RMW system instructions (RMW: Read Modify Write)

AND	Rj, @ Ri	OR	Rj, @ Ri	EOR	Rj, @ Ri
ANDH	Rj, @ Ri	ORH	Rj, @ Ri	EORH	Rj, @ Ri
ANDB	Rj, @ Ri	ORB	Rj, @ Ri	EORB	Rj, @ Ri
BANDL	#µ4, @ Ri	BORL	#µ4, @ Ri	BEORL	#µ4, @ Ri
BANDH	#µ4, @ Ri	BORH	#µ4, @ Ri	BEORH	#µ4, @ Ri

Notes:
- Never execute a RMW system instruction to the resistor has a write only bit.
- The area “vacancy” on the I/O map is reserved area. Access to this area are deal with to an internal area. No access signals to the external area would be generated.

■ INTERRUPT CAUSES, INTERRUPT VECTORS AND INTERRUPT CONTROL REGISTER ALLOCATIONS

Interrupt causes	Interrupt number		Interrupt level		TBR default address
	Decimal	Hexadecimal	Register	Offset	
Reset	0	00	—	$3FC_H$	$000FFFFC_H$
Reserved for system	1	01	—	$3F8_H$	$000FFFF8_H$
Reserved for system	2	02	—	$3F4_H$	$000FFFF4_H$
Reserved for system	3	03	—	$3F0_H$	$000FFFF0_H$
Reserved for system	4	04	—	$3EC_H$	$000FFFEC_H$
Reserved for system	5	05	—	$3E8_H$	$000FFFE8_H$
Reserved for system	6	06	—	$3E4_H$	$000FFFE4_H$
Reserved for system	7	07	—	$3E0_H$	$000FFFE0_H$
Reserved for system	8	08	—	$3DC_H$	$000FFFDC_H$
Reserved for system	9	09	—	$3D8_H$	$000FFFD8_H$
Reserved for system	10	0A	—	$3D4_H$	$000FFFD4_H$
Reserved for system	11	0B	—	$3D0_H$	$000FFFD0_H$
Reserved for system	12	0C	—	$3CC_H$	$000FFFCC_H$
Reserved for system	13	0D	—	$3C8_H$	$000FFFC8_H$
Exception for undefined instruction	14	0E	—	$3C4_H$	$000FFFC4_H$
NMI request	15	0F	F_H fixed	$3C0_H$	$000FFFC0_H$
External interrupt 0	16	10	ICR00	$3BC_H$	$000FFFBC_H$
External interrupt 1	17	11	ICR01	$3B8_H$	$000FFFB8_H$
External interrupt 2	18	12	ICR02	$3B4_H$	$000FFFB4_H$
External interrupt 3	19	13	ICR03	$3B0_H$	$000FFFB0_H$
UART0 receive complete	20	14	ICR04	$3AC_H$	$000FFFAC_H$
UART1 receive complete	21	15	ICR05	$3A8_H$	$000FFFA8_H$
UART2 receive complete	22	16	ICR06	$3A4_H$	$000FFFA4_H$
UART0 transmit complete	23	17	ICR07	$3A0_H$	$000FFFA0_H$
UART1 transmit complete	24	18	ICR08	$39C_H$	$000FFF9C_H$
UART2 transmit complete	25	19	ICR09	398_H	$000FFF98_H$
DMAC0 (complete, error)	26	1A	ICR10	394_H	$000FFF94_H$
DMAC1 (complete, error)	27	1B	ICR11	390_H	$000FFF90_H$
DMAC2 (complete, error)	28	1C	ICR12	$38C_H$	$000FFF8C_H$
DMAC3 (complete, error)	29	1D	ICR13	388_H	$000FFF88_H$
DMAC4 (complete, error)	30	1E	ICR14	384_H	$000FFF84_H$
DMAC5 (complete, error)	31	1F	ICR15	380_H	$000FFF80_H$

(Continued)

Interrupt causes	Interrupt number		Interrupt level		TBR default address
	Decimal	Hexadecimal	Register	Offset	
DMAC6 (complete, error)	32	20	ICR16	37CH	000FFF7CH
DMAC7 (complete, error)	33	21	ICR17	378H	000FFF78H
A/D converter (successive approximation conversion type)	34	22	ICR18	374H	000FFF74H
16-bit reload timer 0	35	23	ICR19	370H	000FFF70H
16-bit reload timer 1	36	24	ICR20	36CH	000FFF6CH
16-bit reload timer 2	37	25	ICR21	368H	000FFF68H
PWM 0	38	26	ICR22	364H	000FFF64H
PWM 1	39	27	ICR23	360H	000FFF60H
PWM 2	40	28	ICR24	35CH	000FFF5CH
PWM 3	41	29	ICR25	358H	000FFF58H
U-TIMER 0	42	2A	ICR26	354H	000FFF54H
U-TIMER 1	43	2B	ICR27	350H	000FFF50H
U-TIMER 2	44	2C	ICR28	34CH	000FFF4CH
FLASH memory	45	2D	ICR29	348H	000FFF48H
Reserved for system	46	2E	ICR30	344H	000FFF44H
Reserved for system	47	2F	ICR31	340H	000FFF40H
Reserved for system	48	30	—	33CH	000FFF3CH
Reserved for system	49	31	—	338H	000FFF38H
Reserved for system	50	32	—	334H	000FFF34H
Reserved for system	51	33	—	330H	000FFF30H
Reserved for system	52	34	—	32CH	000FFF2CH
Reserved for system	53	35	—	328H	000FFF28H
Reserved for system	54	36	—	324H	000FFF24H
Reserved for system	55	37	—	320H	000FFF20H
Reserved for system	56	38	—	31CH	000FFF1CH
Reserved for system	57	39	—	318H	000FFF18H
Reserved for system	58	3A	—	314H	000FFF14H
Reserved for system	59	3B	—	310H	000FFF10H
Reserved for system	60	3C	—	30CH	000FFF0CH
Reserved for system	61	3D	—	308H	000FFF08H
Reserved for system	62	3E	—	304H	000FFF04H
Delayed interrupt cause bit	63	3F	ICR47	300H	000FFF00H

(Continued)

(Continued)

Interrupt causes	Interrupt number		Interrupt level		TBR default address
	Decimal	Hexadecimal	Register	Offset	
Reserved for system (used in REALOS*)	64	40	—	2FC$_H$	000FFEFC$_H$
Reserved for system (used in REALOS*)	65	41	—	2F8$_H$	000FFEF8$_H$
Used in INT instructions	66 to 255	42 to FF	—	2F4$_H$ to 000$_H$	000FFEF4$_H$ to 000FFD00$_H$

*: When using in REALOS/FR, interrupt 0x40, 0x41 for system code.

■ PERIPHERAL RESOURCES

1. I/O Ports

There are 2 types of I/O port register structure; port data register (PDR0 to PDRF) and data direction register (DDR0 to DDRF), where bits PDR0 to PDRF and bits DDR0 to DDRF corresponds respectively. Each bit on the register corresponds to an external pin. In port registers input/output register of the port configures input/output function of the port, while corresponding bit (pin) configures input/output function in data direction registers. Bit “0” specifies input and “1” specifies output.

- For input (DDR = “0”) setting;
  PDR reading operation: reads level of corresponding external pin.
  PDR writing operation: writes set value to PDR.
- For output (DDR = “1”) setting;
  PDR reading operation: reads PDR value.
  PDR writing operation: outputs PDR value to corresponding external pin.

(1) Register configuration

• Port data register

Address	bit 7 — bit 0	Initial value	
000001H	PDR2	XXXXXXXXB	(R/W)
000000H	PDR3	XXXXXXXXB	(R/W)
000007H	PDR4	XXXXXXXXB	(R/W)
000006H	PDR5	XXXXXXXXB	(R/W)
000005H	PDR6	XXXXXXXXB	(R/W)
000004H	PDR7	- - - - - - - XB	(R/W)
00000BH	PDR8	- - XXXXXXB	(R/W)
000009H	PDRA	- XXXXXXXB	(R/W)
000008H	PDRB	XXXXXXXXB	(R/W)
000012H	PDRE	XXXXXXXXB	(R/W)
000013H	PDRF	XXXXXXXXB	(R/W)

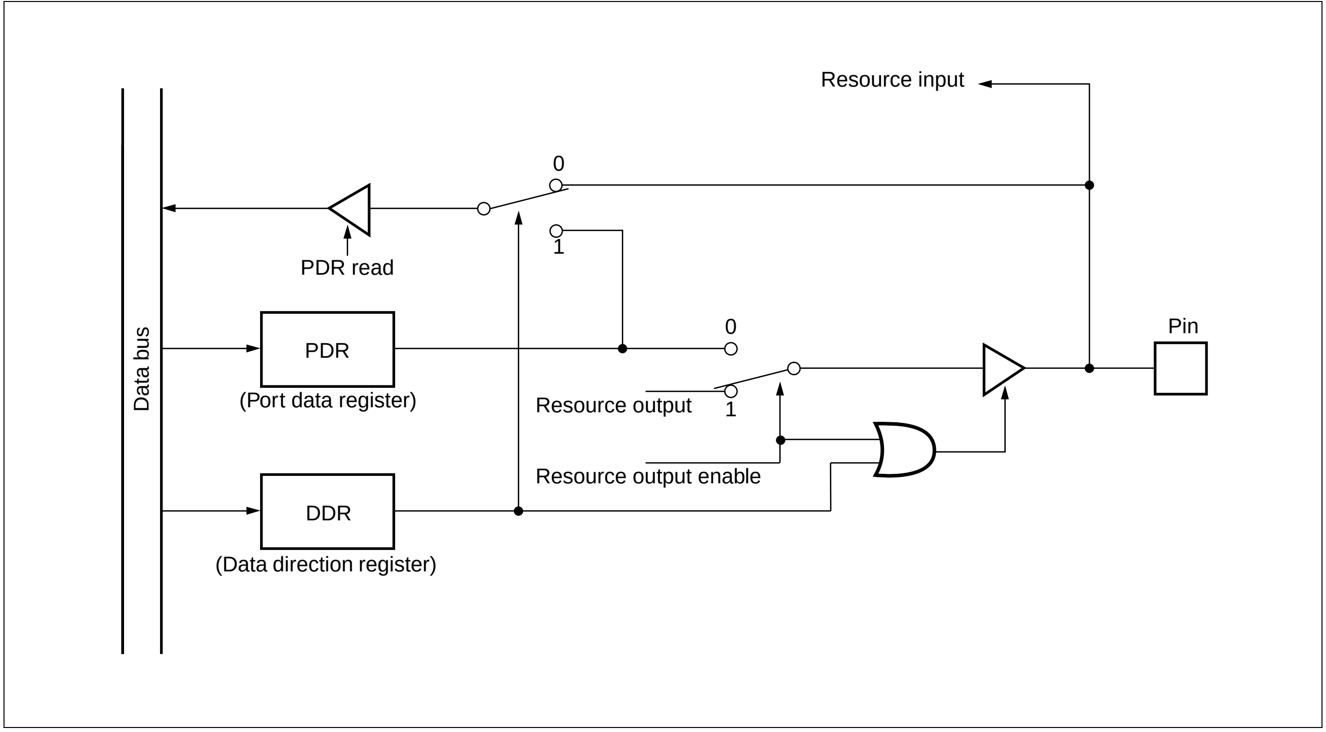
( ) : Access
R/W : Readable and writable
X : Indeterminate

- **Data direction register**

Address	bit 7 … bit 0	Initial value	
000601H	DDR2	0 0 0 0 0 0 0 0 B	(W)
000600H	DDR3	0 0 0 0 0 0 0 0 B	(W)
000607H	DDR4	0 0 0 0 0 0 0 0 B	(W)
000606H	DDR5	0 0 0 0 0 0 0 0 B	(W)
000605H	DDR6	0 0 0 0 0 0 0 0 B	(W)
000604H	DDR7	- - - - - - - 0 B	(W)
00060BH	DDR8	- - 0 0 0 0 0 0 B	(W)
000609H	DDRA	- 0 0 0 0 0 0 0 B	(W)
000608H	DDRB	0 0 0 0 0 0 0 0 B	(W)
0000D2H	DDRE	0 0 0 0 0 0 0 0 B	(W)
0000D3H	DDRF	0 0 0 0 0 0 0 0 B	(W)

( ) : Access
W : Write only
– : Unused

(2) Block diagram



2. DMA Controller (DMAC)

The DMA controller is a module embedded in FR family devices, and performs DMA (direct memory access) transfer.

DMA transfer performed by the DMA controller transfers data without intervention of CPU, contributing to enhanced performance of the system.

- 8 channels
- Mode: single/block transfer, burst transfer and continuous transfer: 3 kinds of transfer
- Transfer all through the area
- Max. 65536 of transfer cycles
- Interrupt function right after the transfer
- Selectable for address transfer increase/decrease by the software
- External transfer request input pin, external transfer request accept output pin, external transfer complete output pin three pins for each

(1) Registers configuration

- **DMAC internal registers**

Register	Address	bit 31 … bit 0	Initial value	Access
DMAC parameter descriptor pointer	00000200H	DPDP	XXXXXXXXB XXXXXXXXB XXXXXXXXB X0000000B	(R/W)
DMAC control status register	00000204H	DACSR	00000000B 00000000B 00000000B 00000000B	(R/W)
DMAC pin control register	00000208H	DATCR	XXXXXXXXB XX000000B XX000000B XX000000B	(R/W)

( ) : Access
R/W : Readable and writable
X : Indeterminate

- **DMAC descriptor**

- The first word of descriptor

bit 31 … bit 16	
DMACT	(R/W)

bit 15	bit 11 … bit 8	bit 7 … bit 0	
–	BLK		(R/W)

- The second word of descriptor

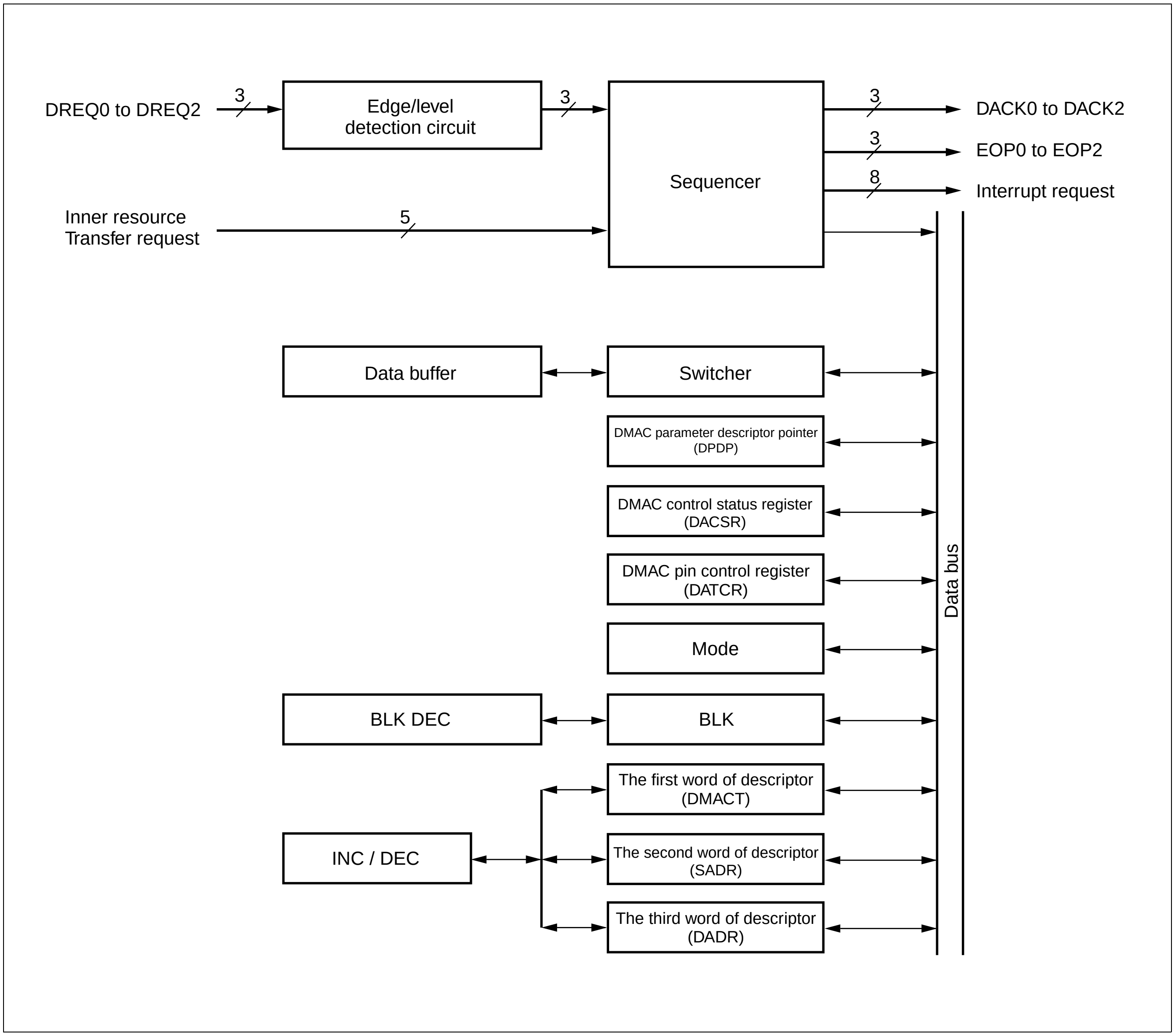
bit 31 … bit 0	
SADR	(R/W)

- The third word of descriptor

bit 31 … bit 0	
DADR	(R/W)

R/W: Readable and writable

(2) Block diagram



3. UART

The UART is a serial I/O port for supporting asynchronous (start-stop system) communication or CLK synchronous communication, and it has the following features.

The MB91F109 consists of 3 channels of UART.

- Full double double buffer
- Both a synchronous (start-stop system) communication and CLK synchronous communication are available.
- Supporting multi-processor mode
- Perfect programmable baud rate
  Any baud rate can be set by internal timer (refer to section “4. U-TIMER”).
- Any baud rate can be set by external clock.
- Error checking function (parity, framing and overrun)
- Transfer signal: NRZ code
- Enable DMA transfer/start by interrupt.

(1) Register configuration

- Serial control register 0 to 2

Address	bit 15 … bit 8	bit 7 … bit 0	Initial value
SCR0 : 00001E$_H$ SCR1 : 000022$_H$ SCR2 : 000026$_H$	SCR0 to SCR2	(SMR)	0 0 0 0 0 1 0 0$_B$ (R/W)

- Serial model register 0 to 2

Address	bit 15 … bit 8	bit 7 … bit 0	Initial value
SMR0 : 00001F$_H$ SMR1 : 000023$_H$ SMR2 : 000027$_H$	(SCR)	SMR0 to SMR2	0 0 - - 0 - 0 0$_B$ (R/W)

- Serial status register 0 to 2

Address	bit 15 … bit 8	bit 7 … bit 0	Initial value
SSR0 : 00001C$_H$ SSR1 : 000020$_H$ SSR2 : 000024$_H$	SSR0 to SSR2	(SIDR)	0 0 0 0 1 - 0 0$_B$ (R/W)

- Serial input data register 0 to 2

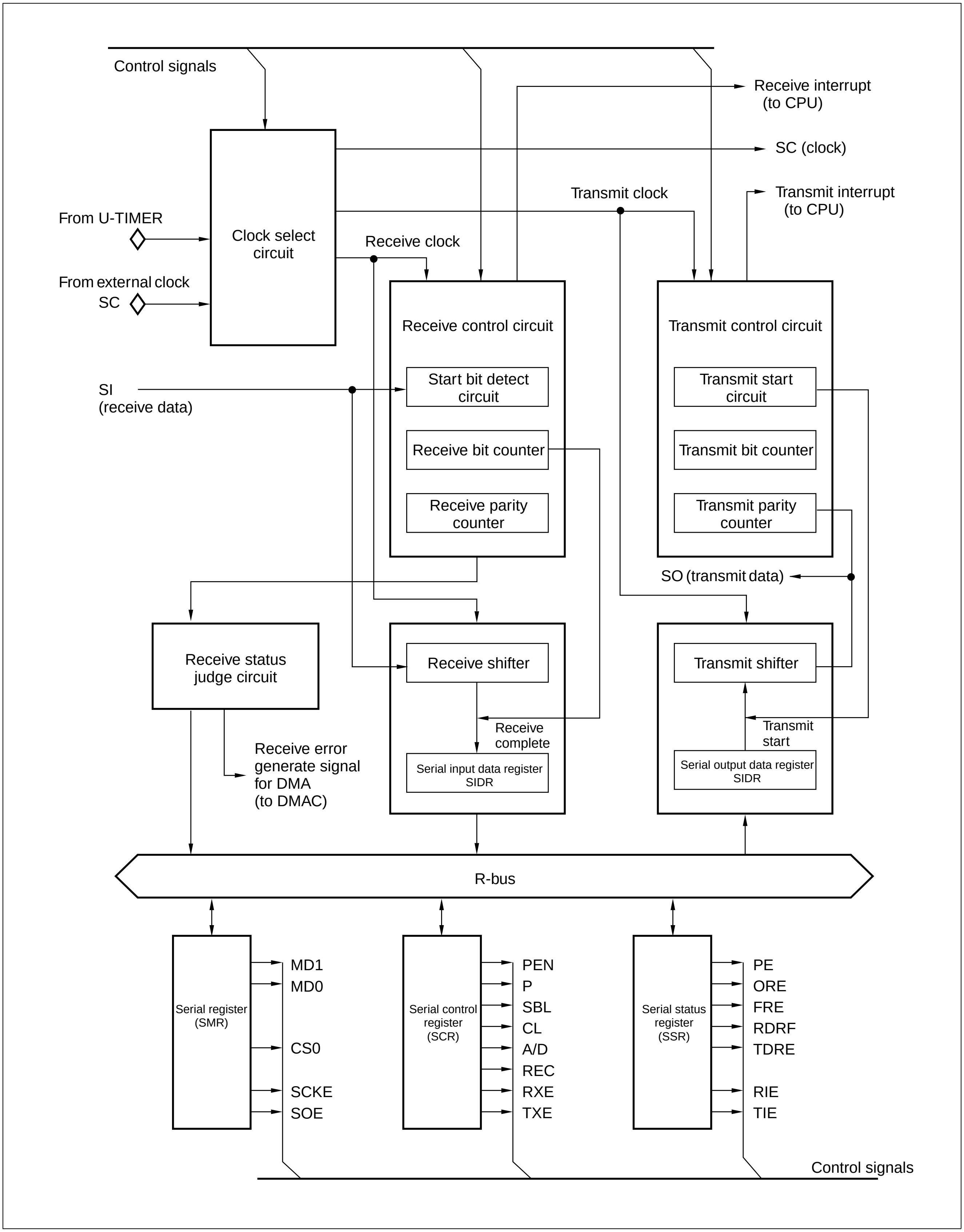
Address	bit 15 … bit 8	bit 7 … bit 0	Initial value
SIDR0 : 00001D$_H$ SIDR1 : 000021$_H$ SIDR2 : 000025$_H$	(SSR)	SIDR0 to SIDR2	X X X X X X X X$_B$ (R)

- Serial output data register 0 to 2

Address	bit 15 … bit 8	bit 7 … bit 0	Initial value
SODR0 : 00001D$_H$ SODR1 : 000021$_H$ SODR2 : 000025$_H$	(SSR)	SODR0 to SODR2	X X X X X X X X$_B$ (W)

( ) : Access
R/W : Readable and writable
– : Unused
X : Indeterminate

(2) Block diagram



4. U-TIMER (16-bit Timer for UART Baud Rate Generation)

The U-TIMER is a 16-bit timer for generating UART baud rate. Combination of chip operating frequency and reload value of U-TIMER allows flexible setting of baud rate.

The U-TIMER operates as an interval timer by using interrupt issued on counter underflow.

The MB91F109 has 3 channel U-TIMER embedded on the chip. When used as an interval timer, two couple of U-TIMER (ch0, ch1) can be cascaded and an interval of up to $2^{32} \times \phi$ can be counted.

(1) Register configuration

- U-TIMER register ch.0 to ch.2

Address	bit 15 … bit 0	Initial value
UTIM0 : 00000078H UTIM1 : 0000007CH UTIM2 : 00000080H	UTIM0 to UTIM2	0 0 0 0 0 0 0 0 B (R) 0 0 0 0 0 0 0 0 B

- U-TIMER reload register ch.0 to ch.2

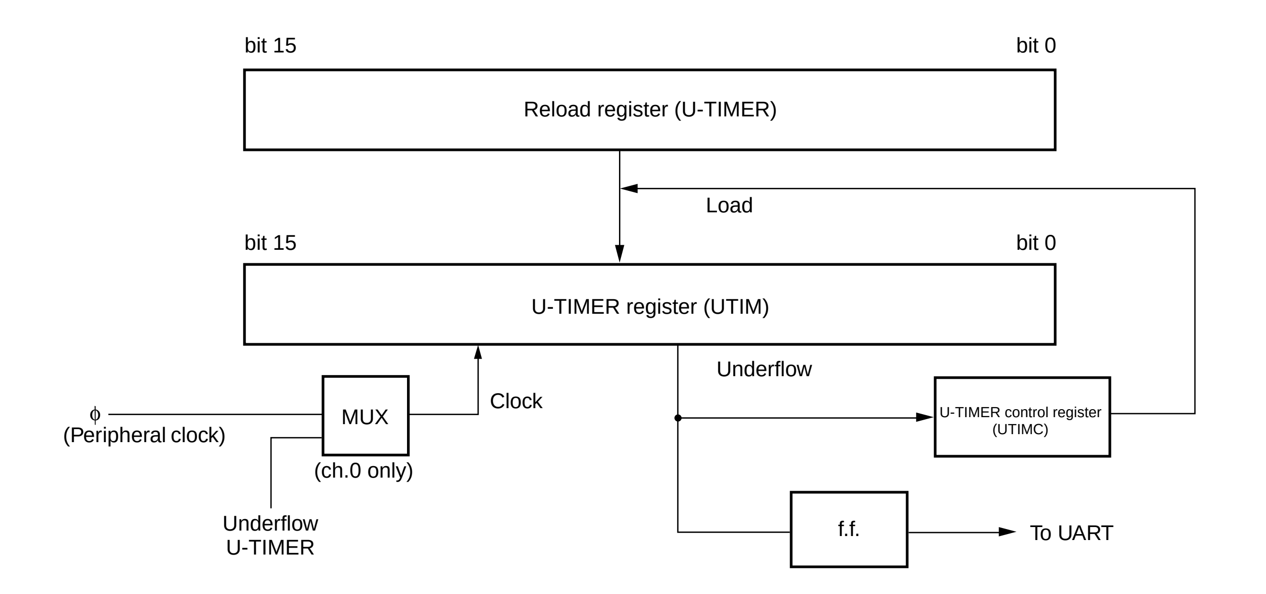
Address	bit 15 … bit 0	Initial value
UTIMR0 : 00000078H UTIMR1 : 0000007CH UTIMR2 : 00000080H	UTIMR0 to UTIMR2	0 0 0 0 0 0 0 0 B (W) 0 0 0 0 0 0 0 0 B

- U-TIMER control register ch.0 to ch.2

Address	bit 15 … bit 8	bit 7 … bit 0	Initial value
UTIMC0 : 0000007BH UTIMC1 : 0000007FH UTIMC2 : 00000083H	(Vacancy)	UTIMC0 to UTIMC2	0 - - 0 0 0 0 1 B (R/W)

( ) : Access
R/W : Readable and writable
– : Unused

(2) Block diagram



5. PWM Timer

The PWM timer can output high accurate PWM waves efficiently.

MB91F109 has inner 4-channel PWM timers, and has the following features.

- Each channel consists of a 16-bit down counter, a 16-bit data resister with a buffer for cycle setting, a 16-bit compare resister with a buffer for duty setting, and a pin controller.
- The count clock of a 16-bit down counter can be selected from the following four inner clocks.
  Inner clock ϕ, $\phi/4$, $\phi/16$, $\phi/64$
- The counter value can be initialized “$FFFF_H$” by the resetting or the counter borrow.
- PWM output (each channel)

(1) Register configuration

• Control status register H0 to 3

Address	bit 15 … bit 8	bit 7 … bit 0	Initial value
PCNH0 : 0000E6$_H$ PCNH1 : 0000EE$_H$ PCNH2 : 0000F6$_H$ PCNH3 : 0000FE$_H$	PCNH0 to PCNH3	(PCNL)	0 0 0 0 0 0 0 - $_B$ (R/W)

• Control status register L0 to 3

Address	bit 15 …	… bit 0	Initial value
PCNL0 : 0000E7$_H$ PCNL1 : 0000EF$_H$ PCNL2 : 0000F7$_H$ PCNL3 : 0000FF$_H$	(PCNH)	PCNL0 to PCNL3	0 0 0 0 0 0 0 0 $_B$ (R/W)

• PWM cycle setting register 0 to 3

Address	bit 15 … bit 0	Initial value
PCSR0 : 0000E2$_H$ PCSR1 : 0000EA$_H$ PCSR2 : 0000F2$_H$ PCSR3 : 0000FA$_H$	PCSR0 to PCSR3	X X X X X X X X $_B$ X X X X X X X X $_B$ (W)

• PWM duty setting register 0 to 3

Address	bit 15 … bit 0	Initial value
PDUT0 : 0000E4$_H$ PDUT1 : 0000EC$_H$ PDUT2 : 0000F4$_H$ PDUT3 : 0000FC$_H$	PDUT0 to PDUT3	X X X X X X X X $_B$ X X X X X X X X $_B$ (W)

• PWM timer register 0 to 3

Address	bit 15 … bit 0	Initial value
PTMR0 : 0000E0$_H$ PTMR1 : 0000E8$_H$ PTMR2 : 0000F0$_H$ PTMR3 : 0000F8$_H$	PTMR0 to PTMR3	1 1 1 1 1 1 1 1 $_B$ 1 1 1 1 1 1 1 1 $_B$ (R)

• General control register 1, 2

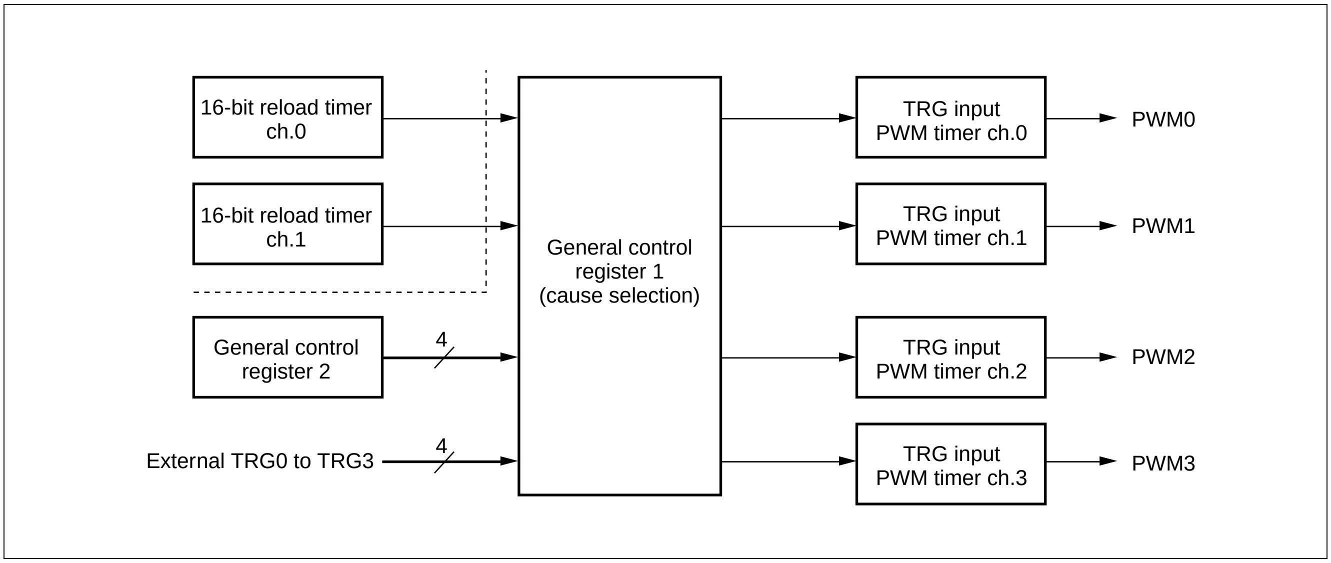
Address	bit 15 … bit 0	Initial value
GCN1 : 0000DC$_H$	GCN1	0 0 1 1 0 0 1 0 $_B$ 0 0 0 1 0 0 0 0 $_B$ (R/W)

Address	bit 15 … bit 8	bit 7 … bit 0	Initial value
GCN1 : 0000DF$_H$	(Vacancy)	GCN2	0 0 0 0 0 0 0 0 $_B$ (R/W)

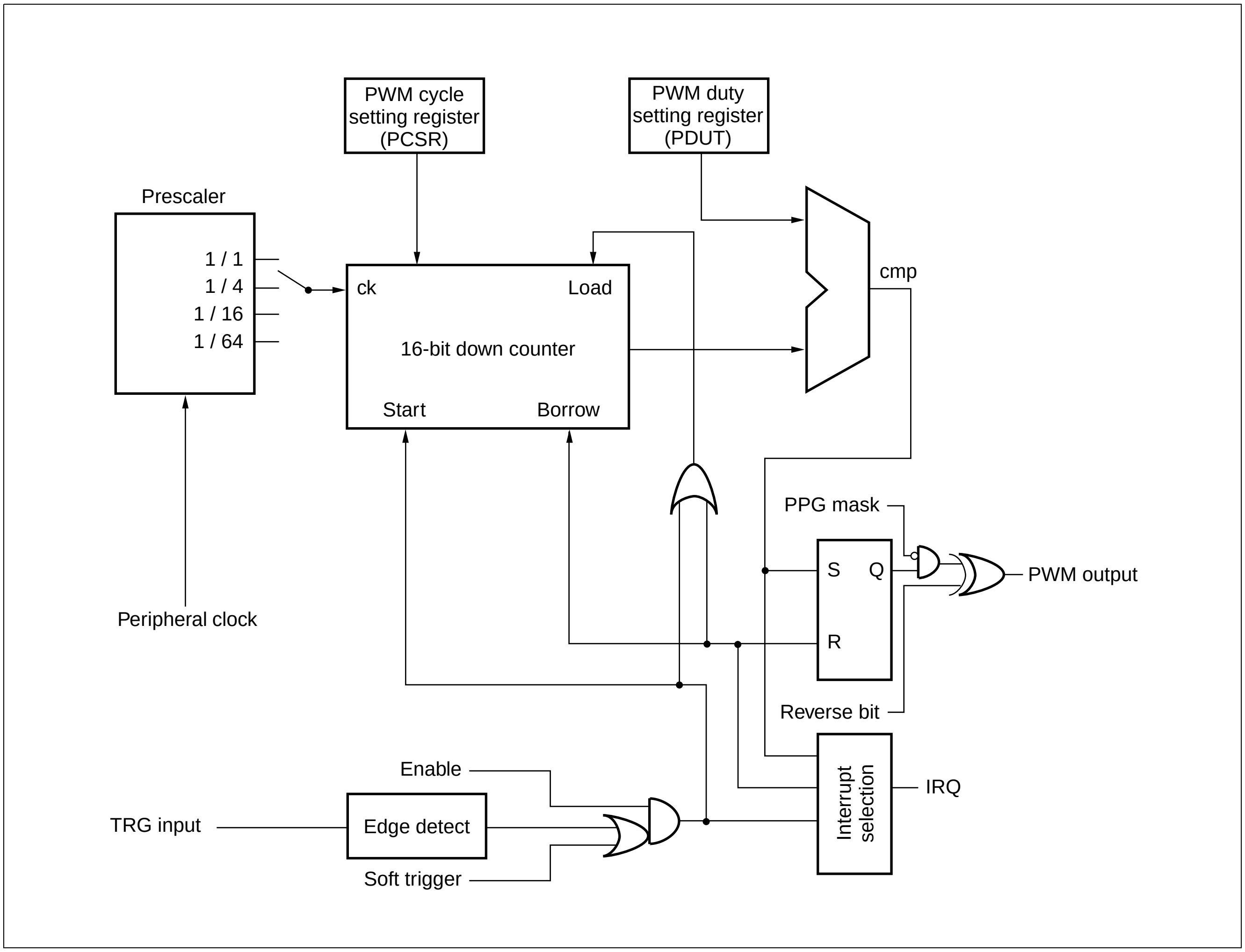
( ) : Access
R/W : Readable and writable
R : Read only
W : Write only
– : Unused
X : Indeterminate

(2) Block diagram

- **Block diagram (general construction)**



- **Block diagram (for one channel)**



6. 16-bit Reload Timer

The 16-bit reload timer consists of a 16-bit down counter, a 16-bit reload timer, a prescaler for generating internal count clock and control registers.

Internal clock can be selected from 3 types of internal clocks (divided by 2/8/32 of machine clock).

The DMA transfer can be started by the interruption.

The MB91F109 consists of 3 channels of the 16-bit reload timer.

(1) Register configuration

• 16-bit reload timer control status register 0 to 2

Address	bit 15 … bit 0	Initial value	
TMCSR0 : 00002EH	TMCSR0 to TMCSR2	- - - - 0 0 0 0 B	(R/W)
TMCSR1 : 000036H		0 0 0 0 0 0 0 0 B	
TMCSR2 : 000042H			

• 16-bit timer register 0 to 2

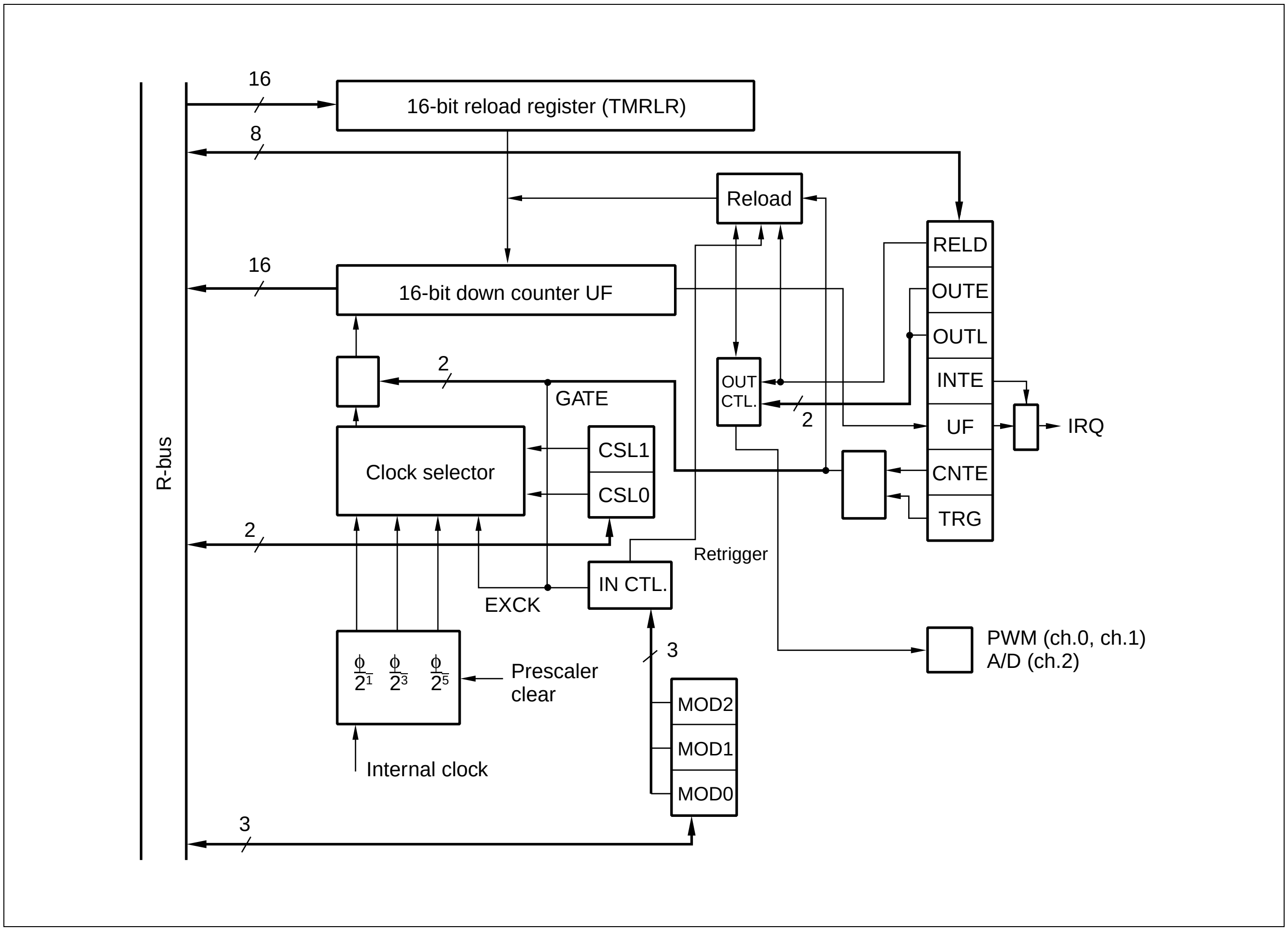
Address	bit 15 … bit 0	Initial value	
TMR0 : 00002AH	TMR0 to TMR2	X X X X X X X X B	(R)
TMR1 : 000032H		X X X X X X X X B	
TMR2 : 00003EH			

• 16-bit reload register 0 to 2

Address	bit 15 … bit 0	Initial value	
TMRLR0 : 000028H	TMRLR0 to TMRLR2	X X X X X X X X B	(W)
TMRLR1 : 000030H		X X X X X X X X B	
TMRLR2 : 00003CH			

( ) : Access
R/W : Readable and writable
R : Read Only
W : Write Only
– : Unused
X : Indeterminate

(2) Block diagram



7. Bit Search Module

The bit search module detects transitions of data (0 to 1/1 to 0) on the data written on the input registers and returns locations of the transitions.

(1) Register configuration

• Bit search module 0, 1-detection data register

Address	bit 31 … bit 0	Initial value	Access
BSD0 : 000003F0H BSD1 : 000003F4H	BSD0, BSD1	XXXXXXXXB XXXXXXXXB XXXXXXXXB XXXXXXXXB	(R/W)

• Bit search module transition-detection data register

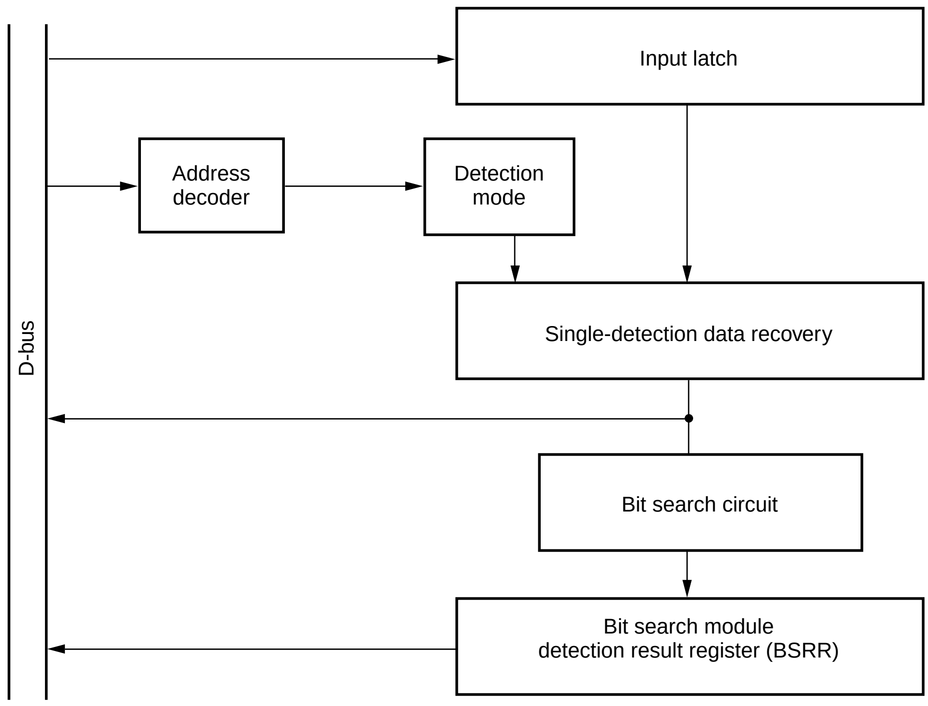
Address	bit 31 … bit 0	Initial value	Access
000003F8H	BSDC	XXXXXXXXB XXXXXXXXB XXXXXXXXB XXXXXXXXB	(W)

• Bit search module detection result register

Address	bit 31 … bit 0	Initial value	Access
000003FCH	BSRR	XXXXXXXXB XXXXXXXXB XXXXXXXXB XXXXXXXXB	(R)

( ) : Access
R/W : Readable and writable
R : Read only
W : Write only
X : Indeterminate

(2) Block diagram



8. 10-bit A/D Converter (Successive Approximation Conversion Type)

The A/D converter is the module which converts an analog input voltage to a digital value, and it has following features.

- Minimum converting time: 5.6 µs/ch. (system clock: 25 MHz)
- Inner sample and hold circuit
- Resolution: 10 bits
- Analog input can be selected from 4 channels by program.
  - Single convert mode: 1 channel is selected and converted.
  - Scan convert mode: Converting continuous channels. Maximum 4 channels are programmable.
  - Continuous convert mode: Converting the specified channel repeatedly.
  - Stop convert mode: After converting one channel then stop and wait till next activation synchronizing at the beginning of conversion can be performed.
- DMA transfer operation is available by interruption.
- Operating factor can be selected from the software, the external trigger (falling edge), and 16-bit reload timer (rising edge).

(1) Register configuration

• A/D converter control status register

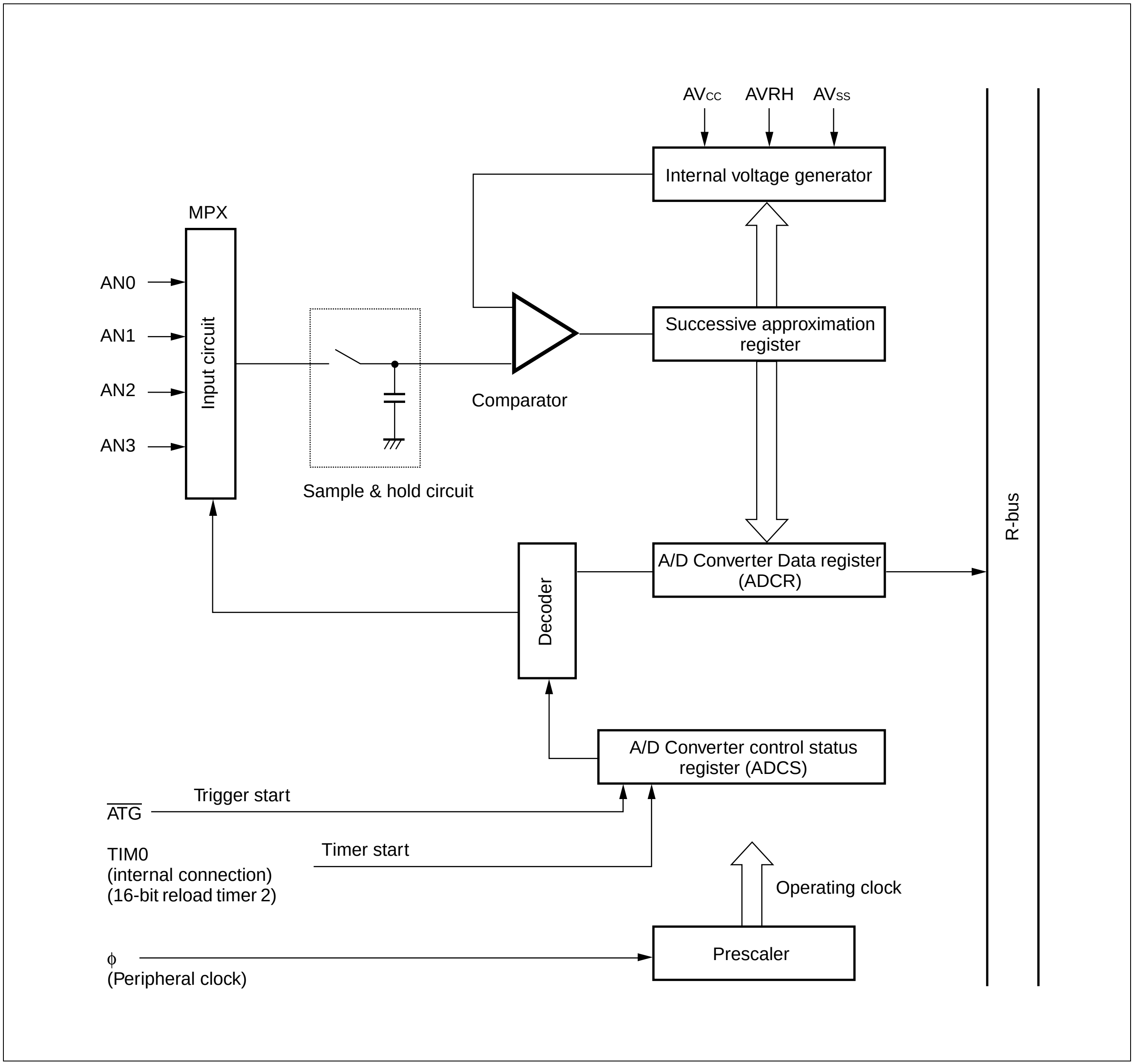
Address	bit 15 … bit 0	Initial value	
$0000003A_H$	ADCS	00000000_B 00000000_B	(R/W)

• A/D converter data register

Address	bit 15 … bit 0	Initial value	
00000038_H	ADCR	$000000XX_B$ $XXXXXXXX_B$	(R)

( ) : Access
R/W : Readable and writable
R : Read only
X : Indeterminate

(2) Block diagram



9. Interrupt Controller

The interrupt controller processes interrupt acknowledgments and arbitration between interrupts.

- Hardware Configuration
  Interrupt controller is configured by ICR resistor, interrupt priority decision circuit, interrupt level, vector generation and HLDREQ cancel request, and has the following functions.
- Main Functions
  NMI request/Interrupt request detection
  Priority (judgement) decision (via level and vector)
  Transfer of judged interrupt level to CPU
  Transfer of judged interrupt vector to CPU
  Return instruction from the stop mode via NMI/interrupt
  Generation of HOLD request cancel request to the bus timer

(1) Register configuration

• Interrupt control register 0 to 31, 47

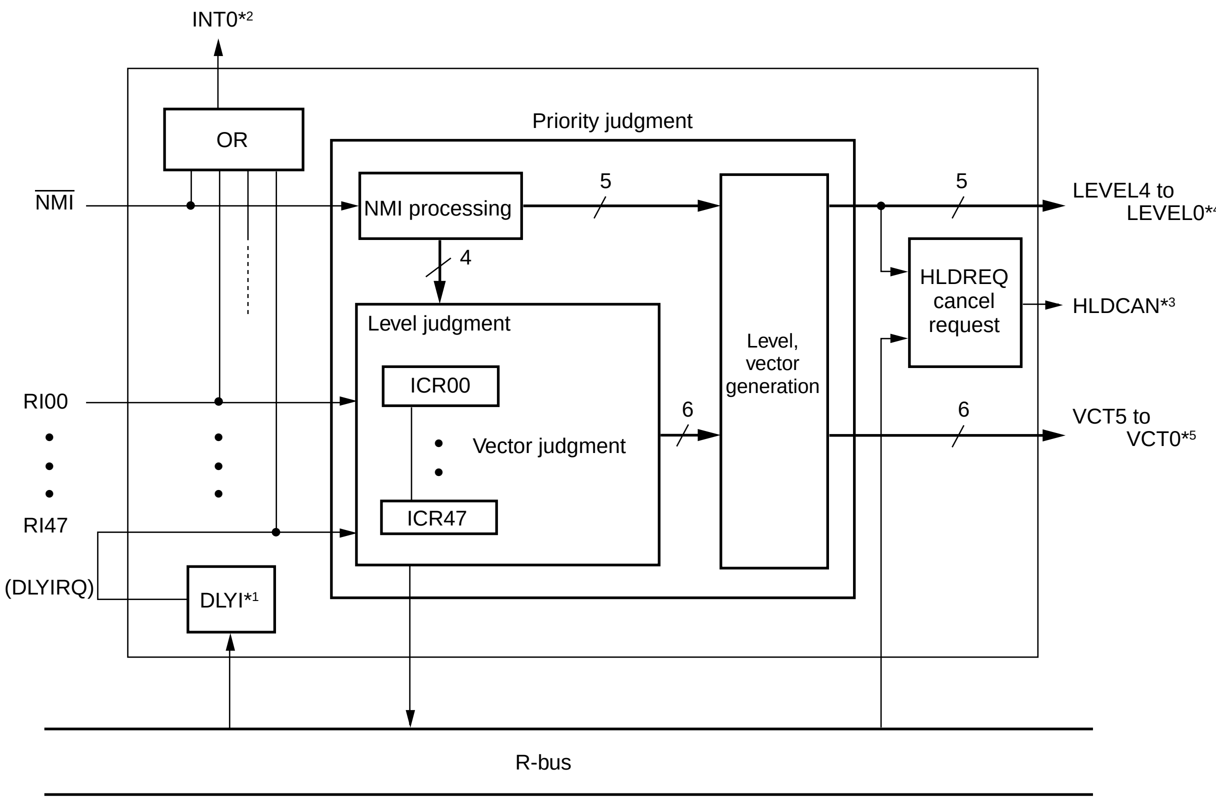
Address	bit 7 … bit 0	Initial value	Address	bit 7 … bit 0	Initial value
00000400_H	ICR00	- - - 11111 $_B$ (R/W)	00000411_H	ICR17	- - - 11111 $_B$ (R/W)
00000401_H	ICR01	- - - 11111 $_B$ (R/W)	00000412_H	ICR18	- - - 11111 $_B$ (R/W)
00000402_H	ICR02	- - - 11111 $_B$ (R/W)	00000413_H	ICR19	- - - 11111 $_B$ (R/W)
00000403_H	ICR03	- - - 11111 $_B$ (R/W)	00000414_H	ICR20	- - - 11111 $_B$ (R/W)
00000404_H	ICR04	- - - 11111 $_B$ (R/W)	00000415_H	ICR21	- - - 11111 $_B$ (R/W)
00000405_H	ICR05	- - - 11111 $_B$ (R/W)	00000416_H	ICR22	- - - 11111 $_B$ (R/W)
00000406_H	ICR06	- - - 11111 $_B$ (R/W)	00000417_H	ICR23	- - - 11111 $_B$ (R/W)
00000407_H	ICR07	- - - 11111 $_B$ (R/W)	00000418_H	ICR24	- - - 11111 $_B$ (R/W)
00000408_H	ICR08	- - - 11111 $_B$ (R/W)	00000419_H	ICR25	- - - 11111 $_B$ (R/W)
00000409_H	ICR09	- - - 11111 $_B$ (R/W)	$0000041A_H$	ICR26	- - - 11111 $_B$ (R/W)
$0000040A_H$	ICR10	- - - 11111 $_B$ (R/W)	$0000041B_H$	ICR27	- - - 11111 $_B$ (R/W)
$0000040B_H$	ICR11	- - - 11111 $_B$ (R/W)	$0000041C_H$	ICR28	- - - 11111 $_B$ (R/W)
$0000040C_H$	ICR12	- - - 11111 $_B$ (R/W)	$0000041D_H$	ICR29	- - - 11111 $_B$ (R/W)
$0000040D_H$	ICR13	- - - 11111 $_B$ (R/W)	$0000041E_H$	ICR30	- - - 11111 $_B$ (R/W)
$0000040E_H$	ICR14	- - - 11111 $_B$ (R/W)	$0000041F_H$	ICR31	- - - 11111 $_B$ (R/W)
$0000040F_H$	ICR15	- - - 11111 $_B$ (R/W)	$0000042F_H$	ICR47	- - - 11111 $_B$ (R/W)
00000410_H	ICR16	- - - 11111 $_B$ (R/W)			

• Hold request cancel request level setting register

Address	bit 7 … bit 0	Initial value
00000431_H	HRCL	- - - 1 1 1 1 1 $_B$ (R/W)

( ) : Access
R/W : Readable and writable
– : Unused

(2) Block diagram



*1: DLYI stands for delayed interrupt module (delayed interrupt generation block) (refer to the section “11. Delayed Interrupt Module” for detail).

*2: INT0 is a wake-up signal to clock control block in the sleep or stop status.

*3: HLDCAN is a bus release request signal for bus masters other than CPU.

*4: LEVEL4 to LEVEL0 are interrupt level outputs.

*5: VCT5 to VCT0 are interrupt vector outputs.

10. External Interrupt/NMI Control Block

The external interrupt/NMI control block controls external interrupt request signals input to $\overline{\text{NMI}}$ pin and INT0 to INT3 pins.

Detecting levels can be selected from “H”, “L”, rising edge and falling edge (not for $\overline{\text{NMI}}$ pin).

(1) Register configuration

- Interrupt enable register

Address	bit 15 … bit 8	bit 7 … bit 0	Initial value
00000095H	(EIRR)	ENIR	0 0 0 0 0 0 0 0 B (R/W)

- External interrupt cause register

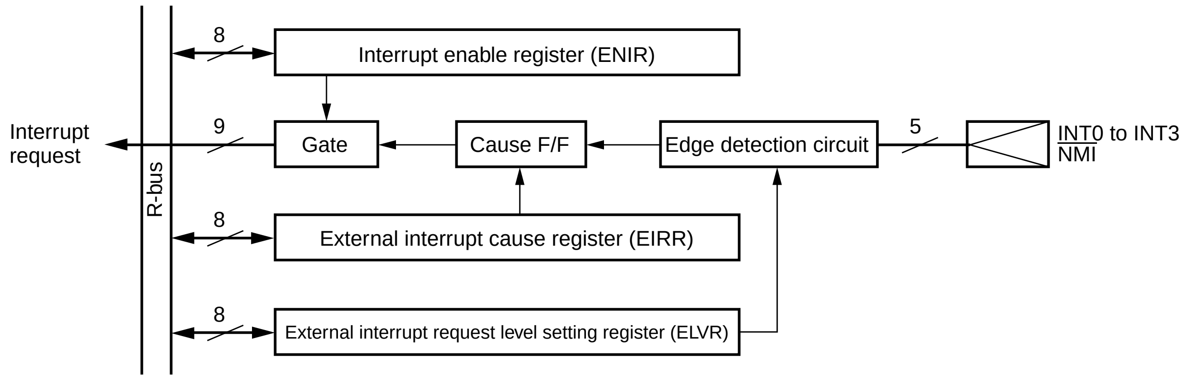
Address	bit 15 … bit 8	bit 7 … bit 0	Initial value
00000094H	EIRR	(ENIR)	0 0 0 0 0 0 0 0 B (R/W)

- External interrupt request level setting register

Address	bit 15 … bit 0	Initial value
00000099H	ELVR	0 0 0 0 0 0 0 0 B (R/W)

( ) : Access
R/W : Readable and writable

(2) Block diagram



11. Delayed Interrupt Module

Delayed interrupt module is a module which generates a interrupt for changing a task. By using this delayed interrupt module, an interrupt request to CPU can be generated/cancelled by the software.

Refer to the section “9. Interrupt Controller” for delayed interrupt module block diagram.

• Register configuration

• Delayed interrupt control register

Address	bit 7 … bit 0	Initial value
00000430_H	DICR	- - - - - - - 0 $_B$ (R/W)

( ) : Access
R/W : Readable and writable
– : Unused

12. Clock Generation (Low-power consumption mechanism)

The clock control block is a module which undertakes the following functions.

- CPU clock generation (including gear function)
- Peripheral clock generation (including gear function)
- Reset generation and cause hold
- Standby function
- DMA request prohibit
- PLL (multiplier circuit) embedded

(1) Register configuration

- Reset cause register/watchdog cycle control register

Address	bit 15 … bit 10	bit 9 … bit 8	bit 7 … bit 0	Initial value
00000480H	RSRR	WTCR	(STCR)	1 X X X X - 0 0 B (R/W)

- Standby control register

Address	bit 15 … bit 8	bit 7 … bit 0	Initial value
00000481H	(RSRR/WTCR)	STCR	0 0 0 1 1 1 - - B (R/W)

- DMA controller request squelch register

Address	bit 15 … bit 8	bit 7 … bit 0	Initial value
00000482H	PDRR	(CTBR)	- - - - 0 0 0 0 B (R/W)

- Timebase timer clear register

Address	bit 15 … bit 8	bit 7 … bit 0	Initial value
00000483H	(PDRR)	CTBR	X X X X X X X X B (W)

- Gear control register

Address	bit 15 … bit 8	bit 7 … bit 0	Initial value
00000484H	GCR	(WPR)	1 1 0 0 1 1 - 1 B (R/W)

- Watchdog reset occurrence postpone register

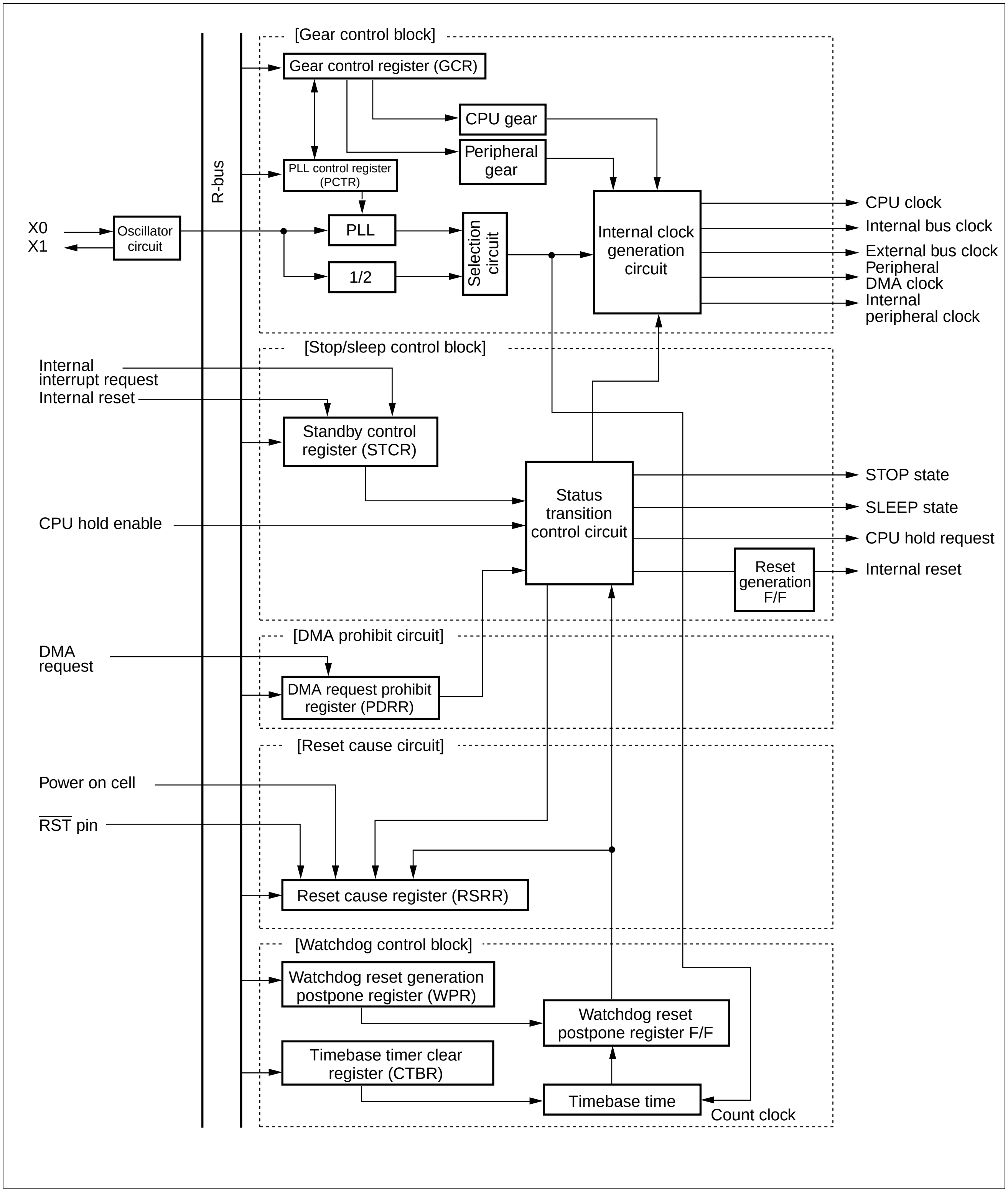
Address	bit 15 … bit 8	bit 7 … bit 0	Initial value
00000485H	(GCR)	WPR	X X X X X X X X B (W)

- PLL control register

Address	bit 15 … bit 8	bit 7 … bit 0	Initial value
00000488H	PCTR	(Vacancy)	0 0 - - 0 - - - B (R/W)

( ) : Access
R/W : Readable and writable
R : Read Only
W : Write Only
– : Unused
X : Indeterminate

(2) Block diagram



13. External Bus Interface

The external bus interface controls the interface between the device and the external memory and also the external I/O, and has the following features.

- 25-bit (32 Mbytes) address output
- 6 independent banks owing to the chip select function.
  Can be set to anywhere on the logical address space for minimum unit 64 Kbytes.
  Total 32 Mbytes × 6 area setting is available by the address pin and the chip select pin.
- 8/16-bit bus width setting are available for every chip select area.
- Programmable automatic memory wait (max. for 7 cycles) can be inserted.
- DRAM interface support
  Three kinds of DRAM interface: Double CAS DRAM (normally DRAM I/F)
  Single CAS DRAM
  Hyper DRAM
  2 banks independent control (RAS, CAS, etc. control signals)
  DRAM select is available from 2CAS/1WE and 1CAS/2WE.
  Hi-speed page mode supported
  CBR/self refresh supported
  Programmable wave form
- Unused address/data pin can be used for I/O port.
- Little endian mode supported
- Without Clock doubler: Internal bus 25 MHz, external bus 25 MHz (at source oscillation 12.5 MHz)

(1) Register configuration

- Area select register 1 to 5

Address	bit 15 … bit 0	Initial value	
0000060CH	ASR1	0 0 0 0 0 0 0 0 B 0 0 0 0 0 0 0 1 B	(W)
00000610H	ASR2	0 0 0 0 0 0 0 0 B 0 0 0 0 0 0 1 0 B	(W)
00000614H	ASR3	0 0 0 0 0 0 0 0 B 0 0 0 0 0 0 1 1 B	(W)
00000618H	ASR4	0 0 0 0 0 0 0 0 B 0 0 0 0 0 1 0 0 B	(W)
0000061CH	ASR5	0 0 0 0 0 0 0 0 B 0 0 0 0 0 1 0 1 B	(W)

- Area mask register 1 to 5

Address	bit 15 … bit 0	Initial value	
AMR1 : 0000060EH AMR2 : 00000612H AMR3 : 00000616H AMR4 : 0000061AH AMR5 : 0000061EH	AMR1 to AMR5	0 0 0 0 0 0 0 0 B 0 0 0 0 0 0 0 0 B	(W)

- Area mode register 0, 1, 32, 4, 5

Address	bit 15 … bit 8	bit 7 … bit 0	Initial value	
AMD0 : 00000620H AMD1 : 00000621H	AMD0	AMD1	- - - 0 0 1 1 1 B 0 - - 0 0 0 0 0 B	(R/W)
AMD32 : 00000622H AMD4 : 00000623H	AMD32	AMD4	0 0 0 0 0 0 0 0 B 0 - - 0 0 0 0 0 B	(R/W)
AMD5 : 00000624H	AMD5	(DSCR)	0 - - 0 0 0 0 0 B	(R/W)

- DRAM single control register

Address	bit 15 … bit 8	bit 7 … bit 0	Initial value	
00000625H	(AMD5)	DSCR	0 0 0 0 0 0 0 0 B	(W)

- Refresh control register

Address	bit 15 … bit 0	Initial value	
00000626H	RFCR	- - X X X X X X B 0 0 - - - 0 0 0 B	(R/W)

- External pin control register 0, 1

Address	bit 15 … bit 0	Initial value	
EPCR0: 00000628H	EPCR0	- - - - 1 1 0 0 B - 1 1 1 1 1 1 1 B	(W)
EPCR1: 0000062AH	EPCR1	- - - - - - - 1 B 1 1 1 1 1 1 1 1 B	(W)

- DRAM control register 4, 5

Address	bit 15 … bit 0	Initial value	
DMCR4: 0000062CH DMCR5: 0000062EH	DMCR4, DMCR5	0 0 0 0 0 0 0 0 B 0 0 0 0 0 0 0 - B	(R/W)

- Litter endian register

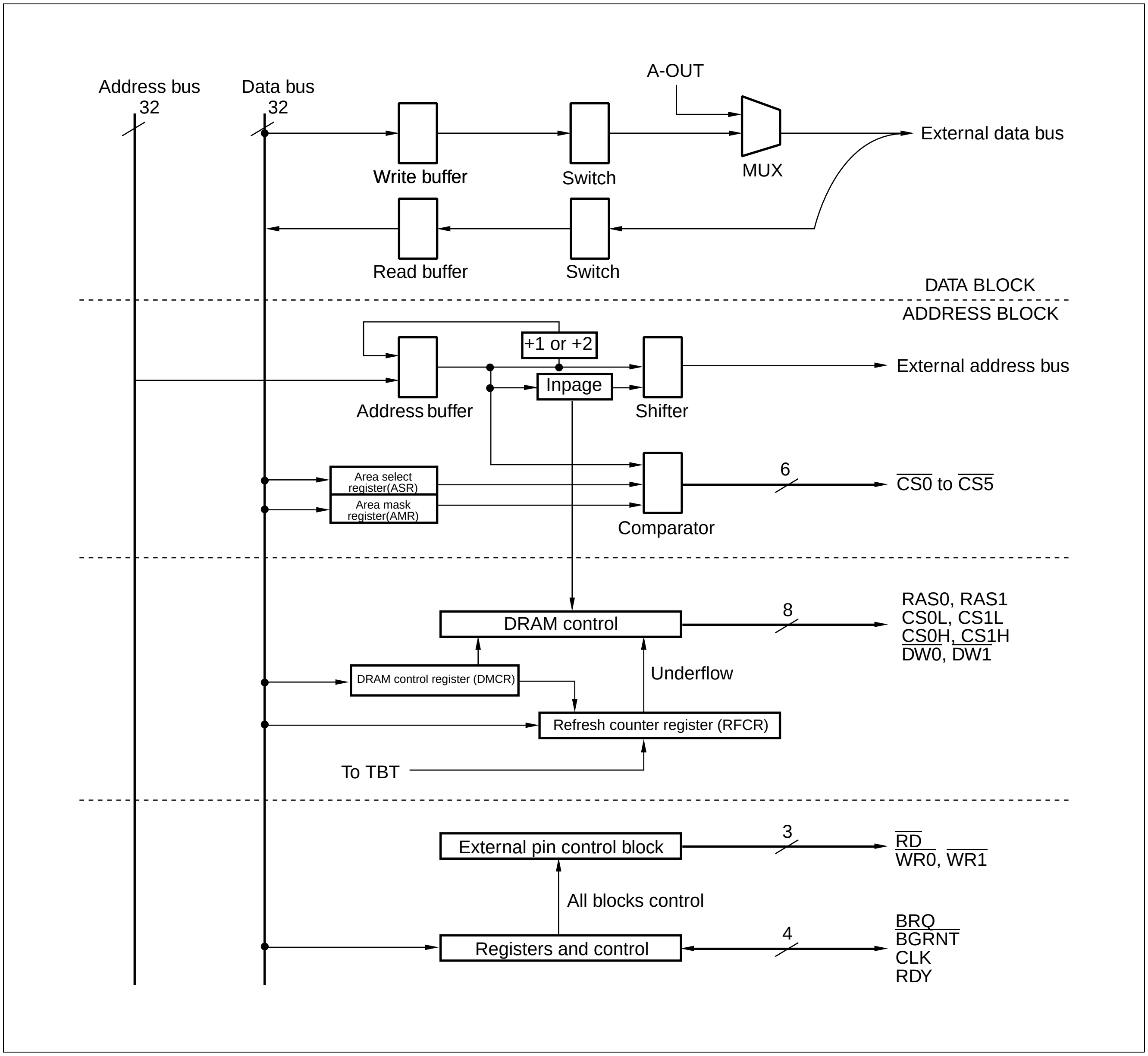
Address	bit 15 … bit 8	bit 7 … bit 0	Initial value	
000007FEH	LER	(MODR)	- - - - - 0 0 0 B	(W)

- Mode register

Address	bit 15 … bit 8	bit 7 … bit 0	Initial value	
000007FFH	(LER)	MODR	X X X X X X X X B	(W)

( ) : Access
R/W : Readable and writable
W : Write only
– : Unused
X : Indeterminate

(2) Block diagram



■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

($V_{SS} = AV_{SS} = 0.0$ V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	$V_{SS} – 0.3$	$V_{SS} + 4.0$	V	*1
Analog supply voltage	AV_{CC}	$V_{SS} – 0.3$	$V_{SS} + 4.0$	V	*2
Analog reference voltage	AVRH	$V_{SS} – 0.3$	$V_{SS} + 4.0$	V	*2
Analog pin input voltage	V_{IA}	$V_{SS} – 0.3$	$AV_{CC} + 0.3$	V	
Input voltage	V_I	$V_{SS} – 0.3$	$V_{CC} + 0.3$	V	
Output voltage	V_O	$V_{SS} – 0.3$	$V_{CC} + 0.3$	V	
“L” level maximum output current	I_{OL}	—	10	mA	*3
“L” level average output current	I_{OLAV}	—	8	mA	*4
“L” level maximum total output current	ΣI_{OL}	—	100	mA	
“L” level average total output current	ΣI_{OLAV}	—	50	mA	*5
“H” level maximum output current	I_{OH}	—	–10	mA	*3
“H” level average output current	I_{OHAV}	—	–4	mA	*4
“H” level maximum total output current	ΣI_{OH}	—	–50	mA	
“H” level average total output current	ΣI_{OHAV}	—	–20	mA	*5
Power consumption	P_D	—	500	mW	
Operating temperature	T_A	0	+70	°C	
Storage temperature	Tstg	–55	+150	°C	

*1: V_{CC} must not be less than V_{SS} – 0.3 V.
*2: Make sure that the voltage does not exceed V_{CC} + 0.3 V, such as when turning on the device.
*3: Maximum output current is a peak current value measured at a corresponding pin.
*4: Average output current is an average current for a 100 ms period at a corresponding pin.
*5: Average total output current is an average current for a 100 ms period for all corresponding pins.

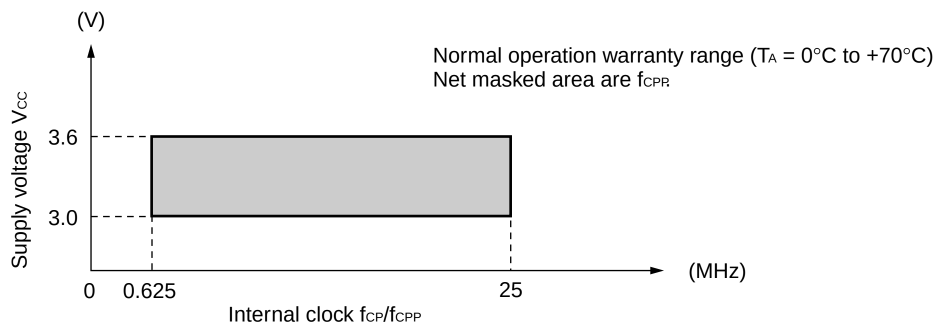
WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

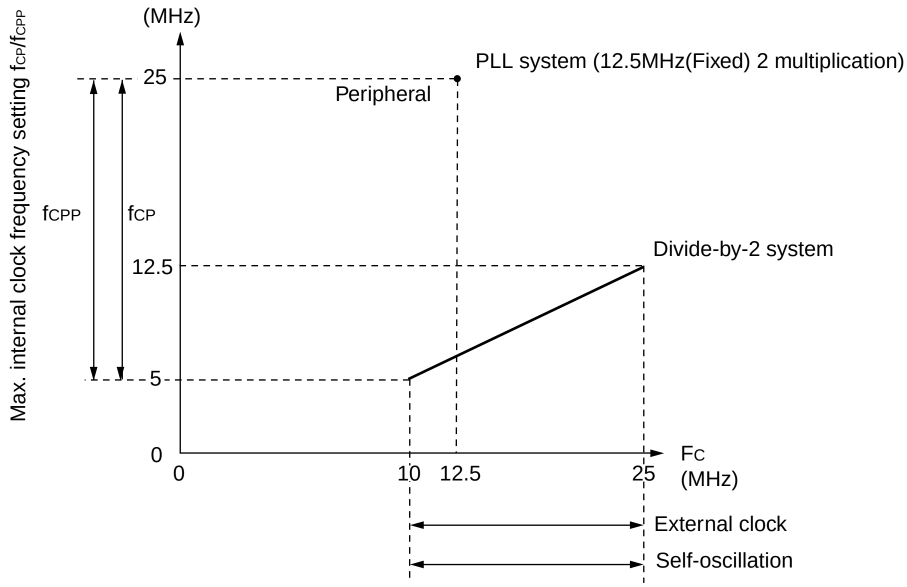
($V_{SS} = AV_{SS} = 0.0$ V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	3.15	3.6	V	Normal operation
	V_{CC}	3.15	3.6	V	Retaining the RAM state in stop mode
Analog supply voltage	AV_{CC}	V_{SS} – 0.3	V_{SS} + 3.6	V	
Analog reference voltage	AVRH	AV_{SS}	AV_{CC}	V	
Operating temperature	T_A	0	+70	°C	

- **Normal operation warranty rage**



- **External/Internal clock setting rage**



Notes:
- When using PLL, the external clock must be used need 12.5 MHz.
- PLL oscillation stabilizing period > 100 µs
- The setting of internal clock must be within above ranges.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

(V_{CC} = 3.15 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level input voltage	V_{IH}	Input pin except for hysteresis input	—	$0.65 \times V_{CC}$	—	$V_{CC} + 0.3$	V	
	V_{IHS}	$\overline{\text{NMI}}$, $\overline{\text{RST}}$, P40 to P47, P50 to P57, P60 to P67, P70, P81, P83 to P85, PA0 to PA6, PB0 to PB7, PE0 to PE7, PF0 to PF7	—	$0.8 \times V_{CC}$	—	$V_{CC} + 0.3$	V	Hysteresis input
"L" level input voltage	V_{IL}	Input other than following symbols	—	$V_{SS} - 0.3$	—	$0.25 \times V_{CC}$	V	
	V_{ILS}	$\overline{\text{NMI}}$, $\overline{\text{RST}}$, P40 to P47, P50 to P57, P60 to P67, P70, P81, P83 to P85, PA0 to PA6, PB0 to PB7, PE0 to PE7, PF0 to PF7	—	$V_{SS} - 0.3$	—	$0.2 \times V_{CC}$	V	Hysteresis input
"H" level output voltage	V_{OH}	P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70, P80 to P85, PA0 to PA6, PB0 to PB7, PE0 to PE7, PF0 to PF7	V_{CC} = 3.15 V, I_{OH} = –4.0 mA	$V_{CC} - 0.5$	—	—	V	
"L" level output voltage	V_{OL}		V_{CC} = 3.15 V, I_{OL} = 4.0 mA	—	—	0.4	V	
Input leakage current (Hi-Z output leakage current)	I_{LI}		V_{CC} = 3.6 V, 0.45 V < V_I < V_{CC}	–5	—	+5	µA	
Pull-up resistance	R_{PULL}	$\overline{\text{RST}}$	V_{CC} = 3.6 V, V_I = 0.45 V	25	50	100	kΩ	
Power supply current	I_{CC}	V_{CC}	F_C = 12.5 MHz, V_{CC} = 3.3 V	—	75	100	mA	(2 multiplication) Operation at 25 MHz
	I_{CCS}	V_{CC}	F_C = 12.5 MHz, V_{CC} = 3.3 V	—	35	50	mA	Sleep mode
	I_{CCH}	V_{CC}	T_A = +25°C, V_{CC} = 3.3 V	—	1.4	150	µA	Stop mode
Input capacitance	C_{IN}	Except for V_{CC}, AV_{CC}, AV_{SS}, V_{SS}	—	—	10	—	pF	

4. FLASH Memory Programming/Erasing Characteristics

(V_{CC} = 3.15 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)

Parameter	Condition	Value			Unit	Remarks
		Min.	Typ.	Max.		
Sector erasing time	T_A = +25°C V_{CC} = 3.3 V	—	1.5	13.5	s	Except for the write time before internal erase operation
Chip erasing time		—	—	27.0	s	Except for the write time before internal erase operation
Byte programming time		—	16	—	µs	Except for the over head time of the system
Chip programming time		—	2.1	—	s	Except for the over head time of the system
Erase/Program cycle	—	100	—	—	cycle	

Note: The internal automatic algorithm continues operations for up to 48 ms, for each 1-byte writing operation.

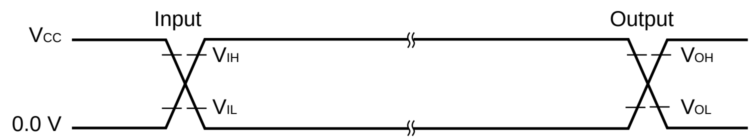
5. AC Characteristics

(1) Measurement Conditions

(V_{CC} = 3.15 V to 3.6 V)

Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
"H" level input voltage	V_{IH}	—	1/2* × V_{CC}	—	V	
"L" level input voltage	V_{IL}	—	1/2* × V_{CC}	—	V	
"H" level output voltage	V_{OH}	—	1/2* × V_{CC}	—	V	
"L" level output voltage	V_{OL}	—	1/2* × V_{CC}	—	V	

*: Input rise/fall time is 10 ns. and less.



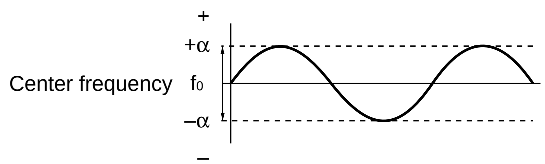
(2) Clock Timing Rating

(V_{CC} = 3.15 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Clock frequency	F_C	X0, X1	Self-oscillation at 12.5 MHz Internal operation at 25 MHz (Via PLL, double)	12.5	12.5	MHz	
	F_C	X0, X1	Self-oscillation (divide-by-2 input)	10	25	MHz	
	F_C	X0, X1	External clock (divide-by-2 input)	10	25	MHz	
Clock cycle time	t_C	X0, X1	Self-oscillation at 12.5 MHz Internal operation at 25 MHz (Via PLL, double)	—	80	ns	
	t_C	X0, X1	—	40	100	ns	
Frequency shift ratio (when locked)	Δf	—	Self-oscillation at 12.5 MHz Internal operation at 25 MHz (Via PLL, double)	—	5	%	*1
Input clock pulse width	P_{WH}, P_{WL}	X0, X1	12.5 MHz to 25.0 MHz	18.5	—	ns	Input clock pulse to X0 and X1
	P_{WH}	X0	12.5 MHz and less	25	—	ns	Input clock pulse to X0 only
Input clock rising/falling time	t_{CR}, t_{CF}	X0, X1	—	—	8	ns	(t_{CR} + t_{CF})
Internal operating clock frequency	f_{CP}	—	CPU system	0.625*2	25	MHz	
	f_{CPP}	—	Peripheral system	0.625*2	25	MHz	
Internal operating clock cycle time	t_{CP}	—	CPU system	40	1600*2	ns	
	t_{CPP}	—	Peripheral system	40	1600*2	ns	

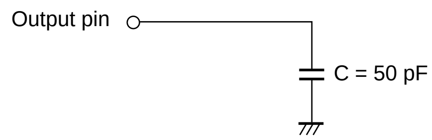
*1: Frequency shift ratio stands for deviation ratio of the operating clock from the center frequency in the clock multiplication system.

$$\Delta f = \frac{|\alpha|}{f_0} \times 100\ (\%)$$

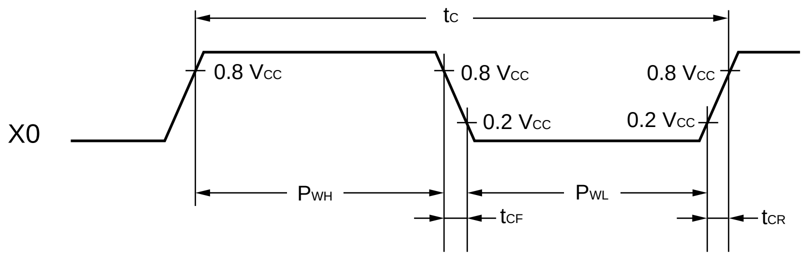


*2: These values are for a minimum clock of 10 MHz input to X0, a divide-by-2 system of the source oscillation and a 1/8 gear.

• **Load conditions**



• **Clock timing rating measurement conditions**



(3) Clock Output Timing

(V_{CC} = 3.15 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)

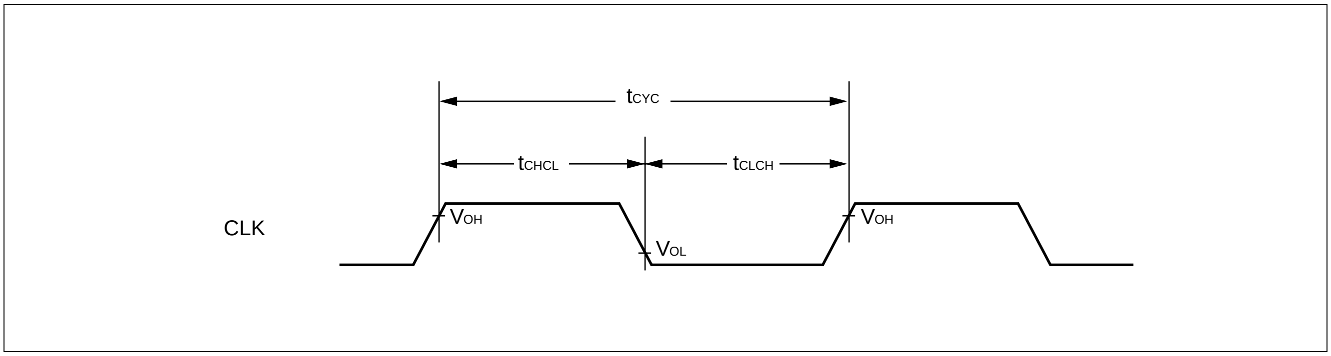
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Cycle time	t_{CYC}	CLK	—	t_{CP}*1	—	ns	*2
CLK ↑ → CLK ↓	t_{CHCL}	CLK	—	$1/2 \times t_{CYC} - 5$	$1/2 \times t_{CYC} + 5$	ns	*3
CLK ↓ → CLK ↑	t_{CLCH}	CLK		$1/2 \times t_{CYC} - 5$	$1/2 \times t_{CYC} + 5$	ns	*4

*1: For information on t_{CP} (internal operating clock cycle time), see “(2) Clock Timing Rating.”

*2: t_{CYC} is a frequency for 1 clock cycle including a gear cycle.

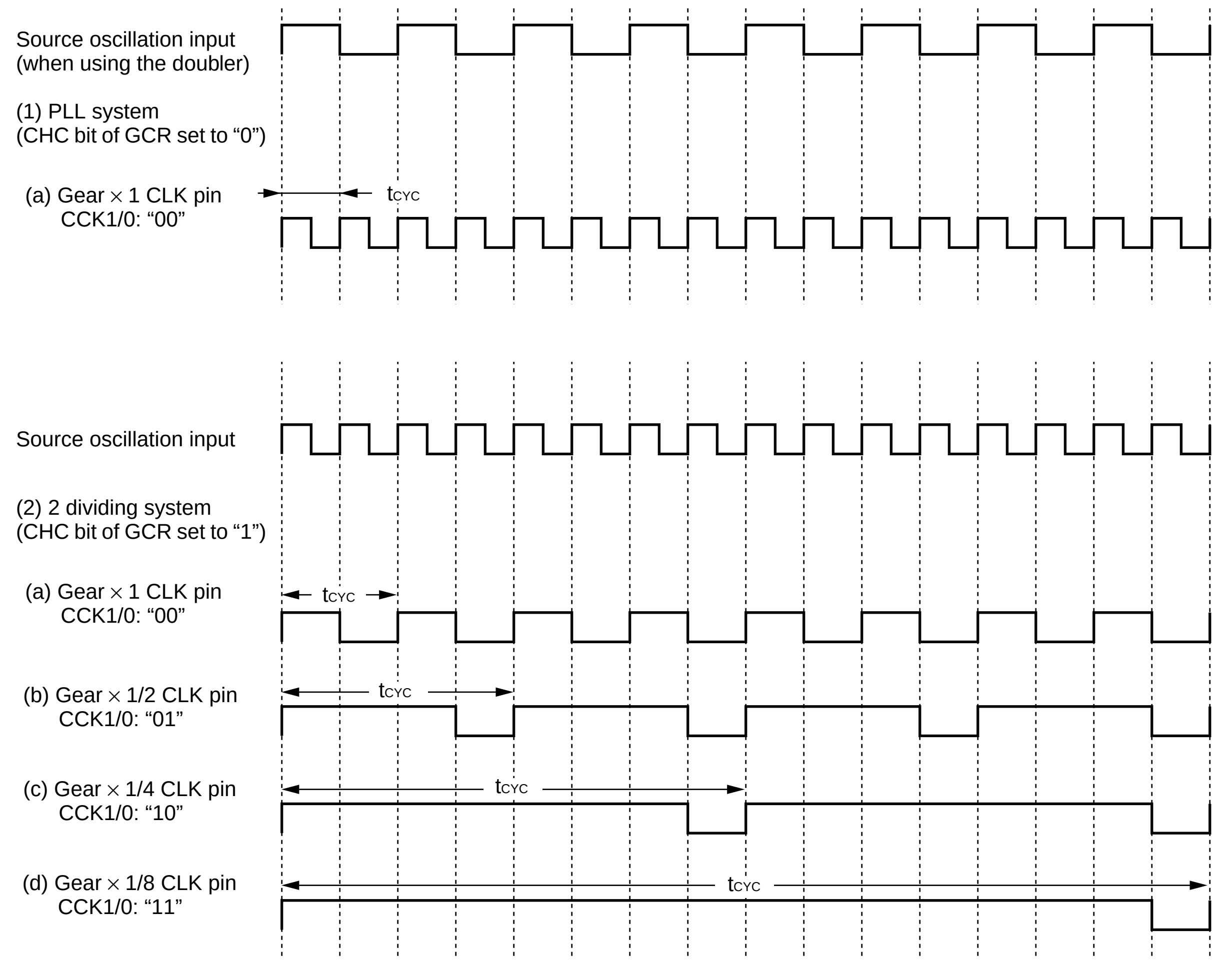
*3: Rating at a gear cycle of × 1.
When a gear cycle of 1/2, 1/4, 1/8 is selected, substitute “n” in the following equations with 1/2, 1/4, 1/8, respectively.
Min. : $(1 - n/2) \times t_{CYC} - 10$
Max. : $(1 - n/2) \times t_{CYC} + 10$

*4: Rating at a gear cycle of × 1.
When a gear cycle of 1/2, 1/4, 1/8 is selected, substitute “n” in the following equations with 1/2, 1/4, 1/8, respectively.
Min. : $n/2 \times t_{CYC} - 10$
Max. : $n/2 \times t_{CYC} + 10$

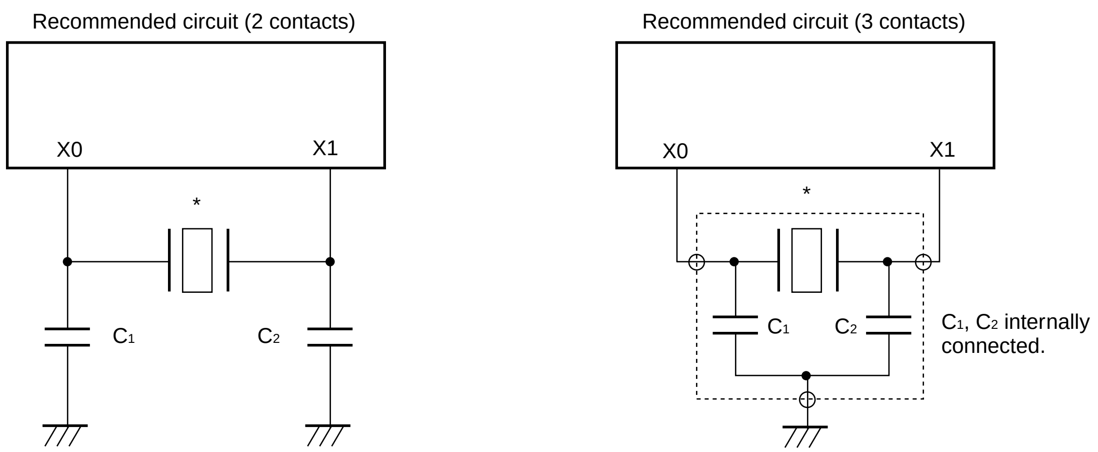


The relation between source oscillation input and CLK pin for configured by CHC/CCK1/CCK0 settings of GCR (gear control register) is as follows:

However, in this chart source oscillation input means X0 input clock.



- **Ceramic oscillator applications**



*: Murata Mfg. Co., Ltd.

- **Discreet type**

Oscillation frequency [MHz]	Model	Load capacitance $C_1 = C_2$ [pF]	Power supply voltage V_{CC} [V]
5.00 to 6.30	CSA□□□MG	30	3.15 to 3.6
	CST□□□MGW	(30)	
	CSA□□□MG093	30	3.15 to 3.6
	CST□□□MGW093	(30)	
6.31 to 10.0	CSA□□□MTZ	30	3.15 to 3.6
	CST□□□MTW	(30)	
	CSA□□□MTZ093	30	3.15 to 3.6
	CST□□□MTW093	(30)	
10.1 to 13.0	CSA□□□MTZ	30	3.15 to 3.6
	CST□□□MTW	(30)	
	CSA□□□MTZ093	30	3.15 to 3.6
	CST□□□MTW093	(30)	
13.01 to 15.00	CSA□□□□MXZ040	15	3.2 to 3.6
	CST□□□□MXW0C3	(15)	

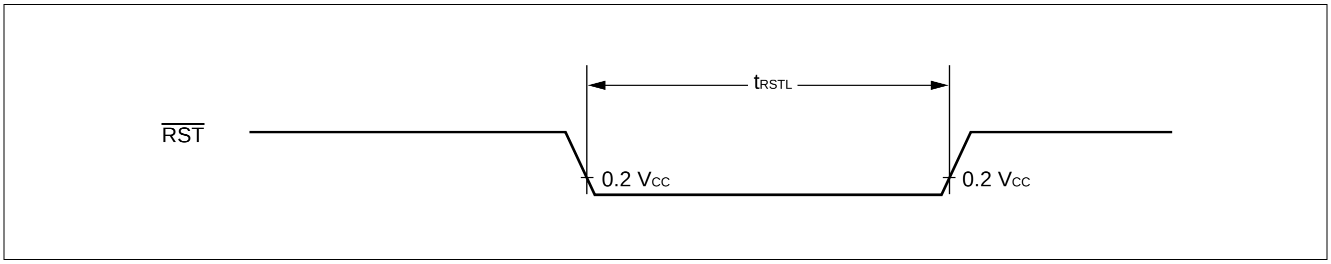
( ): C_1 and C_2 internally connected 3 contacts type.

(4) Reset Input Ratings

(V_{CC} = 3.15 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Reset input time	t_{RSTL}	$\overline{RST}$	—	t_{CP}* × 5	—	ns	

*: For information on t_{CP} (internal operating clock cycle time), see "(2) Clock Timing Rating."

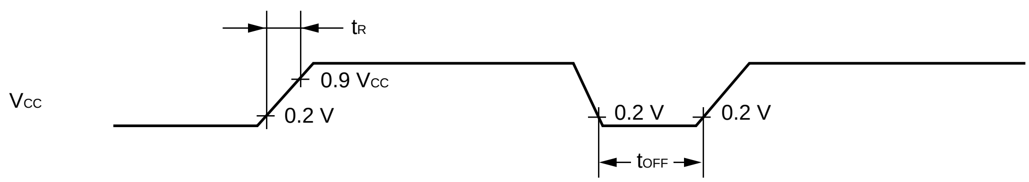


(5) Power on Supply Specifications (Power-on Reset)

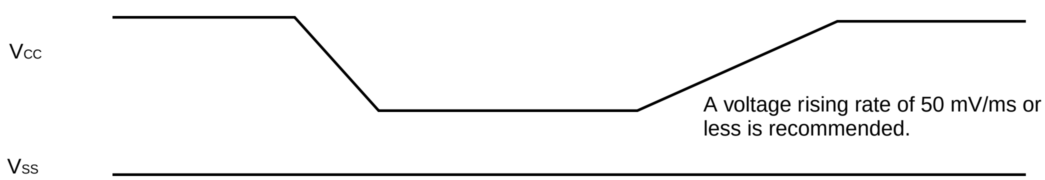
($AV_{CC} = V_{CC} = 3.15$ V to 3.6 V, $V_{SS} = AV_{SS} = 0.0$ V, $T_A = 0$°C to +70°C)

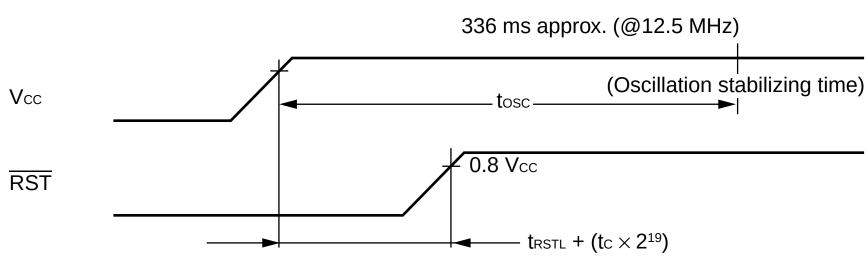
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Power supply rising time	t_R	V_{CC}	$V_{CC} = 3.3$ V	—	18	ms	$V_{CC} < 0.2$ V before the power supply rising
Power supply shut off time	t_{OFF}	V_{CC}	—	1	—	ms	Repeated operations
Oscillation stabilizing time	t_{OSC}	—		$2 \times t_C^* \times 2^{20}$ + 100 µs	—	ns	

*: For information on t_C (clock cycle time), see "(2) Clock Timing Rating."



Note: Sudden change in supply voltage during operation may initiate a power-on sequence.
To change supply voltage during operation, it is recommended to smoothly raise the voltage to avoid rapid fluctuations in the supply voltage.





t_{RSTL}: Reset input time

Notes:
- Set $\overline{RST}$ pin to "L" level when turning on the device, at least the described above duration after the supply voltage reaches Vcc is necessary before turning the $\overline{RST}$ to "H" level.
- Some internal resistors which are initialized only via power on reset are embedded in the device. To initialize these resistors, run power on reset by returning on the power supply.

(6) Normal Bus Access Read/write Operation

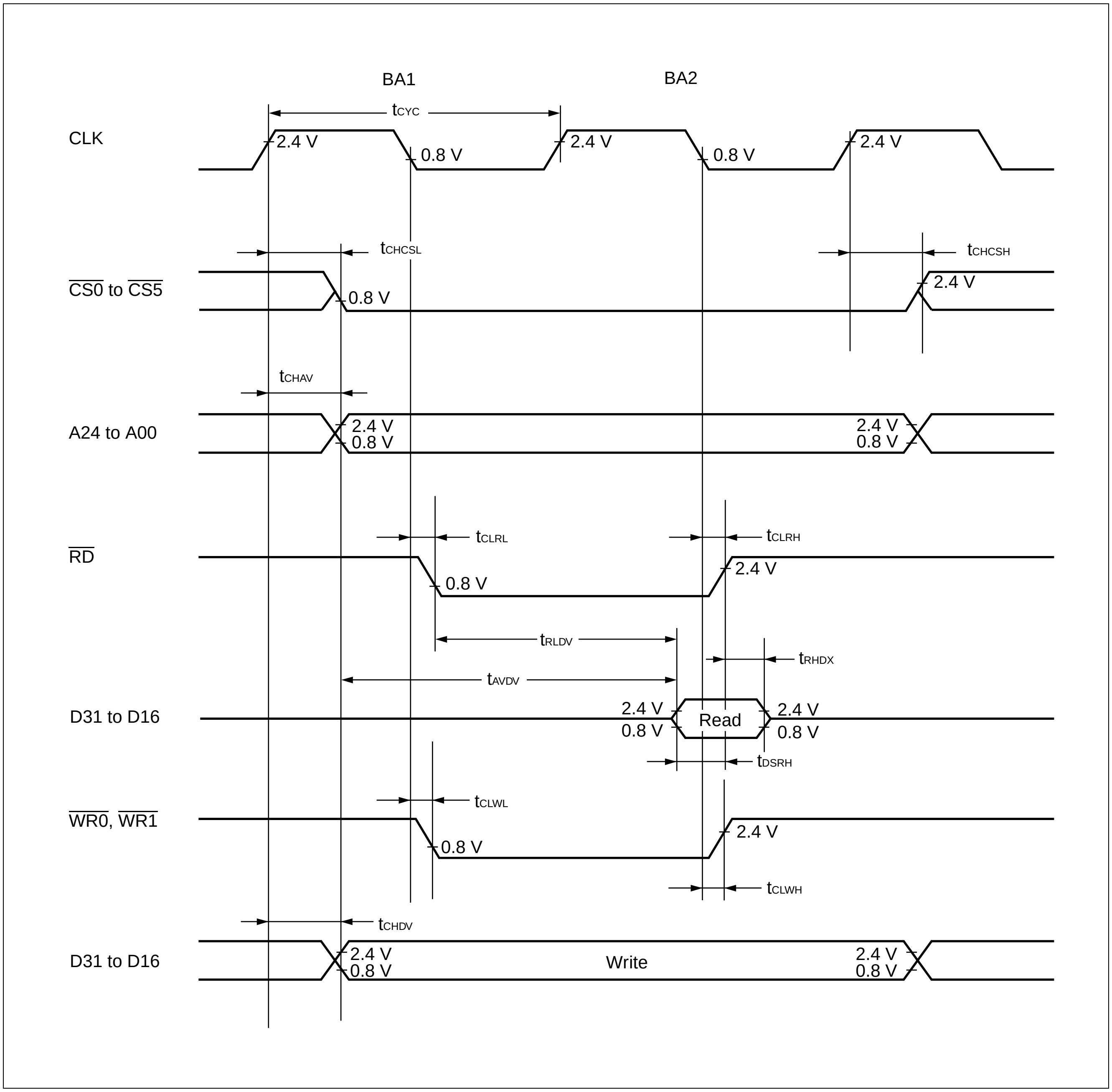
($AV_{CC} = V_{CC} = 3.15$ V to 3.6 V, $V_{SS} = AV_{SS} = 0.0$ V, $T_A = 0°C$ to $+70°C$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
$\overline{CS0}$ to $\overline{CS5}$ delay time	t_{CHCSL}	CLK, $\overline{CS0}$ to $\overline{CS5}$	—	—	15	ns	
	t_{CHCSH}	CLK, $\overline{CS0}$ to $\overline{CS5}$		—	15	ns	
Address delay time	t_{CHAV}	CLK, A24 to A00		—	15	ns	
Data delay time	t_{CHDV}	CLK, D31 to D16		—	15	ns	
$\overline{RD}$ delay time	t_{CLRL}	CLK, $\overline{RD}$		—	15	ns	
	t_{CLRH}	CLK, $\overline{RD}$		—	15	ns	
$\overline{WR0}$, $\overline{WR1}$ delay time	t_{CLWL}	CLK, $\overline{WR0}$, $\overline{WR1}$		—	15	ns	
	t_{CLWH}	CLK, $\overline{WR0}$, $\overline{WR1}$		—	15	ns	
Valid address → valid data input time	t_{AVDV}	A24 to A00, D31 to D16		—	$3/2 \times t_{CYC}$*1 – 25	ns	*2 *3
$\overline{RD}$ ↓→ valid data input time	t_{RLDV}	$\overline{RD}$, D31 to D16		—	t_{CYC}*1 – 10	ns	*2
Data set up → $\overline{RD}$ ↑ time	t_{DSRH}	$\overline{RD}$, D31 to D16		10	—	ns	
$\overline{RD}$ ↑→ data hold time	t_{RHDX}	$\overline{RD}$, D31 to D16		10	—	ns	

*1: For information on t_{CYC} (a cycle time of peripheral system clock), see “(3) Clock Output Timing.”

*2: When bus timing is delayed by automatic wait insertion or RDY input, add (t_{CYC} × extended cycle number for delay) to this rating.

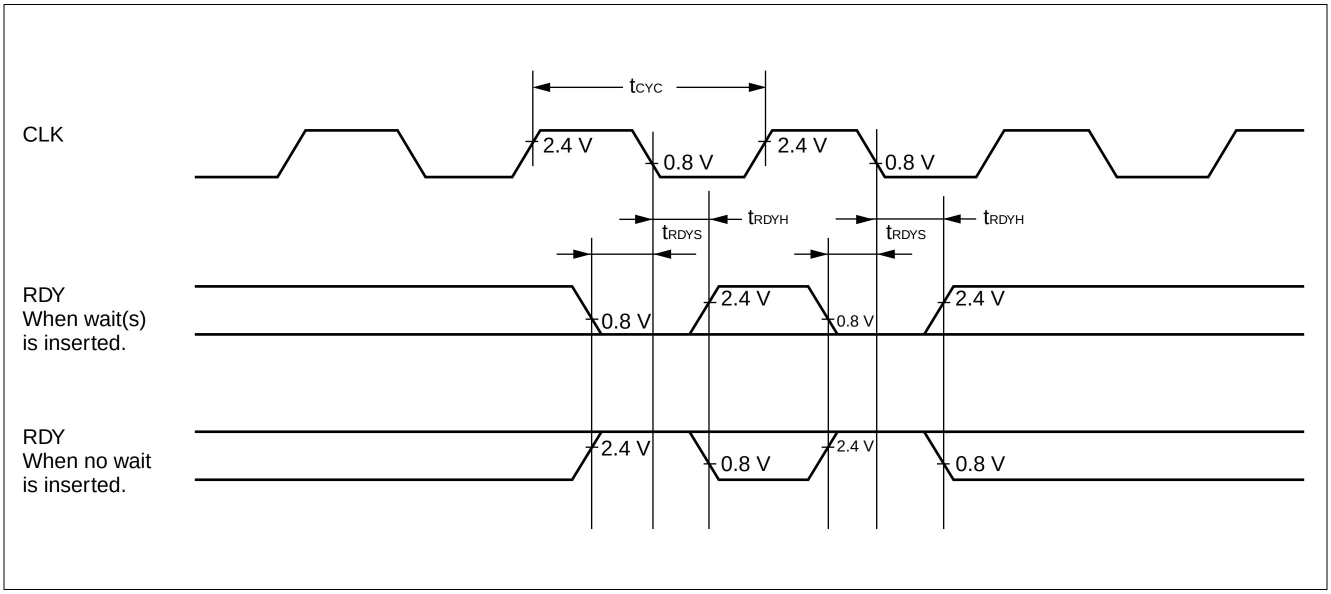
*3: Rating at a gear cycle of × 1.
When a gear cycle of 1/2, 1/4, 1/8 is selected, substitute “n” in the following equation with 1/2, 1/4, 1/8, respectively.
Equation: $(2 – n/2) \times t_{CYC} – 25$


BA1
BA2
CLK
tCYC
2.4 V
0.8 V
CS0 to CS5
tCHCSL
tCHCSH
A24 to A00
tCHAV
RD
tCLRL
tCLRH
tRLDV
tRHDX
tAVDV
D31 to D16
Read
tDSRH
WR0, WR1
tCLWL
tCLWH
tCHDV
Write

(7) Ready Input Timing

(V_{CC} = 3.15 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
RDY set up time → CLK ↓	t_{RDYS}	RDY, CLK	—	15	—	ns	
CLK ↓→ RDY hold time	t_{RDYH}	CLK, RDY		0	—	ns	



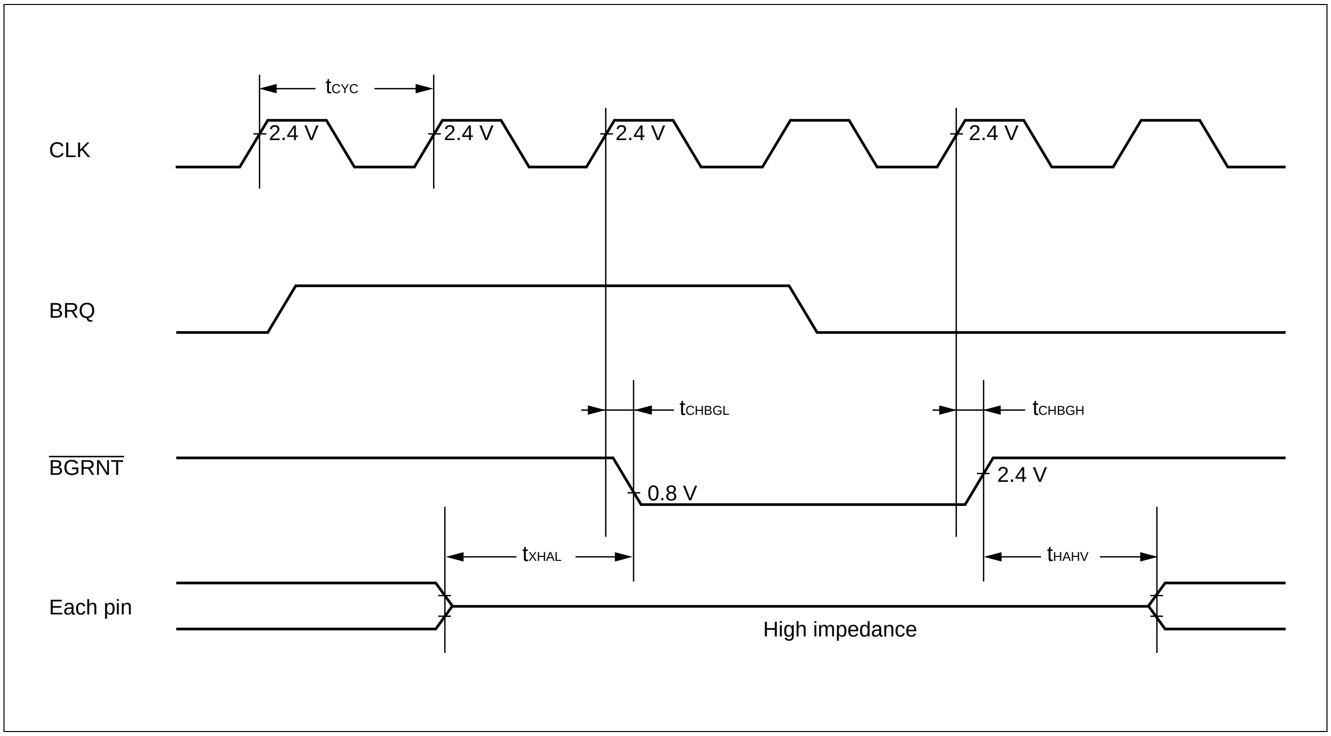
(8) Hold Timing

(V_{CC} = 3.15 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
$\overline{\text{BGRNT}}$ delay time	t_{CHBGL}	CLK, $\overline{\text{BGRNT}}$	—	—	6	ns	
	t_{CHBGH}	CLK, $\overline{\text{BGRNT}}$		—	6	ns	
Pin floating → $\overline{\text{BGRNT}}$ ↓ time	t_{XHAL}	$\overline{\text{BGRNT}}$		t_{CYC}* – 10	t_{CYC}* + 10	ns	
$\overline{\text{BGRNT}}$ ↑→ pin valid time	t_{HAHV}	$\overline{\text{BGRNT}}$		t_{CYC}* – 10	t_{CYC}* + 10	ns	

*: For information on t_{CYC} (a cycle time of peripheral system clock), see “(3) Clock Output Timing.”

Note: There is a delay time of more than 1 cycle from BRQ input to $\overline{\text{BGRNT}}$ change.



(9) Normal DRAM Mode Read/Write Cycle

(V_{CC} = 3.15 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)

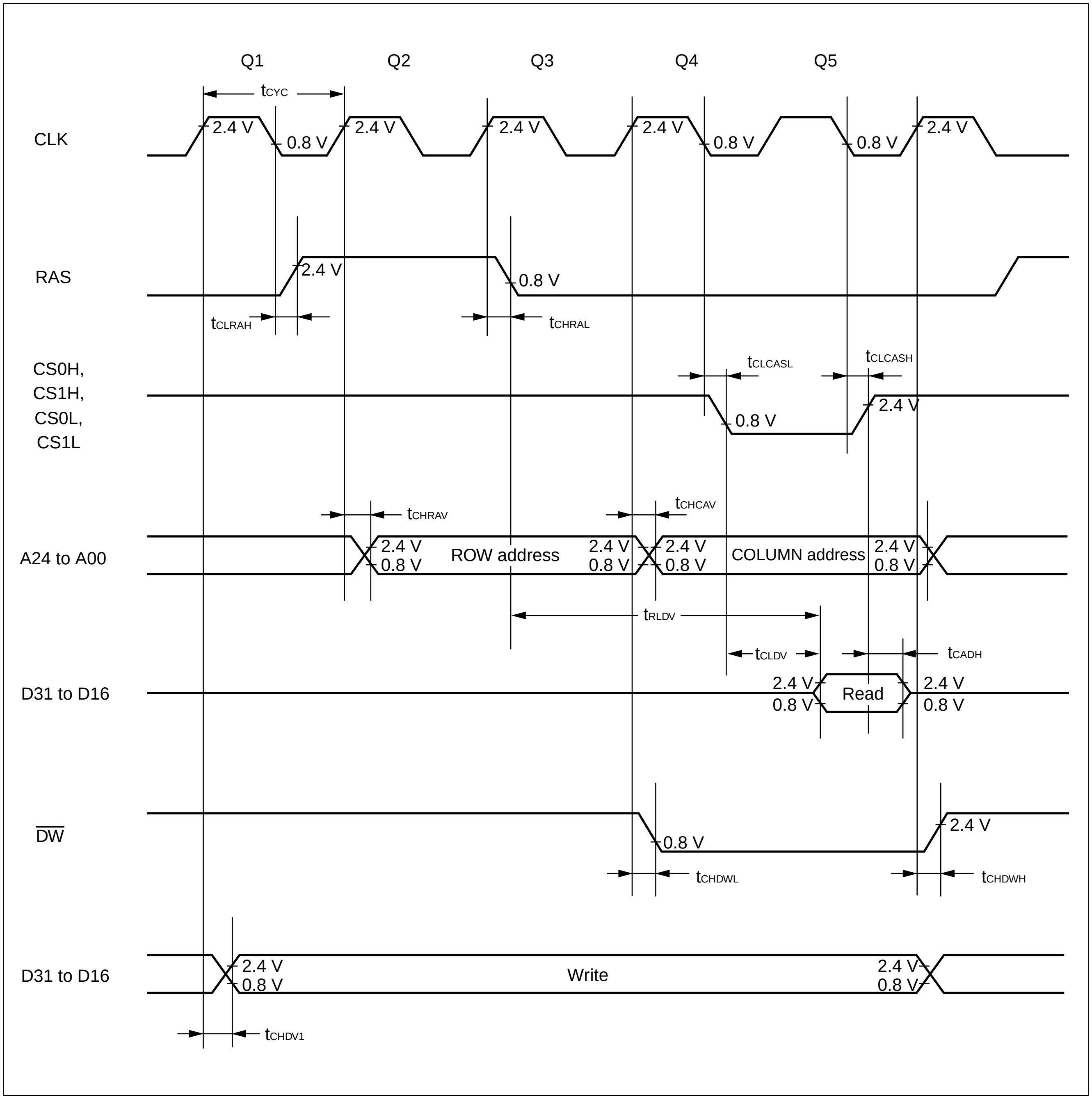
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
RAS delay time	t_{CLRAH}	CLK, RAS	—	—	15	ns	
	t_{CHRAL}	CLK, RAS		—	15	ns	
CAS delay time	t_{CLCASL}	CLK, CS0H, CS1H, CS0L, CS1L		—	15	ns	
	t_{CLCASH}	CLK, CS0H, CS1H, CS0L, CS1L		—	15	ns	
ROW address delay time	t_{CHRAV}	CLK, A24 to A00		—	15	ns	
COLUMN address delay time	t_{CHCAV}	CLK, A24 to A00		—	15	ns	
$\overline{DW}$ delay time	t_{CHDWL}	CLK, $\overline{DW}$*2		—	15	ns	
	t_{CHDWH}	CLK, $\overline{DW}$*2		—	15	ns	
Output data delay time	t_{CHDV1}	CLK, D31 to D16		—	15	ns	
RAS ↓→ valid data input time	t_{RLDV}	RAS, D31 to D16		—	$5/2 \times t_{CYC}$*1 – 16	ns	*3 *4
CAS ↓→ valid data input time	t_{CLDV}	CS0H, CS1H, CS0L, CS1L, D31 to D16		—	t_{CYC}*1 – 17	ns	*3
CAS ↑→ data hold time	t_{CADH}	CS0H, CS1H, CS0L, CS1L, D31 to D16		10	—	ns	

*1: For information on t_{CYC} (a cycle time of peripheral system clock), see “(3) Clock Output Timing.”

*2: $\overline{DW}$ expresses that $\overline{DW0}$, $\overline{DW1}$ and CS0H, CS1H are used for $\overline{WE}$.

*3: When Q1 cycle or Q4 cycle is extended for 1 cycle, add t_{CYC} time to this rating.

*4: Rating at a gear cycle of × 1.
When a gear cycle of 1/2, 1/4, 1/8 is selected, substitute “n” in the following equation with 1/2, 1/4, 1/8, respectively.
Equation: $(3 – n/2) \times t_{CYC} – 16$


Q1
Q2
Q3
Q4
Q5
tCYC
CLK
2.4 V
0.8 V
RAS
tCLRAH
tCHRAL
CS0H,
CS1H,
CS0L,
CS1L
tCLCASL
tCLCASH
tCHRAV
tCHCAV
A24 to A00
ROW address
COLUMN address
tRLDV
tCLDV
tCADH
D31 to D16
Read
DW
tCHDWL
tCHDWH
D31 to D16
Write
tCHDV1

(10) Normal DRAM Mode Fast Page Read/Write Cycle

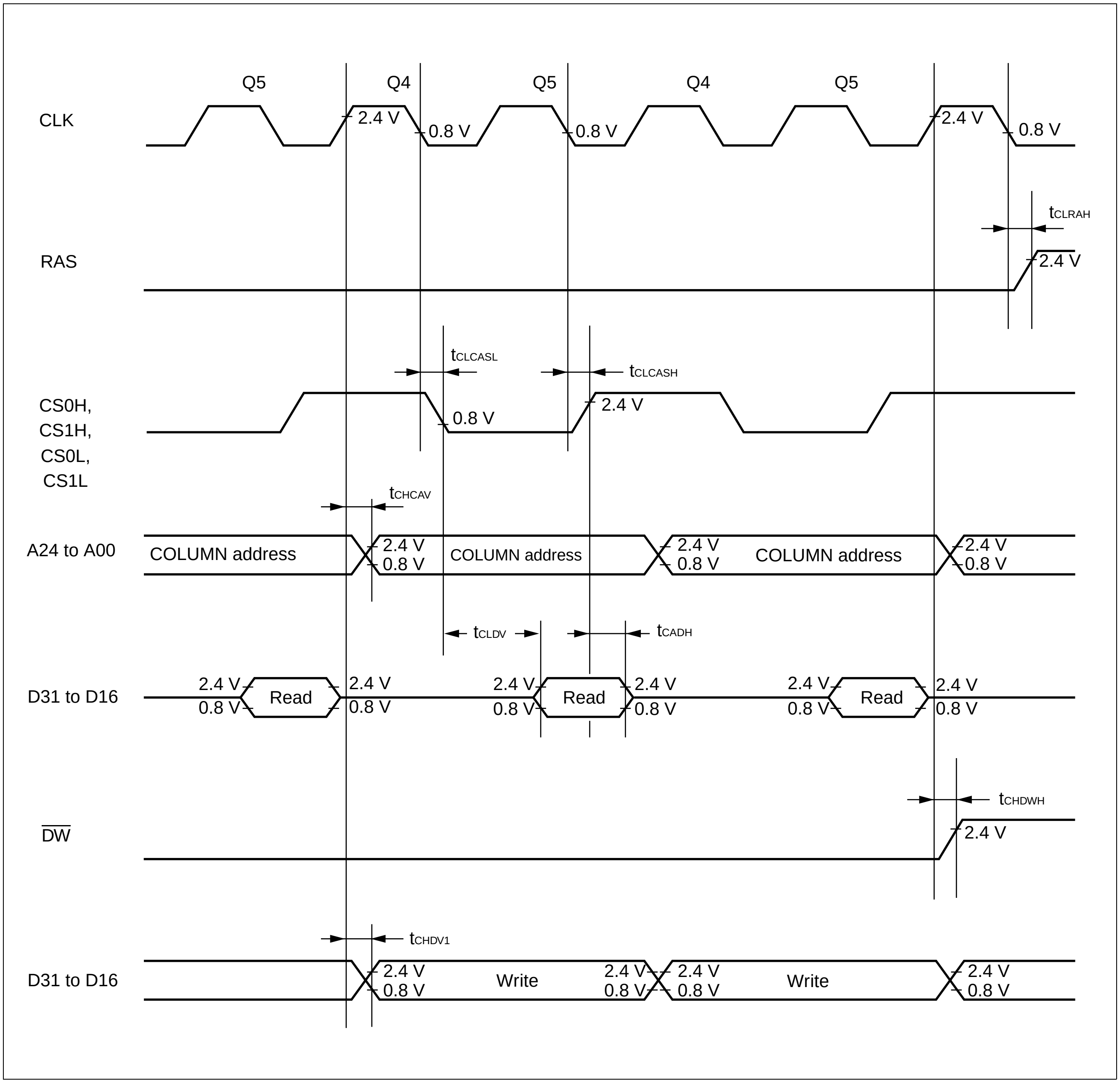
(V_{CC} = 3.15 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
RAS delay time	t_{CLRAH}	CLK, RAS	—	—	15	ns	
CAS delay time	t_{CLCASL}	CLK, CS0H, CS1H, CS0L, CS1L		—	15	ns	
	t_{CLCASH}	CLK, CS0H, CS1H, CS0L, CS1L		—	15	ns	
COLUMN address delay time	t_{CHCAV}	CLK, A24 to A00		—	15	ns	
$\overline{DW}$ delay time	t_{CHDWH}	CLK, $\overline{DW}$*2		—	15	ns	
Output data delay time	t_{CHDV1}	CLK, D31 to D16		—	15	ns	
CAS ↓→ valid data input time	t_{CLDV}	CS0H, CS1H, CS0L, CS1L, D31 to D16		—	t_{CYC}*1 – 17	ns	*3
CAS ↑→ data hold time	t_{CADH}	CS0H, CS1H, CS0L, CS1L, D31 to D16		10	—	ns	

*1: For information on t_{CYC} (a cycle time of peripheral system clock), see “(3) Clock Output Timing.”

*2: $\overline{DW}$ expresses that $\overline{DW0}$, $\overline{DW1}$ and CS0H, CS1H are used for $\overline{WE}$.

*3: When Q4 cycle is extended for 1 cycle, add t_{CYC} time to this rating.



Q5
Q4
Q5
Q4
Q5
CLK
2.4 V
0.8 V
0.8 V
2.4 V
0.8 V
tCLRAH
RAS
2.4 V
tCLCASL
tCLCASH
CS0H,
CS1H,
CS0L,
CS1L
0.8 V
2.4 V
tCHCAV
A24 to A00
COLUMN address
2.4 V
0.8 V
COLUMN address
2.4 V
0.8 V
COLUMN address
2.4 V
0.8 V
tCLDV
tCADH
D31 to D16
2.4 V
0.8 V
Read
2.4 V
0.8 V
Read
Read
tCHDWH
DW
2.4 V
tCHDV1
D31 to D16
Write
Write
2.4 V
0.8 V

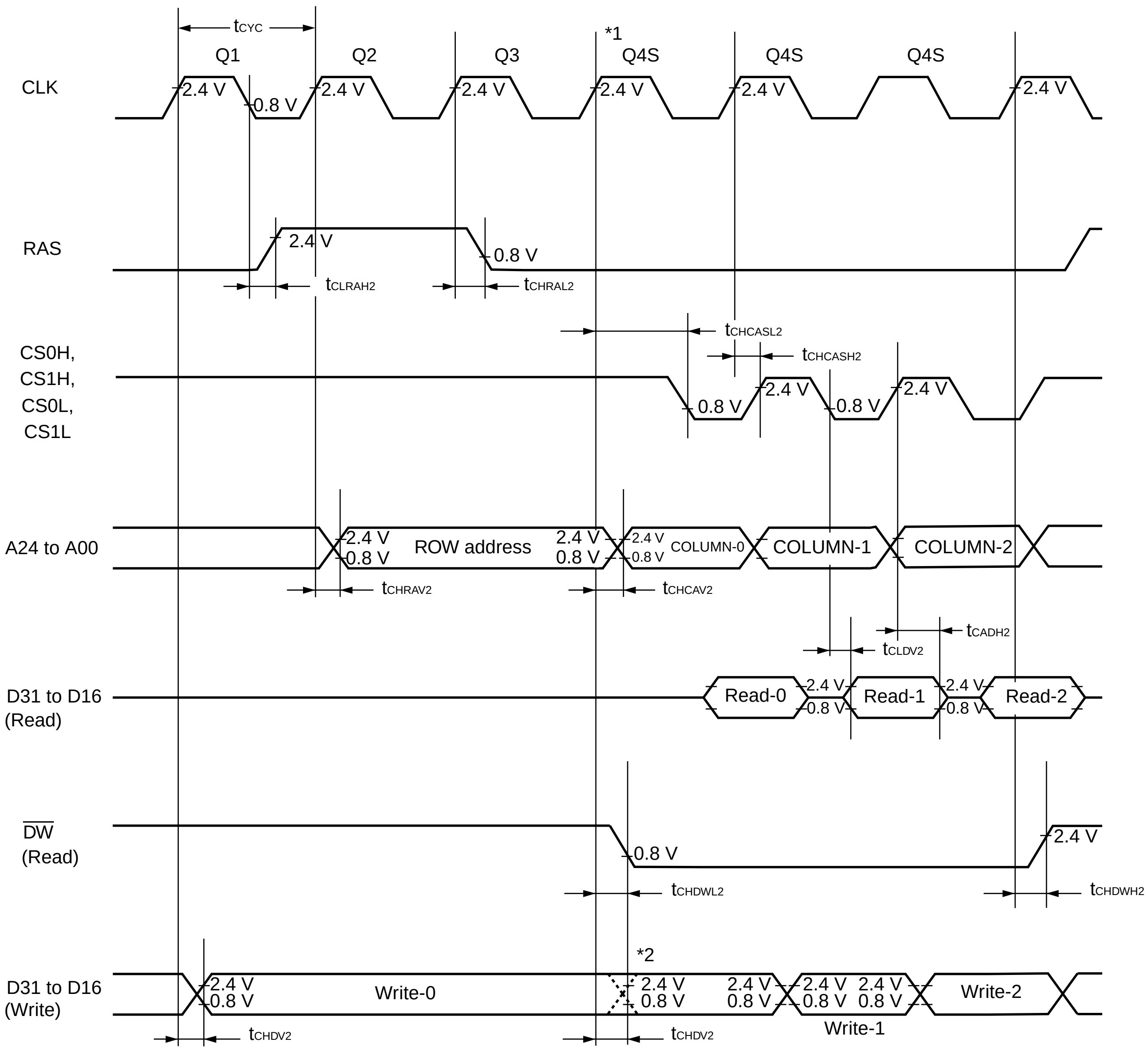
(11) Single DRAM Timing

(V_{CC} = 3.15 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
RAS delay time	t_{CLRAH2}	CLK, RAS	—	—	15	ns	
	t_{CHRAL2}	CLK, RAS			15	ns	
CAS delay time	$t_{CHCASL2}$	CLK, CS0H, CS1H, CS0L, CS1L		—	$n/2 \times t_{CYC}$*1	ns	
	$t_{CHCASH2}$	CLK, CS0H, CS1H, CS0L, CS1L		—	15	ns	
ROW address delay time	t_{CHRAV2}	CLK, A24 to A00		—	15	ns	
COLUMN address delay time	t_{CHCAV2}	CLK, A24 to A00		—	15	ns	
$\overline{\text{DW}}$ delay time	t_{CHDWL2}	CLK, $\overline{\text{DW}}$*2		—	15	ns	
	t_{CHDWH2}	CLK, $\overline{\text{DW}}$*2		—	15	ns	
Output data delay time	t_{CHDV2}	CLK, D31 to D16		—	15	ns	
CAS ↓→ Valid data input time	t_{CLDV2}	CS0H, CS1H, CS0L, CS1L, D31 to D16		—	$(1 - n/2) \times t_{CYC}$*1 – 17	ns	
CAS ↑→ data hold time	t_{CADH2}	CS0H, CS1H, CS0L, CS1L, D31 to D16		10	—	ns	

*1: For information on t_{CYC} (a cycle time of peripheral system clock), see “(3) Clock Output Timing.”

*2: $\overline{\text{DW}}$ expresses that $\overline{\text{DW0}}$, $\overline{\text{DW1}}$ and CS0H, CS1H are used for $\overline{\text{WE}}$.



*1: Q4S indicates Q4SR (Read) of Single DRAM cycle or Q4SW (Write) cycle.
*2: - - - - indicates the timing when the bus cycle begins from the high speed page mode.

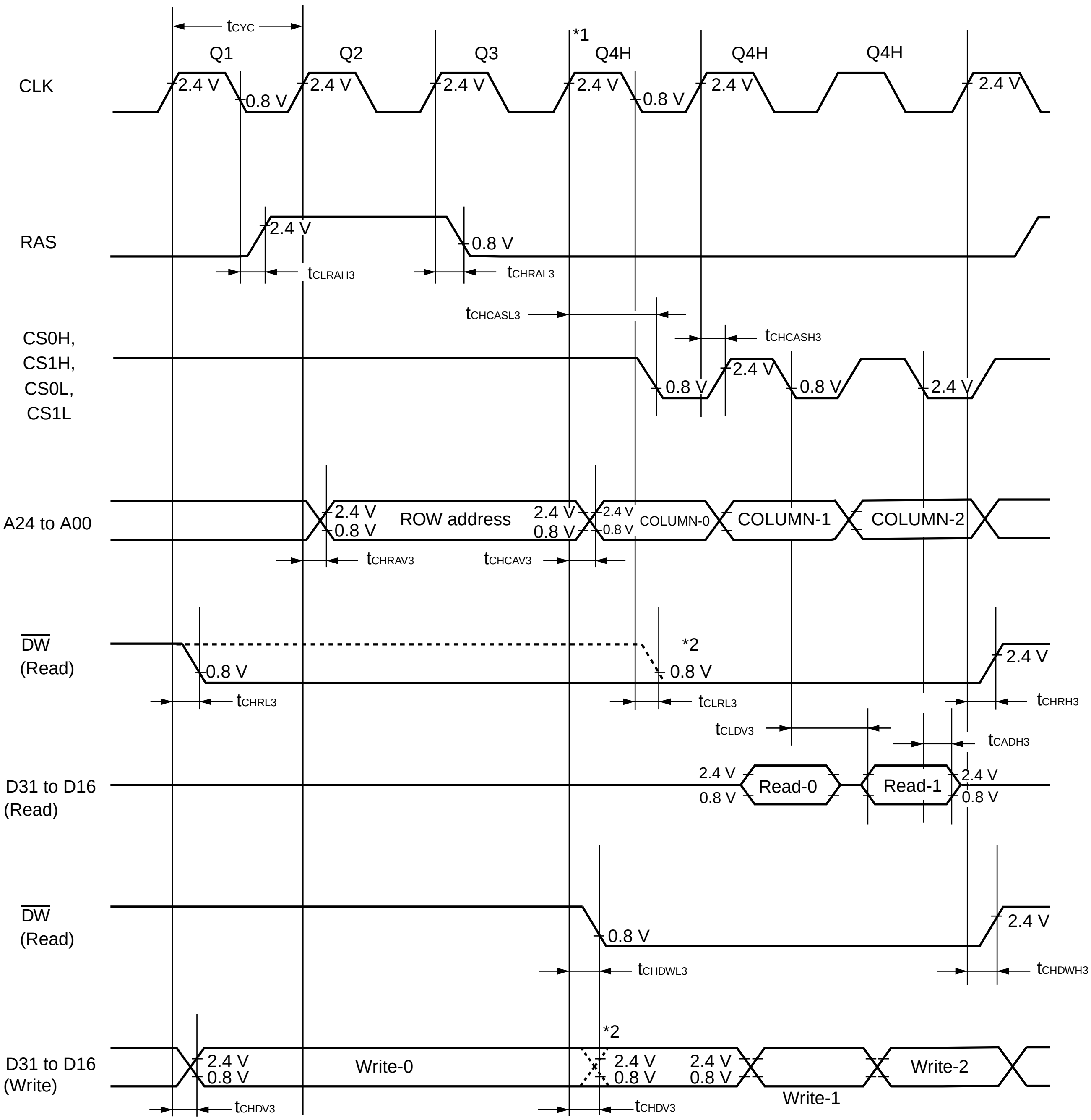
(12) Hyper DRAM Timing

(V_{CC} = 3.15 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
RAS delay time	t_{CLRAH3}	CLK, RAS	—	—	15	ns	
	t_{CHRAL3}	CLK, RAS		—	15	ns	
CAS delay time	$t_{CHCASL3}$	CLK, CS0H, CS1H, CS0L, CS1L		—	n/2 × t_{CYC}*1	ns	
	$t_{CHCASH3}$	CLK, CS0H, CS1H, CS0L, CS1L		—	15	ns	
ROW address delay time	t_{CHRAV3}	CLK, A24 to A00		—	15	ns	
COLUMN address delay time	t_{CHCAV3}	CLK, A24 to A00		—	15	ns	
$\overline{RD}$ delay time	t_{CHRL3}	CLK, $\overline{RD}$		—	15	ns	
	t_{CHRH3}	CLK, $\overline{RD}$		—	15	ns	
	t_{CLRL3}	CLK, $\overline{RD}$		—	15	ns	
$\overline{DW}$ delay time	t_{CHDWL3}	CLK, $\overline{DW}$*2		—	15	ns	
	t_{CHDWH3}	CLK, $\overline{DW}$*2		—	15	ns	
Output data delay time	t_{CHDV3}	CLK, D31 to D16		—	15	ns	
CAS $\downarrow\rightarrow$ valid data input time	t_{CLDV3}	CS0H, CS1H, CS0L, CS1L, D31 to D16		—	t_{CYC} – 17	ns	
CAS $\downarrow\rightarrow$ data hold time	t_{CADH3}	CS0H, CS1H, CS0L, CS1L, D31 to D16		10	—	ns	

*1: For information on t_{CYC} (a cycle time of peripheral system clock), see “(3) Clock Output Timing.”

*2: $\overline{DW}$ expresses that $\overline{DW0}$, $\overline{DW1}$ and CS0H, CS1H are used for $\overline{WE}$.

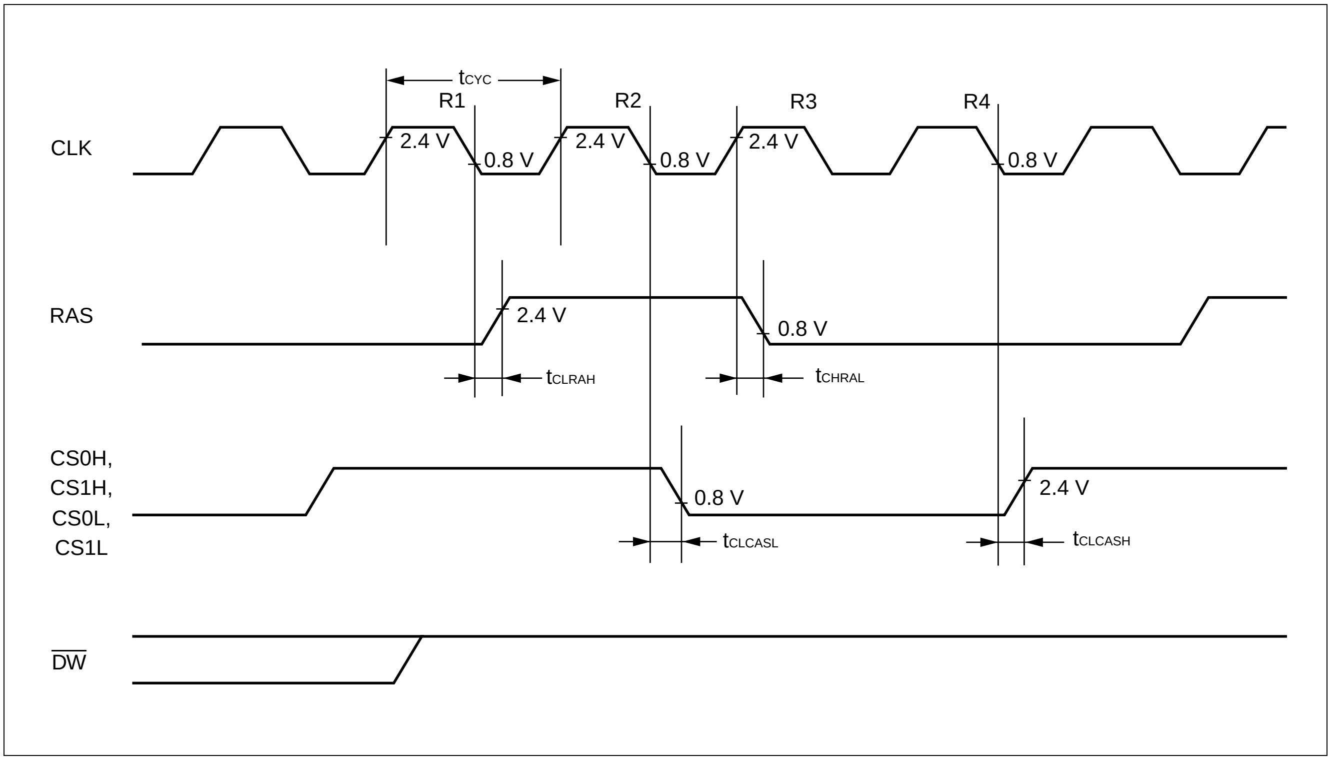


*1: Q4S indicates Q4SR (Read) of Single DRAM cycle or Q4SW (Write) cycle.
*2: - - - - indicates the timing when the bus cycle begins from the high speed page mode.

(13) **CBR Refresh**

(V_{CC} = 3.15 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)

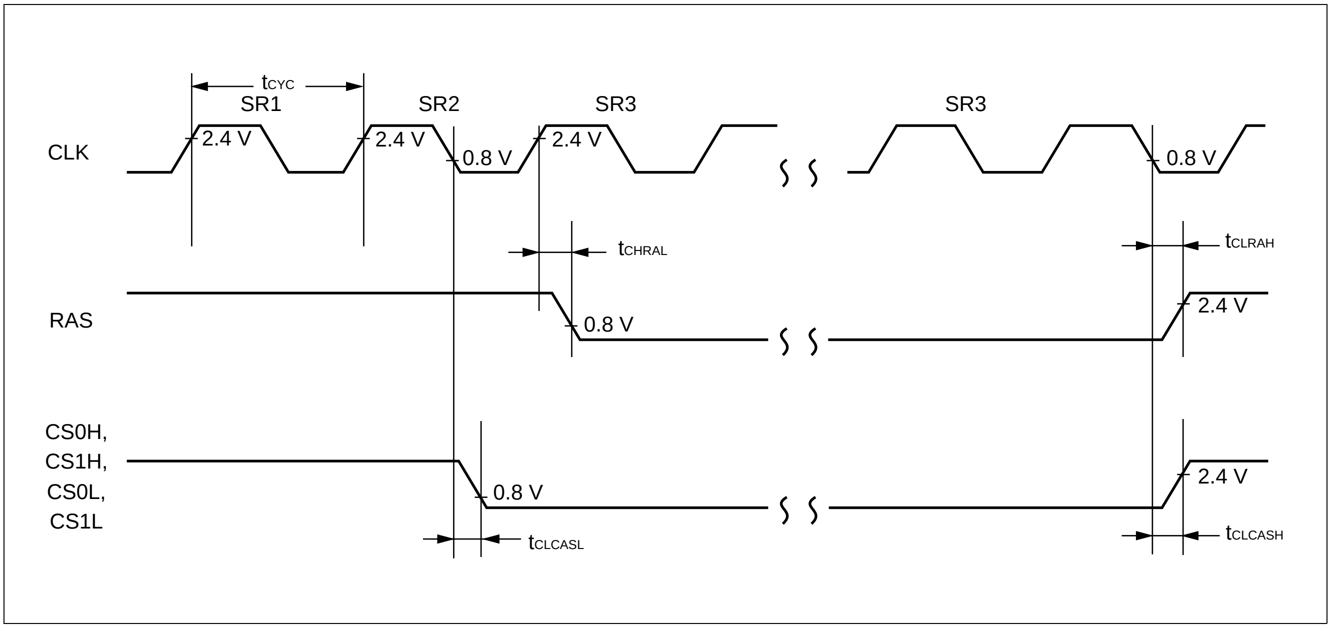
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
RAS delay time	t_{CLRAH}	CLK, RAS	—	—	15	ns	
	t_{CHRAL}	CLK, RAS		—	15	ns	
CAS delay time	t_{CLCASL}	CLK, CS0H, CS1H, CS0L, CS1L		—	15	ns	
	t_{CLCASH}	CLK, CS0H, CS1H, CS0L, CS1L		—	15	ns	



(14) Self Refresh

(V_{CC} = 3.15 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
RAS delay time	t_{CLRAH}	CLK, RAS	—	—	15	ns	
	t_{CHRAL}	CLK, RAS		—	15	ns	
CAS delay time	t_{CLCASL}	CLK, CS0H, CS1H, CS0L, CS1L		—	15	ns	
	t_{CLCASH}	CLK, CS0H, CS1H, CS0L, CS1L		—	15	ns	



(15) UART Timing

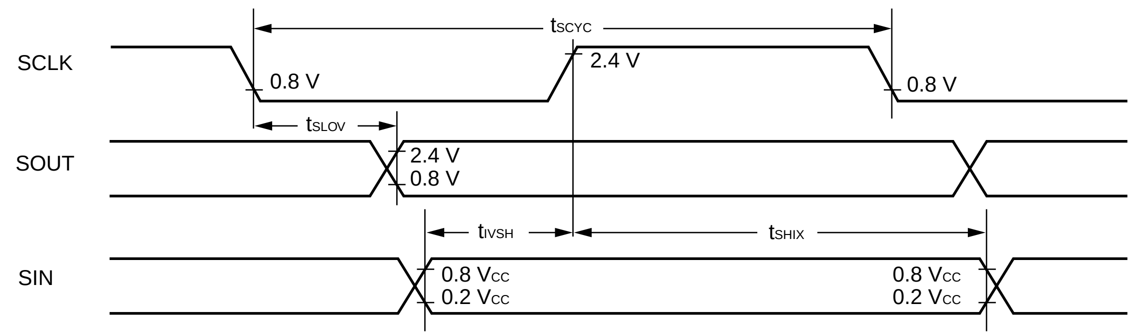
(V_{CC} = 3.15V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	—	Internal shift clock mode	8 × t_{CYCP}*	—	ns	
SCLK ↓→ SOUT delay time	t_{SLOV}	—		–80	80	ns	
Valid SIN → SCLK ↑	t_{IVSH}	—		100	—	ns	
SCLK ↑→ valid SIN hold time	t_{SHIX}	—		60	—	ns	
Serial clock "H" pulse width	t_{SHSL}	—	External shift clock mode	4 × t_{CYCP}*	—	ns	
Serial clock "L" pulse width	t_{SLSH}	—		4 × t_{CYCP}*	—	ns	
SCLK ↓→ SOUT delay time	t_{SLOV}	—		—	150	ns	
Valid SIN → SCLK ↑	t_{IVSH}	—		60	—	ns	
SCLK ↑→ valid SIN hold time	t_{SHIX}	—		60	—	ns	

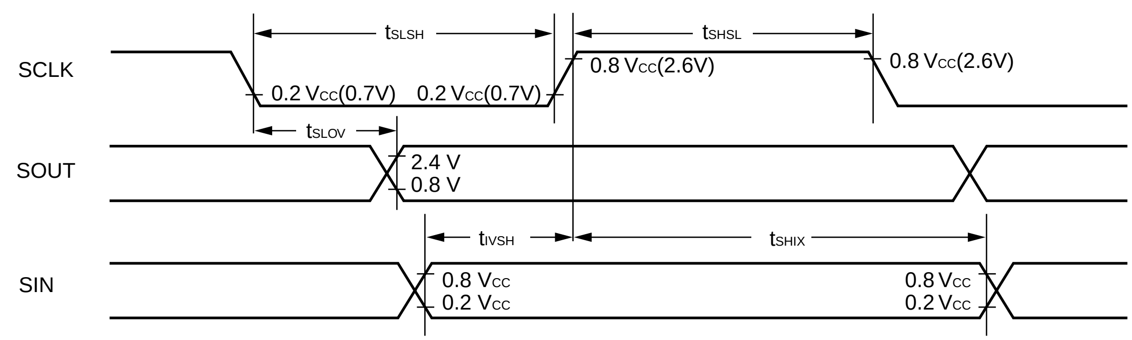
*: For information on t_{CYCP} (a cycle time of peripheral system clock), see "(2) Clock Timing Rating."

Notes: This rating is for AC characteristics in CLK synchronous mode.

• **Internal shift clock mode**



• **External shift clock mode**

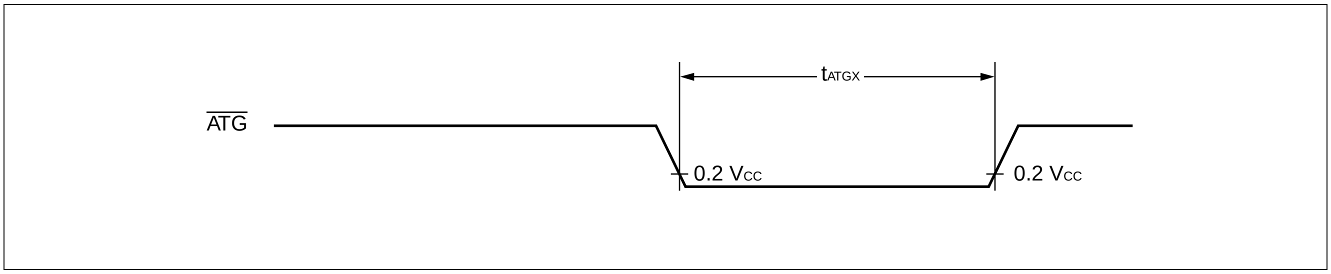


(16) Trigger System Input Timing

(V_{CC} = 3.15 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
A/D start trigger input time	t_{ATGX}	$\overline{ATG}$	—	$5 \times t_{CYCP}$*	—	ns	

*: For information on t_{CYCP} (a cycle time of peripheral system clock), see “(2) Clock Timing Rating.”

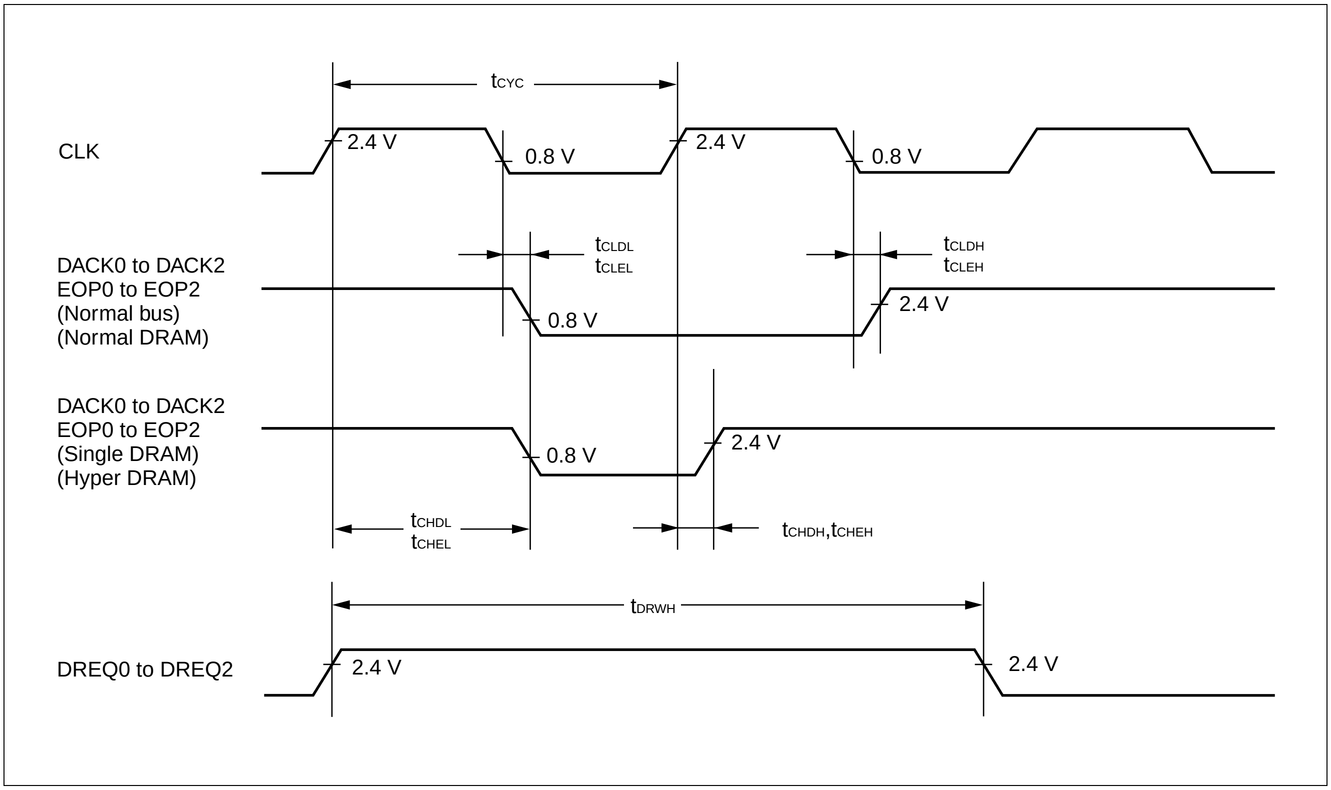


(17) DMA Controller Timing

(V_{CC} = 3.15 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
DREQ input pulse width	t_{DRWH}	DREQ0 to DREQ2	—	$2 \times t_{CYC}$*	—	ns	
DACK delay time (Normal bus) (Normal DRAM)	t_{CLDL}	CLK, DACK0 to DACK2		—	6	ns	
	t_{CLDH}	CLK, DACK0 to DACK2		—	6	ns	
EOP delay time (Normal bus) (Normal DRAM)	t_{CLEL}	CLK, EOP0 to EOP2		—	6	ns	
	t_{CLEH}	CLK, EOP0 to EOP2		—	6	ns	
DACK delay time (Single DRAM) (Hyper DRAM)	t_{CHDL}	CLK, DACK0 to DACK2		—	$n/2 \times t_{CYC}$*	ns	
	t_{CHDH}	CLK, DACK0 to DACK2		—	6	ns	
EOP delay time (Single DRAM) (Hyper DRAM)	t_{CHEL}	CLK, EOP0 to EOP2		—	$n/2 \times t_{CYC}$*	ns	
	t_{CHEH}	CLK, EOP0 to EOP2		—	6	ns	

*: For information on t_{CYC} (a cycle time of peripheral system clock), see “(3) Clock Output Timing.”



6. A/D Converter Block Electrical Characteristics

(V_{CC} = AV_{CC} = 3.15 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, AVRH = 3.15 V to 3.6 V, T_A = 0°C to +70°C)

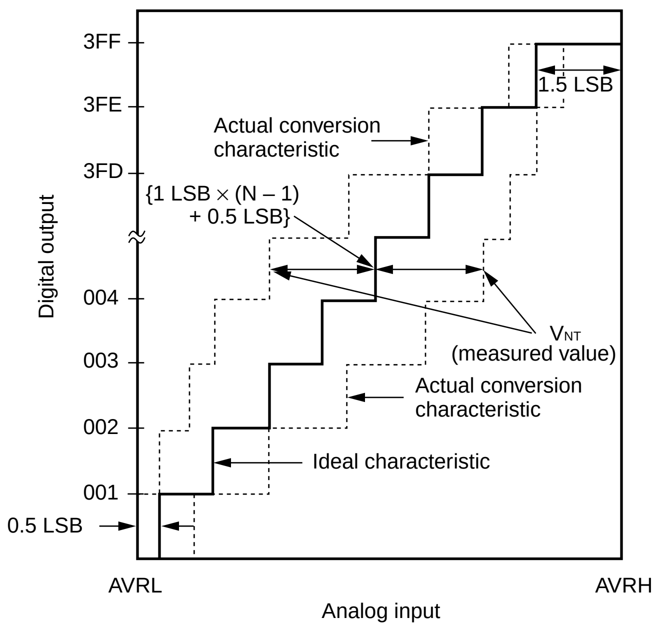
Parameter	Symbol	Pin name	Value			Unit
			Min.	Typ.	Max.	
Resolution	—	—	—	10	10	bit
Total error	—	—	—	—	±3.0	LSB
Linearity error	—	—	—	—	±2.5	LSB
Differentiation linearity error	—	—	—	—	±1.9	LSB
Zero transition voltage	V_{OT}	AN0 to AN3	–1.5LSB	+0.5LSB	+2.5LSB	mV
Full-scale transition voltage	V_{FST}	AN0 to AN3	AVRH – 4.5LSB	AVRH – 1.5LSB	AVRH + 0.5LSB	mV
Conversion time	—	—	5.19 *1	—	—	µs
Analog port input current	I_{AIN}	AN0 to AN3	—	0.1	10	µA
Analog input voltage	V_{AIN}	AN0 to AN3	AV_{SS}	—	AVRH	V
Reference voltage	—	AVRH	AV_{SS}	—	AV_{CC}	V
Power supply current	I_A	AV_{CC}	—	4	—	mA
	I_{AH}	AV_{CC}	—	—	5 *2	µA
Reference voltage supply current	I_R	AVRH	—	110	—	µA
	I_{RH}	AVRH	—	—	5 *2	µA
Conversion variance between channels	—	AN0 to AN3	—	—	4	LSB

*1: V_{CC} = AV_{CC} = 3.15 V to 3.6 V, machine clock 25 MHz
*2: Current value for A/D converters not in operation, CPU stop mode (V_{CC} = AV_{CC} = AVRH = 3.6 V)

7. A/D Converter Glossary

- Resolution
  The smallest change in analog voltage detected by A/D converter.
- Linearity error
  A deviation of actual conversion characteristic from a line connecting the zero-traction point (between "00 0000 0000" ↔ "00 0000 0001") to the full-scale transition point (between "11 1111 1110" ↔ "11 1111 1111").
- Differential linearity error
  A deviation of a step voltage for changing the LSB of output code from ideal input voltage.
- Total error
  A difference between actual value and theoretical value. The overall error includes zero-transition error, full-scale transition error and linearity error.

Total error



$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\text{ LSB} \times (N - 1) + 0.5\text{ LSB}\}}{1\text{ LSB}} \text{ [LSB]}$$

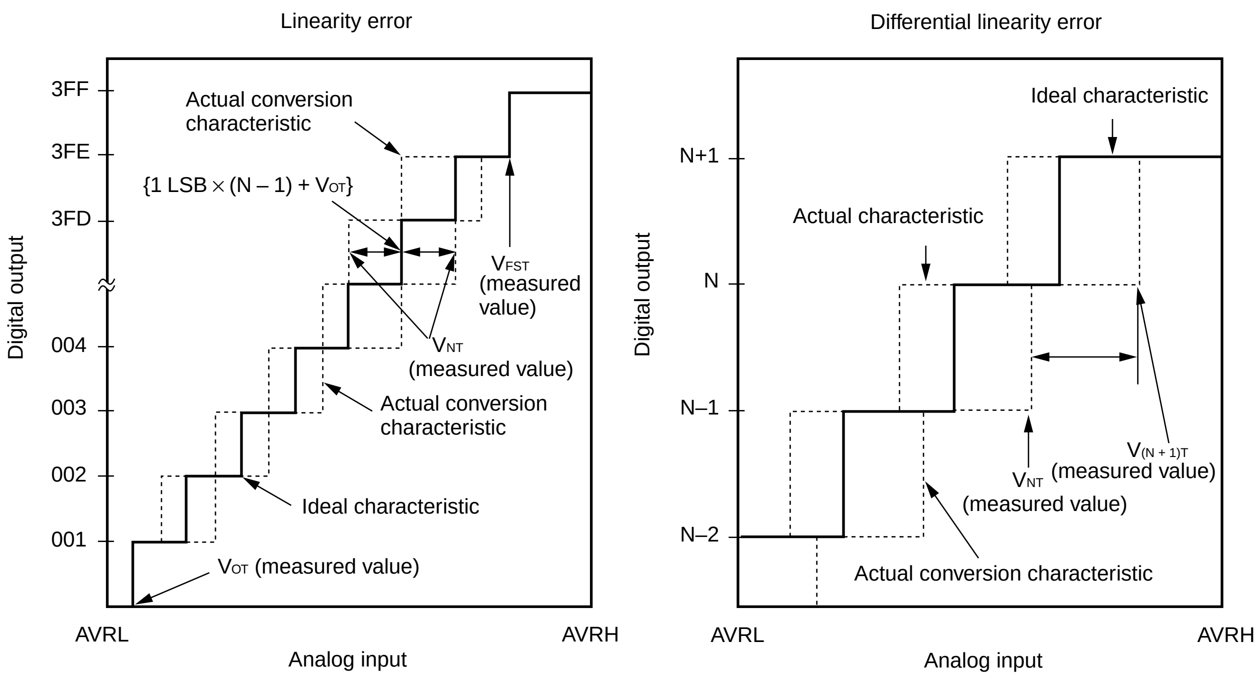
V_{OT} (ideal value) = AVRL + 0.5 LSB [V]

V_{FST} (ideal value) = AVRL – 1.5 LSB [V]

V_{NT}: A voltage for causing transition of digital output from (N – 1) to N

(Continued)

(Continued)



Linearity error of digital output N $= \dfrac{V_{NT} - \{1\ \text{LSB} \times (N-1) + V_{OT}\}}{1\ \text{LSB}}$ [LSB]

Differential linearity error of digital output N $= \dfrac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1$ [LSB]

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

$$1\ \text{LSB (ideal value)} = \frac{\text{AVRH} - \text{AVRL}}{1022}\ [\text{V}]$$

V_{OT}: A voltage for causing transition of digital output from $(000)_H$ to $(001)_H$

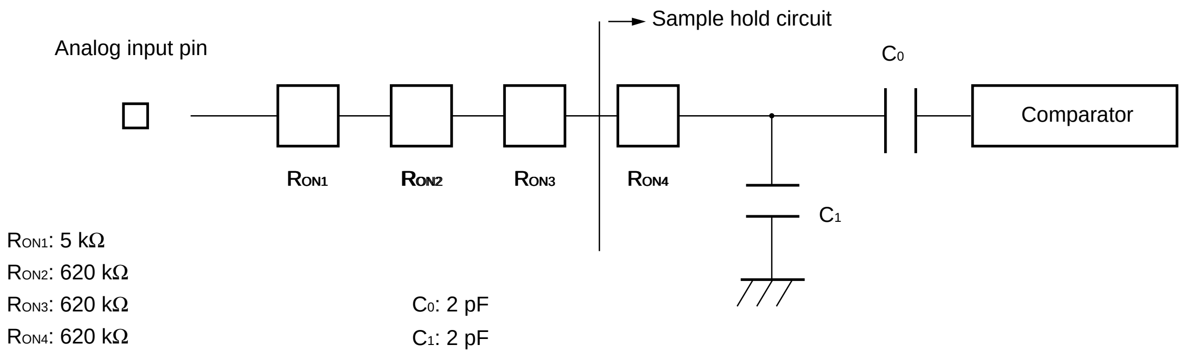
V_{FST}: A voltage for causing transition of digital output from $(3FE)_H$ to $(3FF)_H$

V_{NT}: A voltage for causing transition of digital output from $(N-1)_H$ to N

8. Notes on Using A/D Converter

Output impedance of external circuit of analog input under following conditions;
Output impedance of external circuit < 7 kΩ.
If output impedance of external circuit is too high, analog voltage sampling time may be too short for accurate sampling (sampling time is 5.6 µs for a machine clock of 25 MHz).

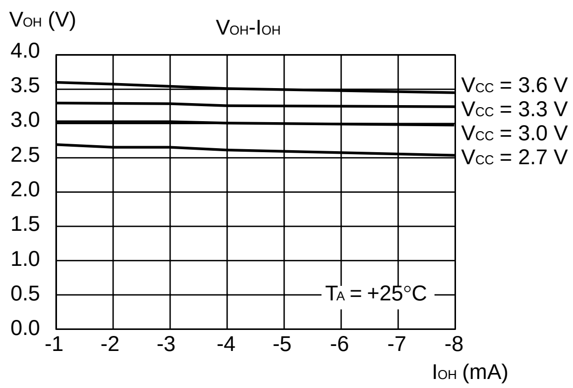
- **Analog input Equivalent Circuit**



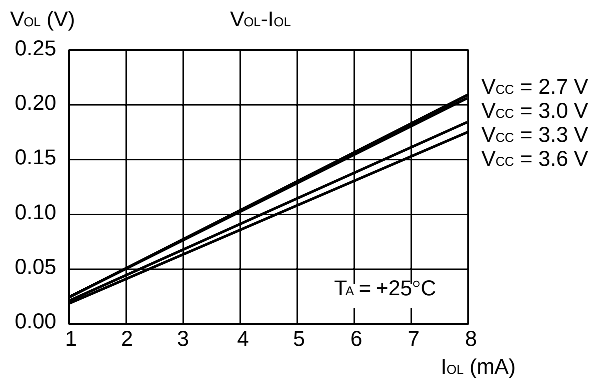
- Error
  As the absolute value of |AVRH − AVRL| decreases, relative error increases.

■ EXAMPLE CHARACTERISTICS

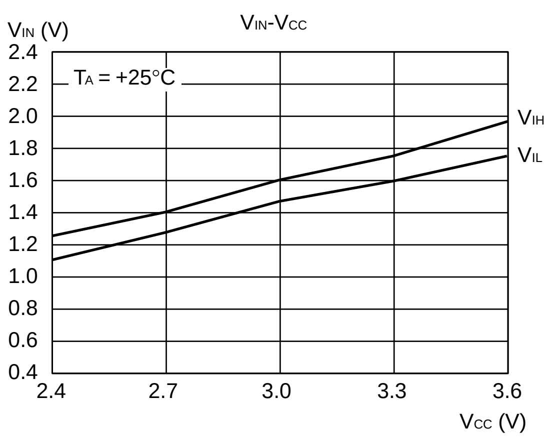
(1) "H" Level Output Voltage



(2) "L" Level Output Voltage



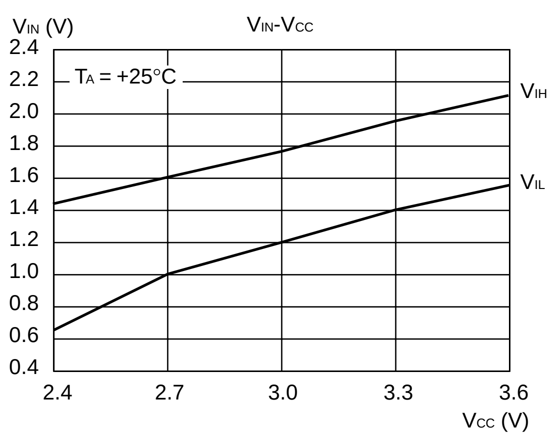
(3) "H" Level Input Voltage/"L" Level Input Voltage (CMOS Input)



V_{IH}: Threshold when input voltage is set to "H" Level.

V_{IL}: Threshold when input voltage is set to "L" Level.

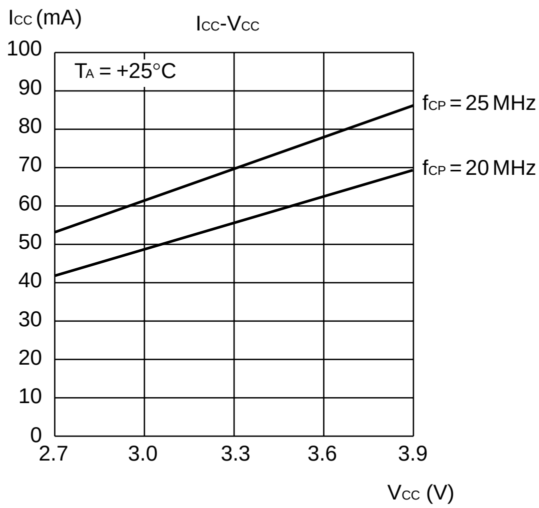
(4) "H" Level Input Voltage/"L" Level Input Voltage (Hysteresis Input)

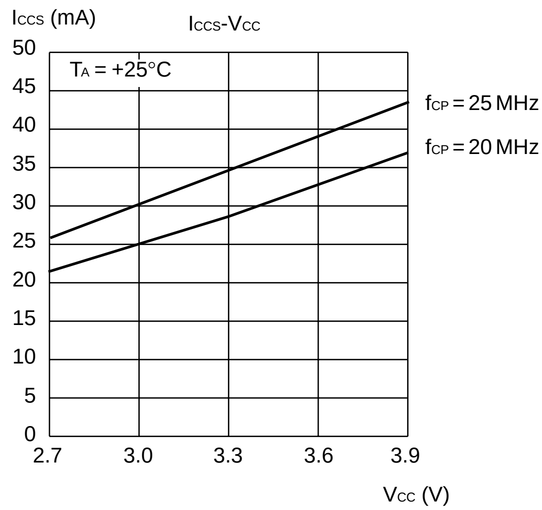


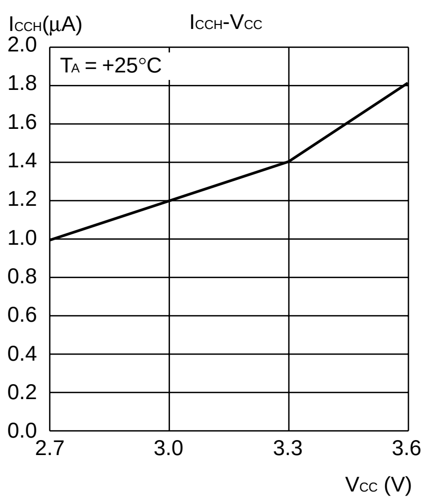
V_{IH}: Threshold when input voltage in hysteresis characteristics is set to "H" Level.

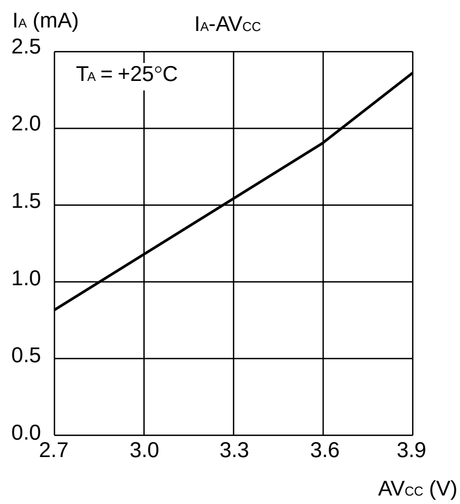
V_{IL}: Threshold when input voltage in hysteresis characteristics is set to "L" Level.

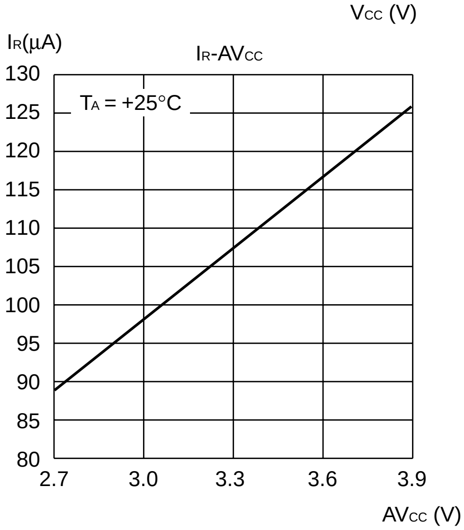
(5) Power Supply Current (fcp = Internal clock frequency)



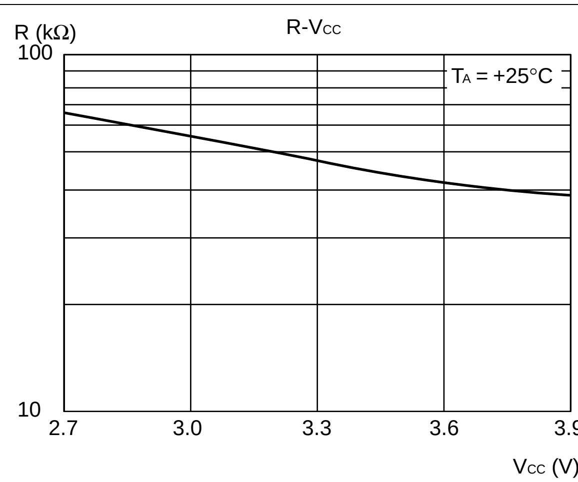








(6) Pull-up Resistance



■ INSTRUCTIONS (165 INSTRUCTIONS)

1. How to Read Instruction Set Summary

Mnemonic	Type	OP	CYC	NZVC	Operation	Remarks
ADD Rj, Ri	A	A6	1	CCCC	Ri + Rj → Ri	
* ADD #s5, Ri	C	A4	1	CCCC	Ri + s5 → Ri	
,	,	,	,	,	,	
,	,	,	,	,	,	

↓ (1) ↓ (2) ↓ (3) ↓ (4) ↓ (5) ↓ (6) ↓ (7)

(1) Names of instructions
Instructions marked with * are not included in CPU specifications. These are extended instruction codes added/extended at assembly language levels.

(2) Addressing modes specified as operands are listed in symbols.
Refer to “2. Addressing mode symbols” for further information.

(3) Instruction types

(4) Hexa-decimal expressions of instructions

(5) The number of machine cycles needed for execution

a: Memory access cycle and it has possibility of delay by Ready function.

b: Memory access cycle and it has possibility of delay by Ready function.
If an object register in a LD operation is referenced by an immediately following instruction, the interlock function is activated and number of cycles needed for execution increases.

c: If an immediately following instruction operates to an object of R15, SSP or USP in read/write mode or if the instruction belongs to instruction format A group, the interlock function is activated and number of cycles needed for execution increases by 1 to make the total number of 2 cycles needed.

d: If an immediately following instruction refers to MDH/MDL, the interlock function is activated and number of cycles needed for execution increases by 1 to make the total number of 2 cycles needed.

For a, b, c and d, minimum execution cycle is 1.

(6) Change in flag sign

- Flag change
  C : Change
  – : No change
  0 : Clear
  1 : Set
- Flag meanings
  N : Negative flag
  Z : Zero flag
  V : Over flag
  C : Carry flag

(7) Operation carried out by instruction

2. Addressing Mode Symbols

Ri	: Register direct (R0 to R15, AC, FP, SP)
Rj	: Register direct (R0 to R15, AC, FP, SP)
R13	: Register direct (R13, AC)
Ps	: Register direct (Program status register)
Rs	: Register direct (TBR, RP, SSP, USP, MDH, MDL)
CRi	: Register direct (CR0 to CR15)
CRj	: Register direct (CR0 to CR15)
#i8	: Unsigned 8-bit immediate (–128 to 255) Note: –128 to –1 are interpreted as 128 to 255
#i20	: Unsigned 20-bit immediate (–0X80000 to 0XFFFFF) Note: –0X7FFFF to –1 are interpreted as 0X7FFFF to 0XFFFFF
#i32	: Unsigned 32-bit immediate (–0X80000000 to 0XFFFFFFFF) Note: –0X80000000 to –1 are interpreted as 0X80000000 to 0XFFFFFFFF
#s5	: Signed 5-bit immediate (–16 to 15)
#s10	: Signed 10-bit immediate (–512 to 508, multiple of 4 only)
#u4	: Unsigned 4-bit immediate (0 to 15)
#u5	: Unsigned 5-bit immediate (0 to 31)
#u8	: Unsigned 8-bit immediate (0 to 255)
#u10	: Unsigned 10-bit immediate (0 to 1020, multiple of 4 only)
@dir8	: Unsigned 8-bit direct address (0 to 0XFF)
@dir9	: Unsigned 9-bit direct address (0 to 0X1FE, multiple of 2 only)
@dir10	: Unsigned 10-bit direct address (0 to 0X3FC, multiple of 4 only)
label9	: Signed 9-bit branch address (–0X100 to 0XFC, multiple of 2 only)
label12	: Signed 12-bit branch address (–0X800 to 0X7FC, multiple of 2 only)
label20	: Signed 20-bit branch address (–0X80000 to 0X7FFFF)
label32	: Signed 32-bit branch address (–0X80000000 to 0X7FFFFFFF)
@Ri	: Register indirect (R0 to R15, AC, FP, SP)
@Rj	: Register indirect (R0 to R15, AC, FP, SP)
@(R13, Rj)	: Register relative indirect (Rj: R0 to R15, AC, FP, SP)
@(R14, disp10)	: Register relative indirect (disp10: –0X200 to 0X1FC, multiple of 4 only)
@(R14, disp9)	: Register relative indirect (disp9: –0X100 to 0XFE, multiple of 2 only)
@(R14, disp8)	: Register relative indirect (disp8: –0X80 to 0X7F)
@(R15, udisp6)	: Register relative (udisp6: 0 to 60, multiple of 4 only)
@Ri+	: Register indirect with post-increment (R0 to R15, AC, FP, SP)
@R13+	: Register indirect with post-increment (R13, AC)
@SP+	: Stack pop
@–SP	: Stack push
(reglist)	: Register list

3. Instruction Types

MSB — 16 bits — LSB

Type A

OP	Rj	Ri
8	4	4

Type B

OP	i8/o8	Ri
4	8	4

Type C

OP	u4/m4	Ri
8	4	4

ADD, ADDN, CMP, LSL, LSR and ASR instructions only

Type *C’

OP	s5/u5	Ri
7	5	4

Type D

OP	u8/rel8/dir/reglist
8	8

Type E

OP	SUB-OP	Ri
8	4	4

Type F

OP	rel11
5	11

4. Detailed Description of Instructions

- **Add/subtract operation instructions (10 instructions)**

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
ADD	Rj, Ri	A	A6	1	C C C C	Ri + Rj → Ri	
* ADD	#s5, Ri	C'	A4	1	C C C C	Ri + s5 → Ri	MSB is interpreted as a sign in assembly language
ADD	#i4, Ri	C	A4	1	C C C C	Ri + extu (i4) → Ri	Zero-extension
ADD2	#i4, Ri	C	A5	1	C C C C	Ri + extu (i4) → Ri	Sign-extension
ADDC	Rj, Ri	A	A7	1	C C C C	Ri + Rj + c → Ri	Add operation with sign
ADDN	Rj, Ri	A	A2	1	– – – –	Ri + Rj → Ri	
* ADDN	#s5, Ri	C'	A0	1	– – – –	Ri + s5 → Ri	MSB is interpreted as a sign in assembly language
ADDN	#i4, Ri	C	A0	1	– – – –	Ri + extu (i4) → Ri	Zero-extension
ADDN2	#i4, Ri	C	A1	1	– – – –	Ri + extu (i4) → Ri	Sign-extension
SUB	Rj, Ri	A	AC	1	C C C C	Ri – Rj → Ri	
SUBC	Rj, Ri	A	AD	1	C C C C	Ri – Rj – c → Ri	Subtract operation with carry
SUBN	Rj, Ri	A	AE	1	– – – –	Ri – Rj → Ri	

- **Compare operation instructions (3 instructions)**

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
CMP	Rj, Ri	A	AA	1	C C C C	Ri – Rj	
* CMP	#s5, Ri	C'	A8	1	C C C C	Ri – s5	MSB is interpreted as a sign in assembly language
CMP	#i4, Ri	C	A8	1	C C C C	Ri + extu (i4)	Zero-extension
CMP2	#i4, Ri	C	A9	1	C C C C	Ri + extu (i4)	Sign-extension

- **Logical operation instructions (12 instructions)**

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
AND	Rj, Ri	A	82	1	C C – –	Ri & = Rj	Word
AND	Rj, @Ri	A	84	1 + 2a	C C – –	(Ri) & = Rj	Word
ANDH	Rj, @Ri	A	85	1 + 2a	C C – –	(Ri) & = Rj	Half word
ANDB	Rj, @Ri	A	86	1 + 2a	C C – –	(Ri) & = Rj	Byte
OR	Rj, Ri	A	92	1	C C – –	Ri | = Rj	Word
OR	Rj, @Ri	A	94	1 + 2a	C C – –	(Ri) | = Rj	Word
ORH	Rj, @Ri	A	95	1 + 2a	C C – –	(Ri) | = Rj	Half word
ORB	Rj, @Ri	A	96	1 + 2a	C C – –	(Ri) | = Rj	Byte
EOR	Rj, Ri	A	9A	1	C C – –	Ri ^ = Rj	Word
EOR	Rj, @Ri	A	9C	1 + 2a	C C – –	(Ri) ^ = Rj	Word
EORH	Rj, @Ri	A	9D	1 + 2a	C C – –	(Ri) ^ = Rj	Half word
EORB	Rj, @Ri	A	9E	1 + 2a	C C – –	(Ri) ^ = Rj	Byte

• **Bit manipulation arithmetic instructions (8 instructions)**

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
BANDL	#u4, @Ri (u4: 0 to 0FH)	C	80	1 + 2a	– – – –	(Ri) & = (F0H + u4)	Manipulate lower 4 bits
BANDH	#u4, @Ri (u4: 0 to 0FH)	C	81	1 + 2a	– – – –	(Ri) & = ((u4<<4) + 0FH)	Manipulate upper 4 bits
* BAND	#u8, @Ri *1			–	– – – –	(Ri) & = u8	
BORL	#u4, @Ri (u4: 0 to 0FH)	C	90	1 + 2a	– – – –	(Ri) | = u4	Manipulate lower 4 bits
BORH	#u4, @Ri (u4: 0 to 0FH)	C	91	1 + 2a	– – – –	(Ri) | = (u4<<4)	Manipulate upper 4 bits
* BOR	#u8, @Ri *2			–	– – – –	(Ri) | = u8	
BEORL	#u4, @Ri (u4: 0 to 0FH)	C	98	1 + 2a	– – – –	(Ri) ^ = u4	Manipulate lower 4 bits
BEORH	#u4, @Ri (u4: 0 to 0FH)	C	99	1 + 2a	– – – –	(Ri) ^ = (u4<<4)	Manipulate upper 4 bits
* BEOR	#u8, @Ri *3			–	– – – –	(Ri) ^ = u8	
BTSTL	#u4, @Ri (u4: 0 to 0FH)	C	88	2 + a	0 C – –	(Ri) & u4	Test lower 4 bits
BTSTH	#u4, @Ri (u4: 0 to 0FH)	C	89	2 + a	C C – –	(Ri) & (u4<<4)	Test upper 4 bits

*1: Assembler generates BANDL if result of logical operation “u8&0x0F” leaves an active (set) bit and generates BANDH if “u8&0xF0” leaves an active bit. Depending on the value in the “u8” format, both BANDL and BANDH may be generated.
*2: Assembler generates BORL if result of logical operation “u8&0x0F” leaves an active (set) bit and generates BORH if “u8&0xF0” leaves an active bit.
*3: Assembler generates BEORL if result of logical operation “u8&0x0F” leaves an active (set) bit and generates BEORH if “u8&0xF0” leaves an active bit.

• **Add/subtract operation instructions (10 instructions)**

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
MUL	Rj, Ri	A	AF	5	C C C –	Rj × Ri → MDH, MDL	32-bit × 32-bit = 64-bit
MULU	Rj, Ri	A	AB	5	C C C –	Rj × Ri → MDH, MDL	Unsigned
MULH	Rj, Ri	A	BF	3	C C – –	Rj × Ri → MDL	16-bit × 16-bit = 32-bit
MULUH	Rj, Ri	A	BB	3	C C – –	Rj × Ri → MDL	Unsigned
DIVOS	Ri	E	97 – 4	1	– – – –		Step calculation
DIVOU	Ri	E	97 – 5	1	– – – –		32-bit/32-bit = 32-bit
DIV1	Ri	E	97 – 6	d	– C – C		
DIV2	Ri	E	97 – 7	1	– C – C		
DIV3		E	9F – 6	1	– – – –		
DIV4S		E	9F – 7	1	– – – –		
* DIV	Ri *1			–	– C – C	MDL/Ri → MDL, MDL%Ri → MDH	
* DIVU	Ri *2			–	– C – C	MDL/Ri → MDL, MDL%Ri → MDH	Unsigned

*1: DIVOS, DIV1 × 32, DIV2, DIV3 and DIV4S are generated. A total instruction code length of 72 bytes.
*2: DIVOU and DIV1 × 32 are generated. A total instruction code length of 66 bytes.

- **Shift arithmetic instructions (9 instructions)**

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
LSL	Rj, Ri	A	B6	1	C C – C	Ri<<Rj → Ri	Logical shift
* LSL	#u5, Ri	C'	B4	1	C C – C	Ri<<u5 → Ri	
LSL	#u4, Ri	C	B4	1	C C – C	Ri<<u4 → Ri	
LSL2	#u4, Ri	C	B5	1	C C – C	Ri<<(u4 + 16) → Ri	
LSR	Rj, Ri	A	B2	1	C C – C	Ri>>Rj → Ri	Logical shift
* LSR	#u5, Ri	C'	B0	1	C C – C	Ri>>u5 → Ri	
LSR	#u4, Ri	C	B0	1	C C – C	Ri>>u4 → Ri	
LSR2	#u4, Ri	C	B1	1	C C – C	Ri>>(u4 + 16) → Ri	
ASR	Rj, Ri	A	BA	1	C C – C	Ri>>Rj → Ri	Logical shift
* ASR	#u5, Ri	C'	B8	1	C C – C	Ri>>u5 → Ri	
ASR	#u4, Ri	C	B8	1	C C – C	Ri>>u4 → Ri	
ASR2	#u4, Ri	C	B9	1	C C – C	Ri>>(u4 + 16) → Ri	

- **Immediate value data transfer instruction (immediate value set/16-bit/32-bit immediate value transfer instruction) (3 instructions)**

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
LDI: 32	#i32, Ri	E	9F – 8	3	– – – –	i32 → Ri	
LDI: 20	#i20, Ri	C	9B	2	– – – –	i20 → Ri	Upper 12 bits are zero-extended
LDI: 8	#i8, Ri	B	C0	1	– – – –	i8 → Ri	Upper 24 bits are zero-extended
* LDI	# {i8 | i20 | i32}, Ri *1					{i8 | i20 | i32} → Ri	

*1: If an immediate value is given in absolute, assembler automatically makes i8, i20 or i32 selection.
If an immediate value contains relative value or external reference, assembler selects i32.

- **Memory load instructions (13 instructions)**

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
LD	@Rj, Ri	A	04	b	– – – –	(Rj) → Ri	
LD	@(R13, Rj), Ri	A	00	b	– – – –	(R13 + Rj) → Ri	
LD	@(R14, disp10), Ri	B	20	b	– – – –	(R14 + disp10) → Ri	
LD	@(R15, udisp6), Ri	C	03	b	– – – –	(R15 + udisp6) → Ri	
LD	@R15 +, Ri	E	07 – 0	b	– – – –	(R15) → Ri, R15 + = 4	
LD	@R15 +, Rs	E	07 – 8	b	– – – –	(R15) → Rs, R15 + = 4	Rs: Special-purpose register
LD	@R15 +, PS	E	07 – 9	1 + a + b	C C C C	(R15) → PS, R15 + = 4	
LDUH	@Rj, Ri	A	05	b	– – – –	(Rj) → Ri	Zero-extension
LDUH	@(R13, Rj), Ri	A	01	b	– – – –	(R13 + Rj) → Ri	Zero-extension
LDUH	@(R14, disp9), Ri	B	40	b	– – – –	(R14 + disp9) → Ri	Zero-extension
LDUB	@Rj, Ri	A	06	b	– – – –	(Rj) → Ri	Zero-extension
LDUB	@(R13, Rj), Ri	A	02	b	– – – –	(R13 + Rj) → Ri	Zero-extension
LDUB	@(R14, disp8), Ri	B	60	b	– – – –	(R14 + disp8) → Ri	Zero-extension

Note :The relations between o8 field of TYPE-B and u4 field of TYPE-C in the instruction format and assembler description from disp8 to disp10 are as follows:
disp8 → o8 = disp8:Each disp is a code extension.
disp9 → o8 = disp9>>1:Each disp is a code extension.
disp10 → o8 = disp10>>2:Each disp is a code extension.
udisp6 → u4 = udisp6>>2:udisp4 is a 0 extension.

- **Memory store instructions (13 instructions)**

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
ST	Ri, @Rj	A	14	a	– – – –	Ri → (Rj)	Word
ST	Ri, @(R13, Rj)	A	10	a	– – – –	Ri → (R13 + Rj)	Word
ST	Ri, @(R14, disp10)	B	30	a	– – – –	Ri → (R14 + disp10)	Word
ST	Ri, @(R15, udisp6)	C	13	a	– – – –	Ri → (R15 + usidp6)	
ST	Ri, @–R15	E	17 – 0	a	– – – –	R15 – = 4, Ri → (R15)	
ST	Rs, @–R15	E	17 – 8	a	– – – –	R15 – = 4, Rs → (R15)	Rs: Special-purpose register
ST	PS, @–R15	E	17 – 9	a	– – – –	R15 – = 4, PS → (R15)	
STH	Ri, @Rj	A	15	a	– – – –	Ri → (Rj)	Half word
STH	Ri, @(R13, Rj)	A	11	a	– – – –	Ri → (R13 + Rj)	Half word
STH	Ri, @(R14, disp9)	B	50	a	– – – –	Ri → (R14 + disp9)	Half word
STB	Ri, @Rj	A	16	a	– – – –	Ri → (Rj)	Byte
STB	Ri, @(R13, Rj)	A	12	a	– – – –	Ri → (R13 + Rj)	Byte
STB	Ri, @(R14, disp8)	B	70	a	– – – –	Ri → (R14 + disp8)	Byte

Note :The relations between o8 field of TYPE-B and u4 field of TYPE-C in the instruction format and assembler description from disp8 to disp10 are as follows:
disp8 → o8 = disp8:Each disp is a code extension.
disp9 → o8 = disp9>>1:Each disp is a code extension.
disp10 → o8 = disp10>>2:Each disp is a code extension.
udisp6 → u4 = udisp6>>2:udisp4 is a 0 extension.

- **Transfer instructions between registers/special-purpose registers transfer instructions (5 instructions)**

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
MOV	Rj, Ri	A	8B	1	– – – –	Rj → Ri	Transfer between general-purpose registers
MOV	Rs, Ri	A	B7	1	– – – –	Rs → Ri	Rs: Special-purpose register
MOV	Ri, Rs	A	B3	1	– – – –	Ri → Rs	Rs: Special-purpose register
MOV	PS, Ri	E	17 – 1	1	– – – –	PS → Ri	
MOV	Ri, PS	E	07 – 1	c	C C C C	Ri → PS	

- **Non-delay normal branch instructions (23 instructions)**

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
JMP	@Ri	E	97 – 0	2	– – – –	Ri → PC	
CALL	label12	F	D0	2	– – – –	PC + 2 → RP, PC + 2 + rel11 × 2 → PC	
CALL	@Ri	E	97 – 1	2	– – – –	PC + 2 → RP, Ri → PC	
RET		E	97 – 2	2	– – – –	RP → PC	Return
INT	#u8	D	1F	3+3a	– – – –	SSP – = 4, PS → (SSP), SSP – = 4, PC + 2 → (SSP), 0 → I flag, 0 → S flag, (TBR + 3FC – u8 × 4) → PC	
INTE		E	9F – 3	3 + 3a	– – – –	SSP – = 4, PS → (SSP), SSP – = 4, PC + 2 → (SSP), 0 → S flag, (TBR + 3D8 – u8 × 4) → PC	For emulator
RETI		E	97 – 3	2 + 2a	C C C C	(R15) → PC, R15 – = 4, (R15) → PS, R15 – = 4	
BNO	label9	D	E1	1	– – – –	Non-branch	
BRA	label9	D	E0	2	– – – –	PC + 2 + rel8 × 2 → PC	
BEQ	label9	D	E2	2/1	– – – –	PCif Z = = 1	
BNE	label9	D	E3	2/1	– – – –	PCif Z = = 0	
BC	label9	D	E4	2/1	– – – –	PCif C = = 1	
BNC	label9	D	E5	2/1	– – – –	PCif C = = 0	
BN	label9	D	E6	2/1	– – – –	PCif N = = 1	
BP	label9	D	E7	2/1	– – – –	PCif N = = 0	
BV	label9	D	E8	2/1	– – – –	PCif V = = 1	
BNV	label9	D	E9	2/1	– – – –	PCif V = = 0	
BLT	label9	D	EA	2/1	– – – –	PCif V xor N = = 1	
BGE	label9	D	EB	2/1	– – – –	PCif V xor N = = 0	
BLE	label9	D	EC	2/1	– – – –	PCif (V xor N) or Z = = 1	
BGT	label9	D	ED	2/1	– – – –	PCif (V xor N) or Z = = 0	
BLS	label9	D	EE	2/1	– – – –	PCif C or Z = = 1	
BHI	label9	D	EF	2/1	– – – –	PCif C or Z = = 0	

Notes:
- “2/1” in cycle sections indicates that 2 cycles are needed for branch and 1 cycle needed for non-branch.
- The relations between rel8 field of TYPE-D and rel11 field of TYPE-F in the instruction format and assembler discription label9 and label12 are as follows.
  label9 → rel8 = (label9 – PC – 2)/2
  label12 → rel11 = (label12 – PC – 2)/2
- RETI must be operated while S flag = 0.

- **Branch instructions with delays (20 instructions)**

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
JMP:D	@Ri	E	9F – 0	1	– – – –	Ri → PC	
CALL:D	label12	F	D8	1	– – – –	PC + 4 → RP, PC + 2 + rel11 × 2 → PC	
CALL:D	@Ri	E	9F – 1	1	– – – –	PC + 4 → RP, Ri → PC	
RET:D		E	9F – 2	1	– – – –	RP → PC	Return
BNO:D	label9	D	F1	1	– – – –	Non-branch	
BRA:D	label9	D	F0	1	– – – –	PC + 2 + rel8 × 2 → PC	
BEQ:D	label9	D	F2	1	– – – –	PCif Z = = 1	
BNE:D	label9	D	F3	1	– – – –	PCif Z = = 0	
BC:D	label9	D	F4	1	– – – –	PCif C = = 1	
BNC:D	label9	D	F5	1	– – – –	PCif C = = 0	
BN:D	label9	D	F6	1	– – – –	PCif N = = 1	
BP:D	label9	D	F7	1	– – – –	PCif N = = 0	
BV:D	label9	D	F8	1	– – – –	PCif V = = 1	
BNV:D	label9	D	F9	1	– – – –	PCif V = = 0	
BLT:D	label9	D	FA	1	– – – –	PCif V xor N = = 1	
BGE:D	label9	D	FB	1	– – – –	PCif V xor N = = 0	
BLE:D	label9	D	FC	1	– – – –	PCif (V xor N) or Z = = 1	
BGT:D	label9	D	FD	1	– – – –	PCif (V xor N) or Z = = 0	
BLS:D	label9	D	FE	1	– – – –	PCif C or Z = = 1	
BHI:D	label9	D	FF	1	– – – –	PCif C or Z = = 0	

Notes:
- The relations between rel8 field of TYPE-D and rel11 field of TYPE-F in the instruction format and assembler discription label9 and label12 are as follows.
  label9 → rel8 = (label9 – PC – 2)/2
  label12 → rel11 = (label12 – PC – 2)/2
- Delayed branch operation always executes next instruction (delay slot) before making a branch.
- Instructions allowed to be stored in the delay slot must meet one of the following conditions. If the other instruction is stored, this device may operate other operation than defined.
  The instruction described “1” in the other cycle column than branch instruction.
  The instruction described “a”, “b”, “c” or “d” in the cycle column.

- **Direct addressing instructions**

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
DMOV	@dir10, R13	D	08	b	– – – –	(dir10) → R13	Word
DMOV	R13, @dir10	D	18	a	– – – –	R13 → (dir10)	Word
DMOV	@dir10, @R13+	D	0C	2a	– – – –	(dir10) → (R13), R13 + = 4	Word
DMOV	@R13+, @dir10	D	1C	2a	– – – –	(R13) → (dir10), R13 + = 4	Word
DMOV	@dir10, @–R15	D	0B	2a	– – – –	R15 – = 4, (dir10) → (R15)	Word
DMOV	@R15+, @dir10	D	1B	2a	– – – –	(R15) → (dir10), R15 + = 4	Word
DMOVH	@dir9, R13	D	09	b	– – – –	(dir9) → R13	Half word
DMOVH	R13, @dir9	D	19	a	– – – –	R13 → (dir9)	Half word
DMOVH	@dir9, @R13+	D	0D	2a	– – – –	(dir9) → (R13), R13 + = 2	Half word
DMOVH	@R13+, @dir9	D	1D	2a	– – – –	(R13) → (dir9), R13 + = 2	Half word
DMOVB	@dir8, R13	D	0A	b	– – – –	(dir8) → R13	Byte
DMOVB	R13, @dir8	D	1A	a	– – – –	R13 → (dir8)	Byte
DMOVB	@dir8, @R13+	D	0E	2a	– – – –	(dir8) → (R13), R13 + +	Byte
DMOVB	@R13+, @dir8	D	1E	2a	– – – –	(R13) → (dir8), R13 + +	Byte

Note :The relations between the dir field of TYPE-D in the instruction format and the assembler description from disp8 to disp10 are as follows:
disp8 → dir + disp8:Each disp is a code extension
disp9 → dir = disp9>>1:Each disp is a code extension
disp10 → dir = disp10>>2:Each disp is a code extension

- **Resource instructions (2 instructions)**

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
LDRES	@Ri+, #u4	C	BC	a	– – – –	(Ri) → u4 resource Ri + = 4	u4: Channel number
STRES	#u4, @Ri+	C	BD	a	– – – –	u4 resource → (Ri) Ri + = 4	u4: Channel number

- **Co-processor instructions (4 instructions)**

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
COPOP	#u4, #CC, CRj, CRi	E	9F – C	2 + a	– – – –	Calculation	
COPLD	#u4, #CC, Rj, CRi	E	9F – D	1 + 2a	– – – –	Rj → CRi	
COPST	#u4, #CC, CRj, Ri	E	9F – E	1 + 2a	– – – –	CRj → Ri	
COPSV	#u4, #CC, CRj, Ri	E	9F – F	1 + 2a	– – – –	CRj → Ri	No error traps

- **Other instructions (16 instructions)**

Mnemonic	Type	OP	Cycle	N Z V C	Operation	Remarks
NOP	E	9F – A	1	– – – –	No changes	
ANDCCR #u8 ORCCR #u8	D D	83 93	c c	C C C C C C C C	CCR and u8 → CCR CCR or u8 → CCR	
STILM #u8	D	87	1	– – – –	i8 → ILM	Set ILM immediate value
ADDSP #s10 *1	D	A3	1	– – – –	R15 + = s10	ADD SP instruction
EXTSB Ri EXTUB Ri EXTSH Ri EXTUH Ri	E E E E	97 – 8 97 – 9 97 – A 97 – B	1 1 1 1	– – – – – – – – – – – – – – – –	Sign extension 8 → 32 bits Zero extension 8 → 32 bits Sign extension 16 → 32 bits Zero extension 16 → 32 bits	
LDM0 (reglist) LDM1 (reglist) * LDM (reglist) *3	D D	8C 8D	*4 *4 –	– – – – – – – – – – – –	(R15) → reglist, R15 increment (R15) → reglist, R15 increment (R15 + +) → reglist,	Load-multi R0 to R7 Load-multi R8 to R15 Load-multi R0 to R15
STM0 (reglist) STM1 (reglist) * STM2 (reglist) *5	D D	8E 8F	*6 *6 –	– – – – – – – – – – – –	R15 decrement, reglist → (R15) R15 decrement, reglist → (R15) reglist → (R15 + +)	Store-multi R0 to R7 Store-multi R8 to R15 Store-multi R0 to R15
ENTER #u10 *2	D	0F	1+a	– – – –	R14 → (R15 – 4), R15 – 4 → R14, R15 – u10 → R15	Entrance processing of function
LEAVE	E	9F – 9	b	– – – –	R14 + 4 → R15, (R15 – 4) → R14	Exit processing of function
XCHB @Rj, Ri	A	8A	2a	– – – –	Ri → TEMP, (Rj) → Ri, TEMP → (Rj)	For SEMAFO management Byte data

*1: In the ADDSP instruction, the reference between u8 of TYPE-D in the instruction format and assembler description s10 is as follows.
s10 → s8 = s10>>2

*2: In the ENTER instruction, the reference between i8 of TYPE-C in the instruction format and assembler description u10 is as follows.
u10 → u8 = u10>>2

*3: If either of R0 to R7 is specified in reglist, assembler generates LDM0. If either of R8 to R15 is specified, assembler generates LDM1. Both LDM0 and LDM1 may be generated.

*4: The number of cycles needed for execution of LDM0 (reglist) and LDM1 (reglist) is given by the following calculation; $a \times (n - 1) + b + 1$ when “n” is number of registers specified.

*5: If either of R0 to R7 is specified in reglist, assembler generates STM0. If either of R8 to R15 is specified, assembler generates STM1. Both STM0 and STM1 may be generated.

*6: The number of cycles needed for execution of STM0 (reglist) and STM1 (reglist) is given by the following calculation; $a \times n + 1$ when “n” is number of registers specified.

- **20-bit normal branch macro instructions**

Mnemonic		Operation	Remarks
* CALL20	label20, Ri	Next instruction address → RP, label20 → PC	Ri: Temporary register *1
* BRA20	label20, Ri	label20 → PC	Ri: Temporary register *2
* BEQ20	label20, Ri	if (Z = = 1) then label20 → PC	Ri: Temporary register *3
* BNE20	label20, Ri	ifs/Z = = 0	Ri: Temporary register *3
* BC20	label20, Ri	ifs/C = = 1	Ri: Temporary register *3
* BNC20	label20, Ri	ifs/C = = 0	Ri: Temporary register *3
* BN20	label20, Ri	ifs/N = = 1	Ri: Temporary register *3
* BP20	label20, Ri	ifs/N = = 0	Ri: Temporary register *3
* BV20	label20, Ri	ifs/V = = 1	Ri: Temporary register *3
* BNV20	label20, Ri	ifs/V = = 0	Ri: Temporary register *3
* BLT20	label20, Ri	ifs/V xor N = = 1	Ri: Temporary register *3
* BGE20	label20, Ri	ifs/V xor N = = 0	Ri: Temporary register *3
* BLE20	label20, Ri	ifs/(V xor N) or Z = = 1	Ri: Temporary register *3
* BGT20	label20, Ri	ifs/(V xor N) or Z = = 0	Ri: Temporary register *3
* BLS20	label20, Ri	ifs/C or Z = = 1	Ri: Temporary register *3
* BHI20	label20, Ri	ifs/C or Z = = 0	Ri: Temporary register *3

*1: CALL20

(1) If label20 – PC – 2 is between –0x800 and +0x7fe, instruction is generated as follows;

    CALL   label12

(2) If label20 – PC – 2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;

    LDI:20 #label20, Ri
    CALL   @Ri

*2: BRA20

(1) If label20 – PC – 2 is between –0x100 and +0xfe, instruction is generated as follows;

    BRA   label9

(2) If label20 – PC – 2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;

    LDI:20 #label20, Ri
    JMP   @Ri

*3: Bcc20 (BEQ20 to BHI20)

(1) If label20 – PC – 2 is between –0x100 and +0xfe, instruction is generated as follows;

    Bcc   label9

(2) If label20 – PC – 2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;

    Bxcc   false   xcc is a revolt condition of cc
    LDI:20 #label20, Ri
    JMP   @Ri
    false:

- **20-bit delayed branch macro instructions**

Mnemonic	Operation	Remarks
* CALL20:D label20, Ri	Next instruction address + 2 → RP, label20 → PC	Ri: Temporary register *1
* BRA20:D label20, Ri	label20 → PC	Ri: Temporary register *2
* BEQ20:D label20, Ri	if (Z = = 1) then label20 → PC	Ri: Temporary register *3
* BNE20:D label20, Ri	ifs/Z = = 0	Ri: Temporary register *3
* BC20:D label20, Ri	ifs/C = = 1	Ri: Temporary register *3
* BNC20:D label20, Ri	ifs/C = = 0	Ri: Temporary register *3
* BN20:D label20, Ri	ifs/N = = 1	Ri: Temporary register *3
* BP20:D label20, Ri	ifs/N = = 0	Ri: Temporary register *3
* BV20:D label20, Ri	ifs/V = = 1	Ri: Temporary register *3
* BNV20:D label20, Ri	ifs/V = = 0	Ri: Temporary register *3
* BLT20:D label20, Ri	ifs/V xor N = = 1	Ri: Temporary register *3
* BGE20:D label20, Ri	ifs/V xor N = = 0	Ri: Temporary register *3
* BLE20:D label20, Ri	ifs/(V xor N) or Z = = 1	Ri: Temporary register *3
* BGT20:D label20, Ri	ifs/(V xor N) or Z = = 0	Ri: Temporary register *3
* BLS20:D label20, Ri	ifs/C or Z = = 1	Ri: Temporary register *3
* BHI20:D label20, Ri	ifs/C or Z = = 0	Ri: Temporary register *3

*1: CALL20:D
(1) If label20 – PC – 2 is between –0x800 and +0x7fe, instruction is generated as follows;
```
CALL:D  label12
```
(2) If label20 – PC – 2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;
```
LDI:20  #label20, Ri
CALL:D  @Ri
```
*2: BRA20:D
(1) If label20 – PC – 2 is between –0x100 and +0xfe, instruction is generated as follows;
```
BRA:D   label9
```
(2) If label20 – PC – 2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;
```
LDI:20  #label20, Ri
JMP:D   @Ri
```
*3: Bcc20:D (BEQ20:D to BHI20:D)
(1) If label20 – PC – 2 is between –0x100 and +0xfe, instruction is generated as follows;
```
Bcc:D   label9
```
(2) If label20 – PC – 2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;
```
  Bxcc    false         xcc is a revolt condition of cc
  LDI:20  #label20, Ri
  JMP:D   @Ri
false:
```

• **32-bit normal macro branch instructions**

Mnemonic		Operation	Remarks	
* CALL32	label32, Ri	Next instruction address → RP, label32 → PC	Ri: Temporary register	*1
* BRA32	label32, Ri	label32 → PC	Ri: Temporary register	*2
* BEQ32	label32, Ri	if (Z = = 1) then label32 → PC	Ri: Temporary register	*3
* BNE32	label32, Ri	ifs/Z = = 0	Ri: Temporary register	*3
* BC32	label32, Ri	ifs/C = = 1	Ri: Temporary register	*3
* BNC32	label32, Ri	ifs/C = = 0	Ri: Temporary register	*3
* BN32	label32, Ri	ifs/N = = 1	Ri: Temporary register	*3
* BP32	label32, Ri	ifs/N = = 0	Ri: Temporary register	*3
* BV32	label32, Ri	ifs/V = = 1	Ri: Temporary register	*3
* BNV32	label32, Ri	ifs/V = = 0	Ri: Temporary register	*3
* BLT32	label32, Ri	ifs/V xor N = = 1	Ri: Temporary register	*3
* BGE32	label32, Ri	ifs/V xor N = = 0	Ri: Temporary register	*3
* BLE32	label32, Ri	ifs/(V xor N) or Z = = 1	Ri: Temporary register	*3
* BGT32	label32, Ri	ifs/(V xor N) or Z = = 0	Ri: Temporary register	*3
* BLS32	label32, Ri	ifs/C or Z = = 1	Ri: Temporary register	*3
* BHI32	label32, Ri	ifs/C or Z = = 0	Ri: Temporary register	*3

*1: CALL32

(1) If label32 – PC – 2 is between –0x800 and +0x7fe, instruction is generated as follows;

```
CALL    label12
```

(2) If label32 – PC – 2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;

```
LDI:32  #label32, Ri
CALL    @Ri
```

*2: BRA32

(1) If label32 – PC – 2 is between –0x100 and +0xfe, instruction is generated as follows;

```
BRA     label9
```

(2) If label32 – PC – 2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;

```
LDI:32  #label32, Ri
JMP     @Ri
```

*3: Bcc32 (BEQ32 to BHI32)

(1) If label32 – PC – 2 is between –0x100 and +0xfe, instruction is generated as follows;

```
Bcc     label9
```

(2) If label32 – PC – 2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;

```
  Bxcc    false         xcc is a revolt condition of cc
  LDI:32  #label32, Ri
  JMP     @Ri
false:
```

- **32-bit delayed macro branch instructions**

Mnemonic	Operation	Remarks
* CALL32:D label32, Ri	Next instruction address + 2 → RP, label32 → PC	Ri: Temporary register *1
* BRA32:D label32, Ri	label32 → PC	Ri: Temporary register *2
* BEQ32:D label32, Ri	if (Z = = 1) then label32 → PC	Ri: Temporary register *3
* BNE32:D label32, Ri	ifs/Z = = 0	Ri: Temporary register *3
* BC32:D label32, Ri	ifs/C = = 1	Ri: Temporary register *3
* BNC32:D label32, Ri	ifs/C = = 0	Ri: Temporary register *3
* BN32:D label32, Ri	ifs/N = = 1	Ri: Temporary register *3
* BP32:D label32, Ri	ifs/N = = 0	Ri: Temporary register *3
* BV32:D label32, Ri	ifs/V = = 1	Ri: Temporary register *3
* BNV32:D label32, Ri	ifs/V = = 0	Ri: Temporary register *3
* BLT32:D label32, Ri	ifs/V xor N = = 1	Ri: Temporary register *3
* BGE32:D label32, Ri	ifs/V xor N = = 0	Ri: Temporary register *3
* BLE32:D label32, Ri	ifs/(V xor N) or Z = = 1	Ri: Temporary register *3
* BGT32:D label32, Ri	ifs/(V xor N) or Z = = 0	Ri: Temporary register *3
* BLS32:D label32, Ri	ifs/C or Z = = 1	Ri: Temporary register *3
* BHI32:D label32, Ri	ifs/C or Z = = 0	Ri: Temporary register *3

*1: CALL32:D
(1) If label32 – PC – 2 is between –0x800 and +0x7fe, instruction is generated as follows;
    CALL:D label12
(2) If label32 – PC – 2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;
    LDI:32 #label32, Ri
    CALL:D @Ri

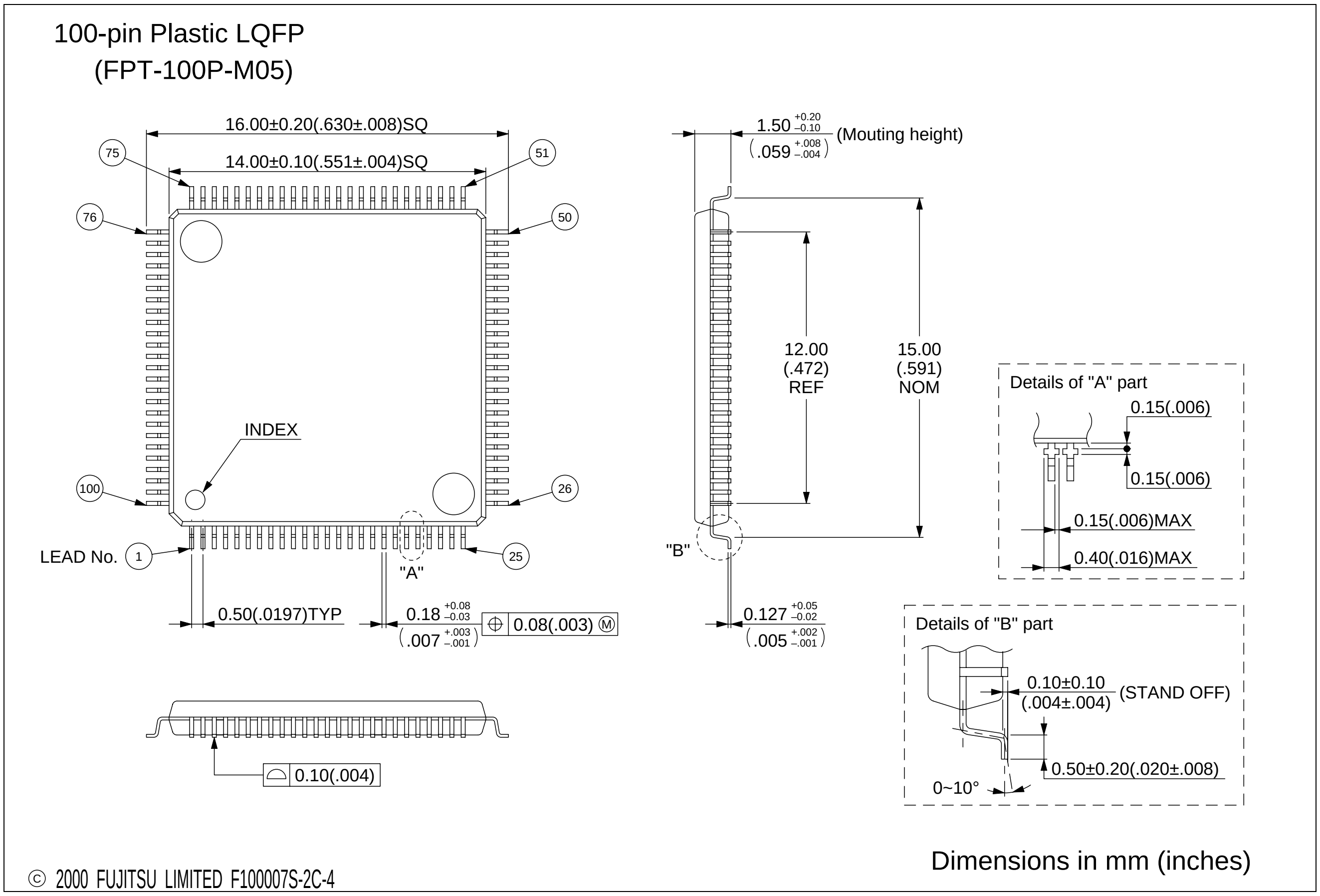
*2: BRA32:D
(1) If label32 – PC – 2 is between –0x100 and +0xfe, instruction is generated as follows;
    BRA:D label9
(2) If label32 – PC – 2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;
    LDI:32 #label32, Ri
    JMP:D @Ri

*3: Bcc32:D (BEQ32:D to BHI32:D)
(1) If label32 – PC – 2 is between –0x100 and +0xfe, instruction is generated as follows;
    Bcc:D label9
(2) If label32 – PC – 2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;
    Bxcc false xcc is a revolt condition of cc
    LDI:32 #label32, Ri
    JMP:D @Ri
    false:

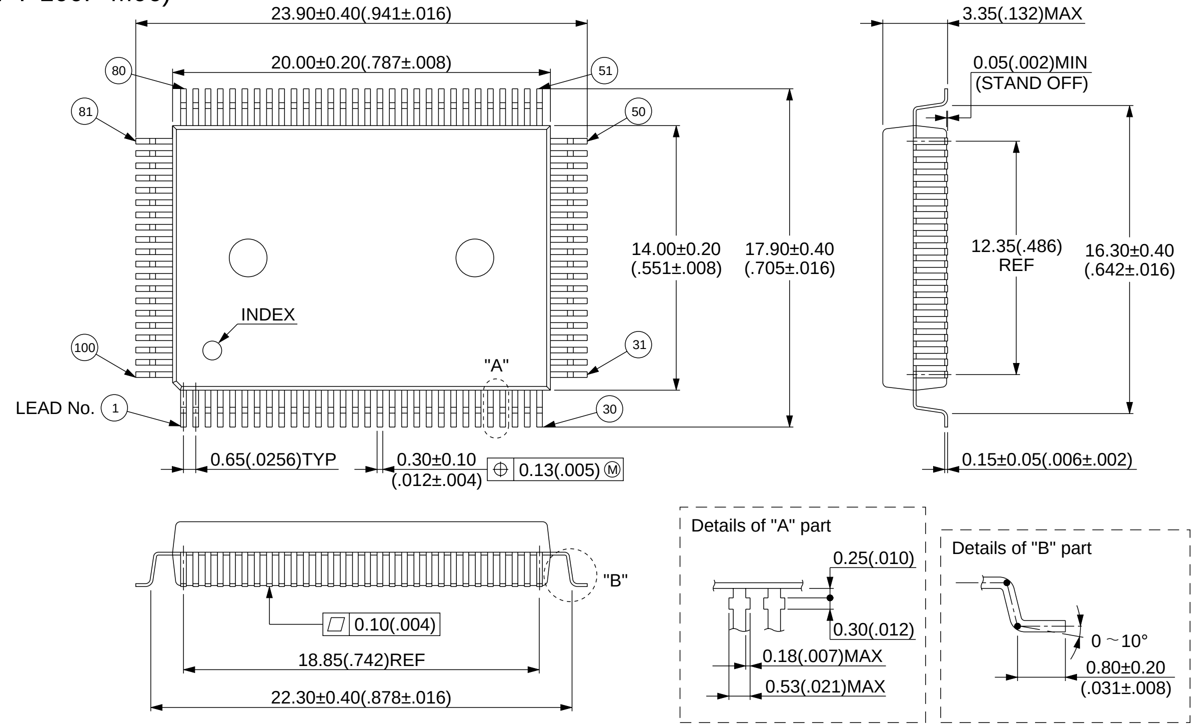
■ ORDERING INFORMATION

Part number	Package	Remarks
MB91F109PFV-XXX	100-pin Plastic LQFP (FPT-100P-M05)	
MB91F109PF-XXX	100-pin Plastic QFP (FPT-100P-M06)	

■ PACKAGE DIMENSIONS



100-pin Plastic QFP
(FPT-100P-M06)



Dimensions in mm (inches)

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