MC145450

Advance Information

CMOS

1200 BAUD
FSK MODEM

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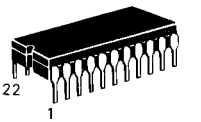
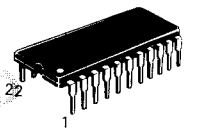
1200 BAUD FSK MODEM

The MC145450 is a silicon-gate CMOS frequency shift keying (FSK) modem intended for use in Bell 202 and CCITT V.23 applications. Features of the device include:

- Bell 202 Compatible 0 to 1800 Baud Main Channel
- 0 to 150 Baud Reverse Channel
- CCITT V.23 Mode 2 Compatible 0 to 1800 Main Channel
- CCITT V.23 0 to 75 Baud Compatible Reverse Channel
- TTL Compatible
- Eight Selectable $\overline{RTS}$-$\overline{CTS}$ Delay Options
- Soft Turn-Off Capability
- Answer Back Tone Generator (US and CCITT Tones)
- Carrier Detect Input
- 22 Pin Package

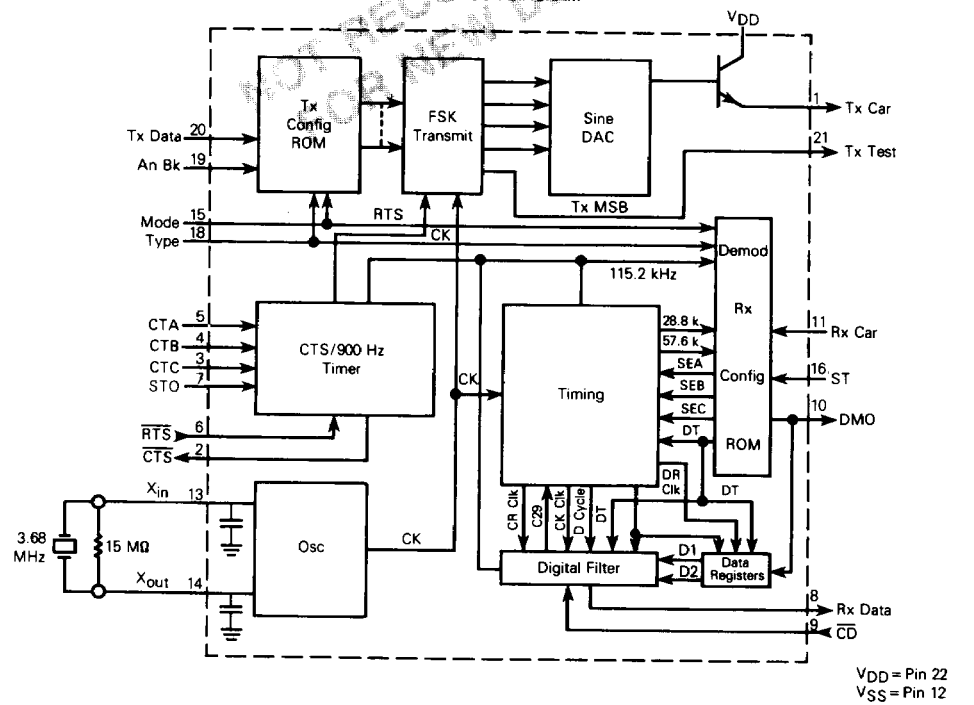


L SUFFIX
CERAMIC PACKAGE
CASE 736



P SUFFIX
PLASTIC PACKAGE
CASE 708

MC145450 1200 BAUD FSK MODEM
BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

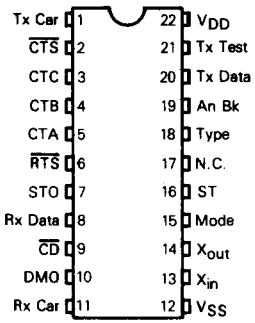
ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	10	V
Input Voltages, All Inputs	V_{in}	$V_{SS}-0.5$ to $V_{DD}+0.5$	V
DC Current Drain per Pin Pin 3-6, 9, 15, 16, 18, 19, 20 Pins 2, 8	I_{out}	 10 35	mA
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	$V_{DD}-V_{SS}$	4.5	5.0	6.5	V

PIN ASSIGNMENTS



DC ELECTRICAL CHARACTERISTICS ($V_{DD}=5.0$ V ±5%, $V_{SS}=0$, $T_A=0$ to 70°C)

Characteristics	Symbol	Min	Typ	Max	Unit
Input High Voltage	V_{IH}				V
Pins 3-7, 9, 15, 16, 18, 19, 20	—	2.8	—	—	
Pin 13, 11	—	4.0	—	—	
Input Low Voltage	V_{IL}				V
Pins 3-7, 9, 15, 16, 18, 19, 20		—	—	0.5	
Pin 13, 11		—	—	0.6	
Input Current	I_{in}				μA
All Inputs (V_{IL} 0 V)		—	—	−5.0	
All Inputs Except Pins 11, 13, ($V_{IH}>2.8$ V) (Note 1)		—	—	600	
Output High Current ($V_{OH}=2.4$ V)	I_{OH}				mA
Pins 2, 8 (Test Load A)		0.75	—	—	
Pins 10, 21 (Test Load B)		0.75	—	—	
Output Low Current ($V_{OL}=0.4$ V)	I_{OL}				mA
Pins 2, 8 (Test Load A)		1.2	—	—	
Pins 10, 21 (Test Load B)		0.6	—	—	
Operating Current	I_{DD}	—	2.5	6	mA
Input Capacitance	C_{in}				pF
All Except Pin 13		—	—	12	
Pin 13 (X_{in})		—	8	—	
Output Capacitance	C_{out}				pF
All Except Pin 14		—	—	12	
Pin 14 (X_{out})		—	13	—	
Transmit Audio Signal Level (Pin 1 $R_L=10$ kΩ (Note 2)	—	0.428	0.5	0.578	Vp-p
Total Harmonic Distortion (2nd to 14th) (Note 2)	THD	—	−50	−40	dB

AC ELECTRICAL CHARACTERISTICS ($V_{DD}=5.0$ V ±5%, $V_{SS}=0$, $T_A=0$ to 70°C)

Characteristics		Symbol	Min	Typ	Max	Unit
Output Rise Time (Test Load A) (Pins 2, 8)		t_r	—	20	100	ns
Output Rise Time (Test Load B) (Pins 10, 14, 21)		t_r	—	20	100	ns
Output Fall Time (Test Load A) (Pins 2, 8)		t_f	—	20	100	ns
Output Fall Time (Test Load B) (Pins 10, 14, 21)		t_f	—	20	100	ns
Input Rise and Fall Times (Except Pin 13)		t_r, t_f	—	—	1000	μs
Delay From $\overline{RTS}$ to $\overline{CTS}$	STO = Low	$t_{d(low)}$	—	1	—	μs
Delay From $\overline{RTS}$ to $\overline{CTS}$	STO = High	$t_{d(high)}$	18.3	—	21.7	ms

NOTES:

1. Active pull-up devices are used on these inputs to allow interfacing to TTL devices. The I_{in} specified is a transitional load (not steady state) which is drawn when the input is brought up to 2.8 V until the internal pull-up device has raised the signal to the V_{DD} level.
2. Measured in any mode using HP-3555B dB meter (or equivalent) with 3 kHz flat filtering.

PIN DESCRIPTIONS

V_{DD}, POSITIVE POWER SUPPLY (PIN 22)
This is nominally 5.0 V.

V_{SS}, NEGATIVE POWER SUPPLY (PIN 12)
This is usually 0 volts.

Tx Car, TRANSMIT CARRIER (PIN 1)
The transmit carrier output is a 16 step digitally-synthesized sine wave with an amplitude of 0.1 V_{DD} (p-p) (±10%) and offset by a dc bias of 0.5 V_{DD} (±10%). The output load should be 10 kilohms or greater.

$\overline{CTS}$, CLEAR TO SEND (PIN 2)
The clear to send output goes low in response to a high-to-low translation of $\overline{RTS}$ following a selected delay (see CTA, CTB, CTC pin description). This output goes high immediately after loss of $\overline{RTS}$. During the time following activation of $\overline{RTS}$ and before the activation of $\overline{CTS}$, Tx Data should be held in the mark condition.

CTA, CLEAR TO SEND SELECT A (PIN 5)
CTB, CLEAR TO SEND SELECT B (PIN 4)
CTC, CLEAR TO SEND SELECT C (PIN 3)

For delay times for clear to send delay select inputs, see Table 1.

$\overline{RTS}$, REQUEST TO SEND (PIN 6)
The request to send input controls data transmission from the modulator. A low level enables the modulator output and a high level will disable the modulator. See Figure 1.

STO, SOFT TURN OFF INPUT (PIN 7)
Activation of STO causes a 900 Hz tone to be transmitted and $\overline{CTS}$ to remain active for 20 ms following the loss of $\overline{RTS}$. See Figure 5.

Rx Data, RECEIVE DATA (PIN 8)
The receive data output is the serial data output from the demodulator. Rx Data is clamped high when $\overline{CD}$ is not active.

$\overline{CD}$, CARRIER DETECT (PIN 9)
When carrier detect input is high (1), the Rx Data output will be clamped to a high state. When carrier detect is low (0), Rx Data output demodulates the Rx carrier input signal.

DMO, DEMODULATOR OUTPUT (PIN 10)
The demodulator output is the output of the differential delay detector. It is used for production testing of the demodulator. In normal operation, this pin should be left open.

Rx Car, RECEIVER CARRIER (PIN 11)
The receiver carrier input is the FSK input to the demodulator. This signal should be the hard-limited output of the receive filter, nominally 50%.

X_{in}, OSCILLATIOR INPUT (PIN 13)
X_{out}, OSCILLATOR OUTPUT (PIN 14)
X_{in} should be driven from either an AT-cut crystal or a digital signal source at 3.6864 MHz ±0.01%. When driven by a crystal, a 15 megohm resisitor should be connected from X_{in} to X_{out} in parallel with the crystal.

MODE (PIN 15)
The mode pin selects the pair of frequencies used during modulation and demodulation. A "0" on this pin selects forward channel operation; i.e. high-speed transmit and low-speed receive. A "1" on this pin selects reverse channel operation; i.e. low-speed transmit and high-speed receive.

ST, SELF TEST (PIN 16)
When a high level is placed on this pin, the demodulator is switched to the modulator frequencies and baud rate (as determined by Mode and Type pins). The modulator should be looped back through the receive filter to the demodulator for self test (echo back).

N.C. NO CONNECTION (PIN 17)
This pin is not bonded internally and should be left open in normal operation.

TYPE (PIN 18)
This pin is used to select Bell 202 type operation and CCITT V.23 operation. When the type input pin is a "1", Bell operation is selected. When the type input pin is a "0", the CCITT standard is selected.

An Bk, ANSWER BACK (PIN 19)
The answer back input causes the answer back tone to be transmitted. The answer back tone is 2025 Hz for the Bell mode and 2100 Hz for the CCITT modes. When a high level is placed on the An Bk input pin, the Tx Car pin will output an answer back tone and $\overline{CTS}$ will go to a high state, regardless of the state of $\overline{RTS}$ (see Figure 1).

Tx Data, TRANSMIT DATA (PIN 20)
The transmit data input is the serial input to the modulator. A high level causes a mark frequency to be transmitted, a low level causes a space frequency to be transmitted.

Tx Test, TRANSMIT TEST (PIN 21)
The transmit test output is a square wave representation of the modulator transmit frequency. It is used for test purposes and should be left open in normal operation.

FIGURE 1 – An Bk AND $\overline{RTS}$-$\overline{CTS}$ TIMING

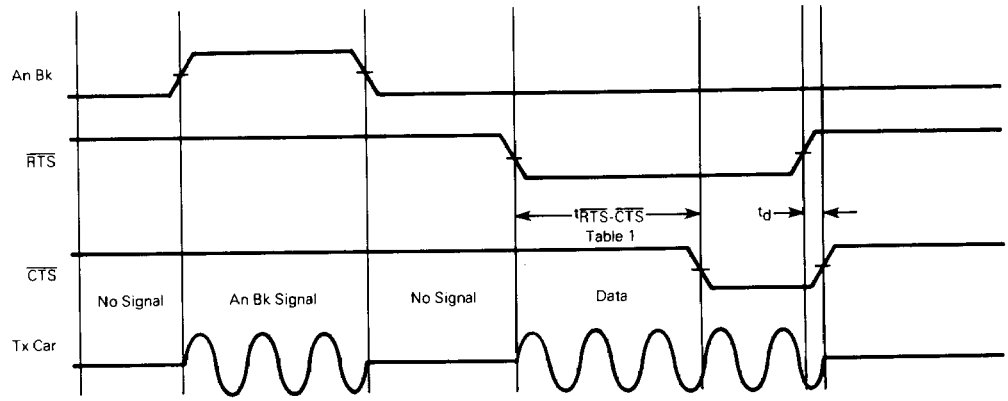


TABLE 1 – $\overline{RTS}$-$\overline{CTS}$ DELAY TIMES

CTC	CTB	CTA	Delay*
0	0	0	0 ms
0	0	1	26.7 ms
0	1	0	40.0 ms
0	1	1	60.0 ms
1	0	0	133.3 ms
1	0	1	213.3 ms
1	1	0	266.7 ms
1	1	1	426.6 ms

* All delays are ± 1.7 ms.

TABLE 2 – OPERATING MODES

Type	Mode	Transmit Data	Transmit Frequency Spec	Transmit Frequency Actual	Answer Back Tone	Application
0	0	0	2100	2099.32	2100	CCITT V.23 75 Baud Receive 1200 Baud Transmit Forward Channel
		1	1300	1299.86		
0	1	0	450	450	2100	CCITT V.23 1200 Baud Receive 75 Baud Transmit Reverse Channel
		1	390	390.5		
1	0	0	2200	2199.52	2025	U.S. 150 Baud Receive 1200 Baud Transmit (Bell 202) Forward Channel
		1	1200	1200		
1	1	0	510	509.73	390	U.S. 1200 Baud Receive (Bell 202) 150 Baud Transmit Reverse Channel
		1	390	390.5		

Data = 0 = Space
= 1 = Mark

* Crystal Frequency = 3.6864 MHz

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FIGURE 2 – STO TIMING

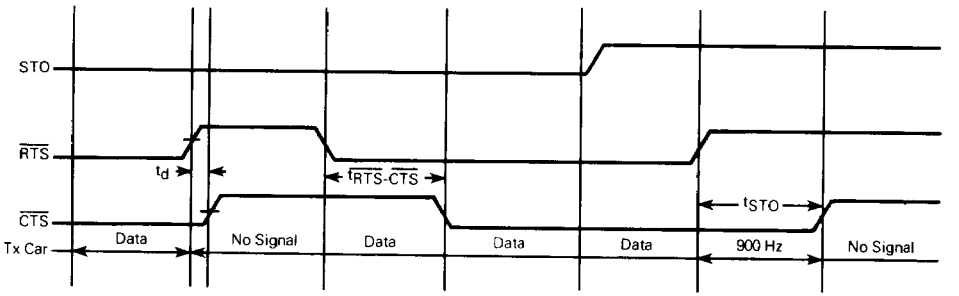
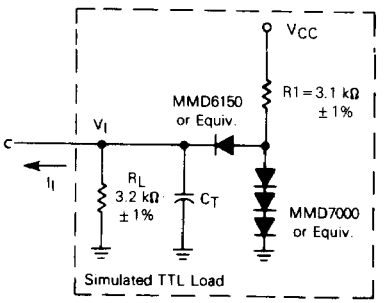
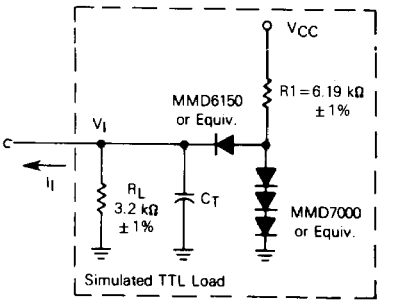


FIGURE 3 – OUTPUT TEST LOAD A



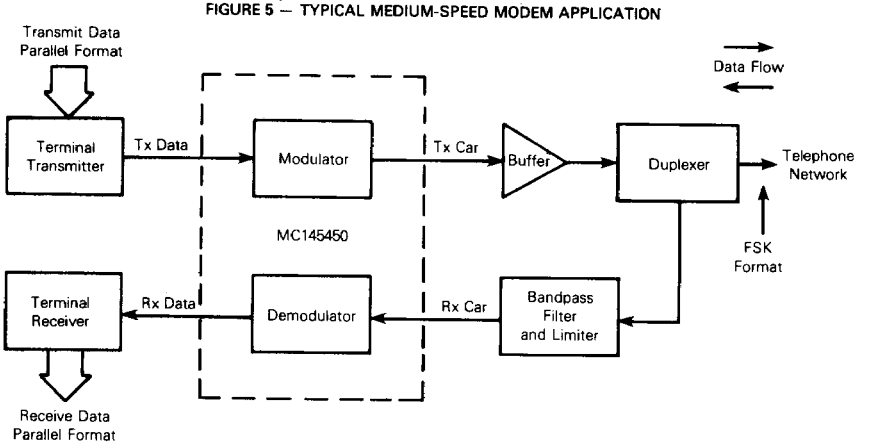
C_T = 20 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

FIGURE 4 – OUTPUT TEST LOAD B



C_T = 20 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

FIGURE 5 – TYPICAL MEDIUM-SPEED MODEM APPLICATION



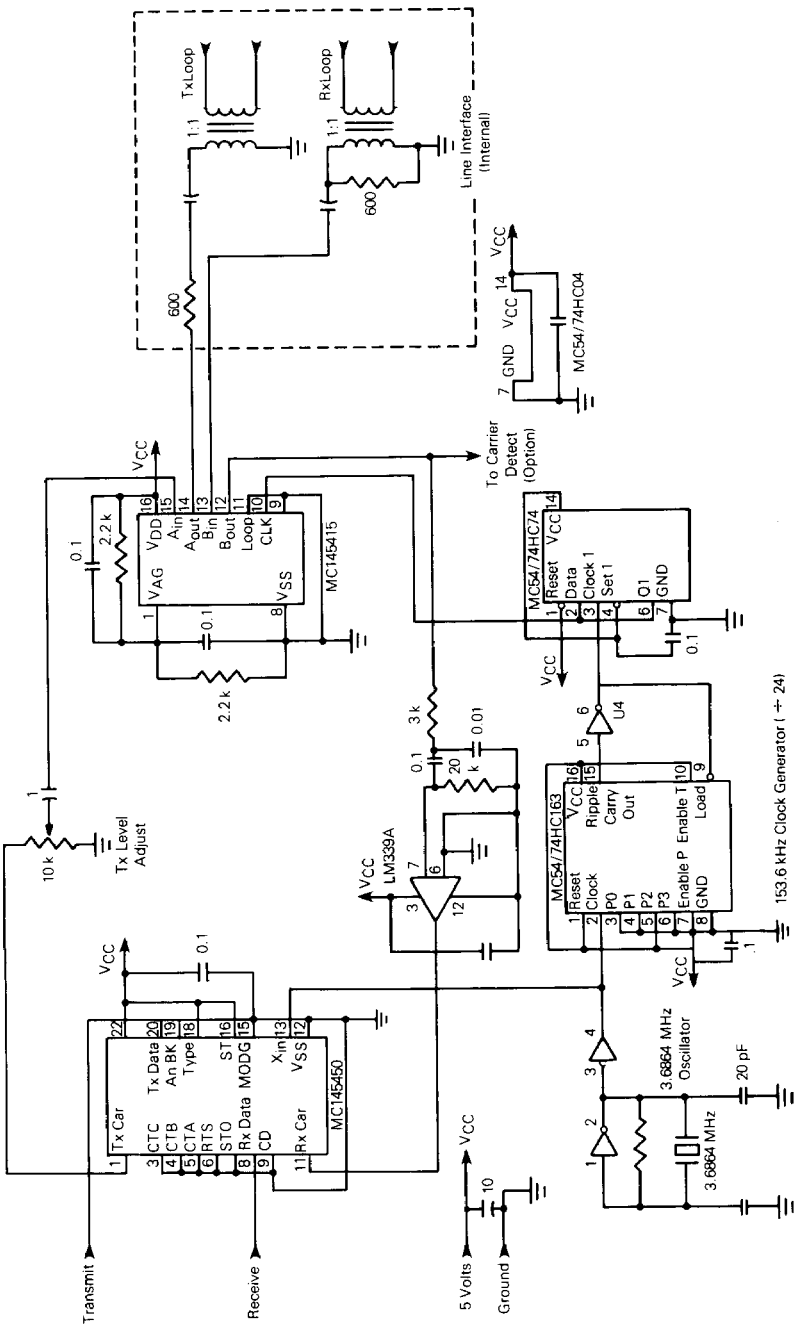


FIGURE 6 -- TYPICAL 1200 BAUD 4 WIRE MODEM APPLICATION