

MC33290

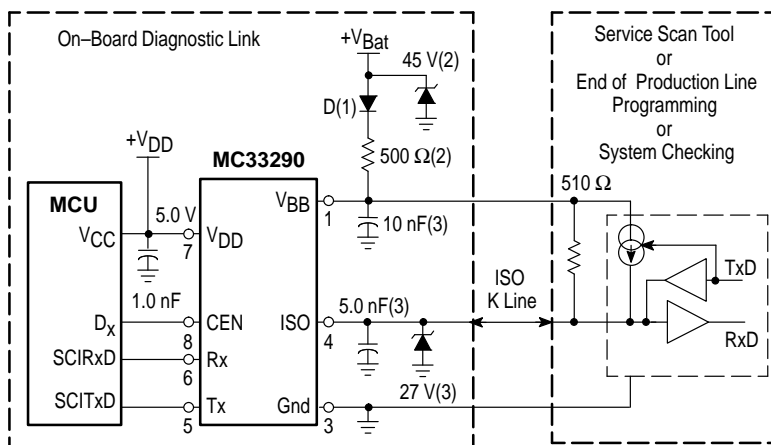
Advance Information ISO Serial Link Interface

The MC33290 is a serial link bus interface device designed to provide bi-directional half-duplex communication interfacing in automotive diagnostic applications. It is designed to interface between the vehicle's on-board microcontroller and systems off-board the vehicle via the special ISO K line. The MC33290 is designed to meet the "Diagnostic Systems ISO9141" specification. The device's K line bus driver's output is fully protected against bus shorts and over temperature conditions.

The MC33290 derives its robustness to temperature and voltage extremes from being built on a SMARTMOS™ process, incorporating CMOS logic, bipolar/MOS analog circuitry, and DMOS power FETs. Though the MC33290 was principally designed for automotive applications, it is suited for other serial communication applications. It is parametrically specified over an ambient temperature range of $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ and $8.0\text{ V} \leq V_{\text{Bat}} \leq 18\text{ V}$ supply. The economical 8 pin DIP and SO-8 surface mount plastic packages make the MC33290 very cost effective.

- Designed to Operate Over Wide Supply Voltage of 8.0 to 18 V
- Ambient Operating Temperature of -40°C to 125°C
- Interfaces Directly to Standard CMOS Microprocessors
- ISO K Line Pin Protected Against Shorts to Ground
- Thermal Shutdown with Hysteresis
- Maximum Transmission Speeds in Excess of 50 k Baud
- ISO K Line Pin Capable of High Currents
- ISO K Line can be Driven with up to 10 nF of Parasitic Capacitance
- 8.0 kV ESD Protection Attainable with Few Additional Components
- Standby Mode: No V_{Bat} Current Drain with V_{DD} at 5.0 V
- Low Current Drain during Operation with V_{DD} at 5.0 V

Typical Application Schematic

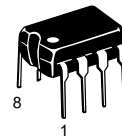


Components Necessary for: Reverse Battery (1), Overvoltage Transient (2), and 8.0 kV ESD Protection (3) in a metal module case.

This device contains 85 active transistors.

ISO SERIAL LINK INTERFACE

SEMICONDUCTOR TECHNICAL DATA

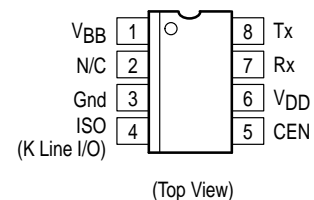


P SUFFIX
PLASTIC PACKAGE
CASE 626



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

PIN CONNECTIONS

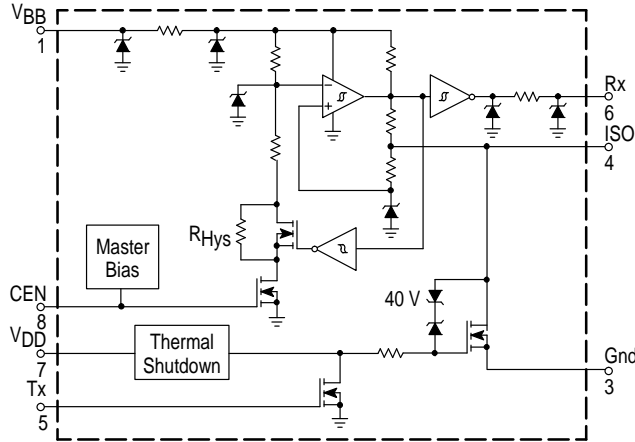


ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33290D	$T_A = -40^{\circ}\text{ to } +125^{\circ}\text{C}$	SO-8
MC33290P		DIP-8

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Figure 1. Simplified Block Diagram



MAXIMUM RATINGS (All voltages are with respect to ground, unless otherwise noted.)

Rating	Symbol	Value	Unit
V _{DD} DC Supply Voltage	V _{DD}	-0.3 to 7.0	V
V _{BB} Load Dump Peak Voltage	V _{BB(LD)}	45	V
ISO Pin Load Dump Peak Voltage	V _{ISO}	40	V
ISO Short Circuit Current Limit	I _{ISO(LIM)}	1.0	A
ESD Voltage (Note 1)			V
Human Body Model (Note 2)	V _{ESD1}	2000	
Machine Model (Note 3)	V _{ESD2}	200	
ISO Clamp Energy (Note 4)	E _{clamp}	10	mJ
Storage Temperature	T _{stg}	-55 to +150	°C
Operating Case Temperature	T _C	-40 to +125	°C
Operating Junction Temperature	T _J	-40 to +150	°C
Power Dissipation (T _A = 25°C)	P _D	0.8	W
Soldering Temperature (for 10 seconds)	T _{solder}	260	°C
Thermal Resistance (Junction-to-Ambient)	R _{θJA}	150	°C/W

- NOTES:** 1. ESD data available upon request.
 2. Testing in accordance with Human Body Model (C_{Zap} = 100 pF, R_{Zap} = 1500 Ω).
 3. Testing in accordance with Machine Model (C_{Zap} = 100 pF, R_{Zap} = 0 Ω).
 4. Non-repetitive clamping capability at 25°C.

ELECTRICAL CHARACTERISTICS (Characteristics noted under conditions of 4.75 V ≤ V_{DD} ≤ 5.25 V, 8.0 V ≤ V_{BB}, HSIP ≤ 18.0 V, -40°C ≤ T_C ≤ 125°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
POWER AND CONTROL					
V _{DD} Sleep State Current (HSIM = HSIP, LSIM = LSIP = 0 V, VRSM = VRSP = 0 V, Tx = 0.8 V _{DD} , CEN = 0.3 V _{DD})	I _{DD(SS)}	-	-	0.1	mA
V _{DD} Quiescent Operating Current (HSIM = HSIP - 0.3 V, LSIM = 0 V, LSIP = 0.3 V, VRSM = 0 V, VRSP = -0.5 V, Tx = 0.2 V _{DD} , CEN = 0.7 V _{DD})	I _{DD(Q)}	-	-	1.0	mA
V _{BB} Sleep State Current (V _{BB} = 16 V, HSIM = HSIP, LSIM = LSIP = 0 V, VRSM = VRSP = 0 V, Tx = 0.8 V _{DD} , CEN = 0.3 V _{DD})	I _{BB(SS)}	-	-	50	μA
V _{BB} Quiescent Operating Current (HSIM = HSIP - 0.3 V, LSIM = 0 V, LSIP = 0.3 V, VRSM = 0 V, VRSP = -0.5 V, Tx = 0.2 V _{DD} , CEN = 0.7 V _{DD})	I _{BB(Q)}	-	-	1.0	mA
Chip Enable					V
Input High Voltage Threshold (Note 1)	V _{IH(CEN)}	0.7 V _{DD}	-	-	
Input Low Voltage Threshold (Note 2)	V _{IL(CEN)}	-	-	0.3 V _{DD}	

- NOTES:** 1. When I_{BB} transitions to >100 μA.
 2. When I_{BB} transitions to <100 μA.

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ELECTRICAL CHARACTERISTICS (continued) (Characteristics noted under conditions of $4.75\text{ V} \leq V_{DD} \leq 5.25\text{ V}$, $8.0\text{ V} \leq V_{BB}$, $HSIP \leq 18.0\text{ V}$, $-40^{\circ}\text{C} \leq T_C \leq 125^{\circ}\text{C}$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
POWER AND CONTROL					
Chip Enable Pull-Down Current (Note 3)	$I_{PD}(CEN)$	2.0	–	40	μA
Tx Input Low Voltage Threshold ($R_{ISO} = 510\ \Omega$) (Note 4)	$V_{LTP}(Tx)$	–	–	$0.3 \times V_{DD}$	V
Tx Input High Voltage Threshold ($R_{ISO} = 510\ \Omega$) (Note 5)	$V_{UTP}(Tx)$	$0.7 \times V_{DD}$	–	–	V
Tx Pull-Up Current (Note 6)	$I_{PU}(Tx)$	–40	–	–2.0	μA
Rx Output Low Voltage Threshold ($R_{ISO} = 510\ \Omega$, Tx = $0.2 V_{DD}$, Rx Sinking 1.0 mA)	$V_L(Rx)$	–	–	$0.2 V_{DD}$	V
Rx Output High Voltage Threshold ($R_{ISO} = 510\ \Omega$, Tx = $0.8 V_{DD}$, Rx Sourcing 250 μA)	$V_H(Rx)$	$0.8 V_{DD}$	–	–	V
Thermal Shutdown (Note 7)	T_{LIM}	150	170	–	$^{\circ}\text{C}$

- NOTES**
3. Enable pin has an internal current pull-down equivalent to greater than 50 k Ω .
 4. Measured by ramping Tx down from $0.7 V_{DD}$ to $0.3 V_{DD}$ and noting Tx value at which ISO falls below $0.2 V_{BB}$.
 5. Measured by ramping Tx up from $0.3 V_{DD}$ to $0.7 V_{DD}$ and noting the value at which ISO rises above $0.9 V_{BB}$.
 6. Tx pin has internal current pull-up equivalent to greater than 50 k Ω . Pull-Up current measure with Tx pin at $0.7 V_{DD}$.
 7. Thermal Shutdown performance (T_{LIM}) is guaranteed by design but not production tested.

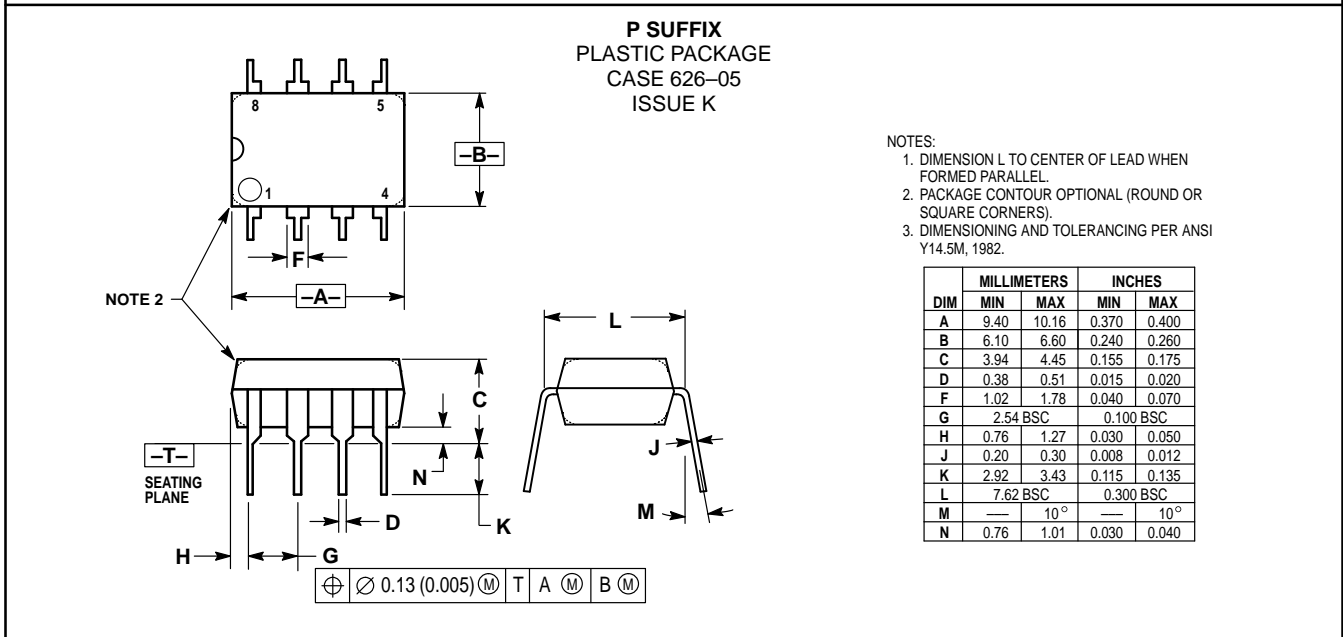
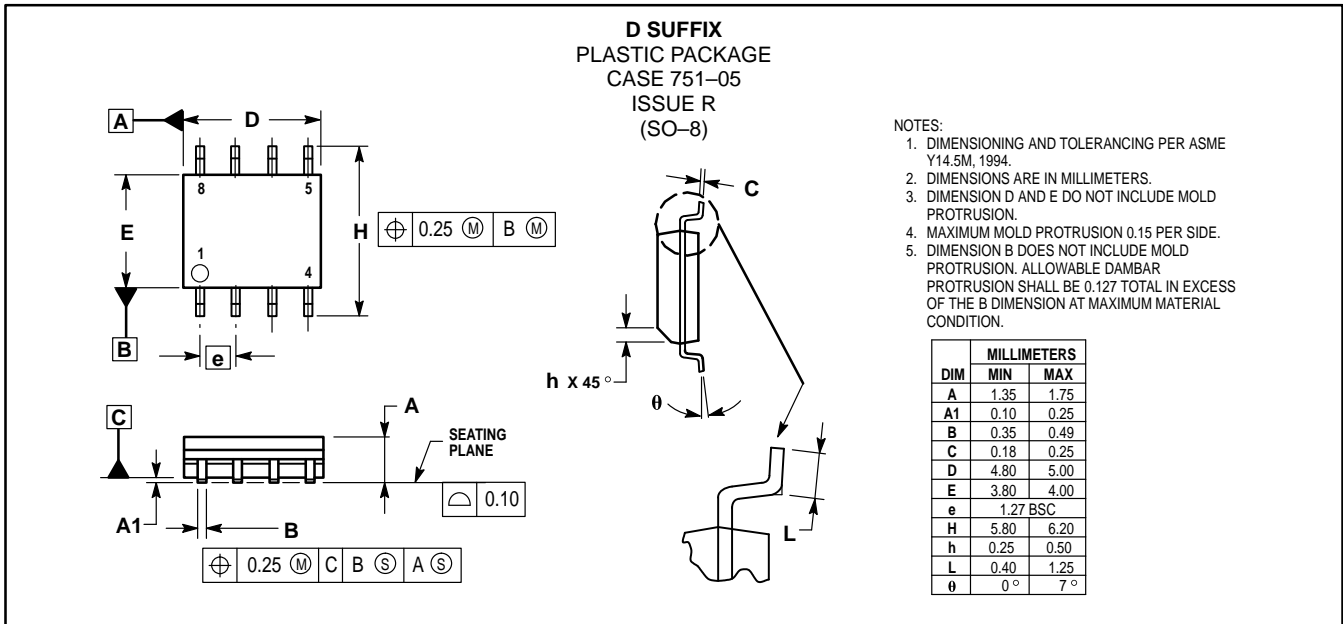
ELECTRICAL CHARACTERISTICS (Characteristics noted under conditions of $4.75\text{ V} \leq V_{DD} \leq 5.25\text{ V}$, $8.0\text{ V} \leq V_{BB}$, $HSIP \leq 18.0\text{ V}$, $-40^{\circ}\text{C} \leq T_C \leq 125^{\circ}\text{C}$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ISO I/O					
Input Low Voltage Threshold ($R_{ISO} = 0\ \Omega$, Tx = $0.8 V_{DD}$) (Note 1)	$V_{LTP}(ISO)$	–	–	$0.4 \times V_{BB}$	V
Input High Voltage Threshold ($R_{ISO} = 0\ \Omega$, Tx = $0.8 V_{DD}$) (Note 2)	$V_{UTP}(ISO)$	$0.8 \times V_{BB}$	–	–	V
Input Hysteresis (Note 3)	$V_{Hys}(ISO)$	$0.01 \times V_{BB}$	–	$0.1 \times V_{BB}$	V
Internal Pull-Up Current (Note 4) ($R_{ISO} = \infty\ \Omega$, Tx = $0.8 V_{DD}$, $V_{ISO} = 0.5 V_{BB}$)	$I_{PU}(ISO)$	–5.0	–	–90	μA
Short Circuit Current Limit (Note 5) ($R_{ISO} = 0\ \Omega$, Tx = $0.4 V_{DD}$, $V_{ISO} = V_{BB}$)	$I_{SC}(ISO)$	50	–	1000	mA
Output Low Voltage Threshold ($R_{ISO} = 510\ \Omega$, Tx = $0.2 V_{DD}$)	$V_L(ISO)$	–	–	$0.125 \times V_{BB}$	V
Output High Voltage Threshold ($R_{ISO} = \infty\ \Omega$, Tx = $0.8 V_{DD}$)	$V_H(ISO)$	$0.95 \times V_{BB}$	–	–	V
Fall Time (Note 6) ($R_{ISO} = 510\ \Omega$ to V_{BB} , $C_{ISO} = 10\text{ nF}$ to Ground)	$t_{fall}(ISO)$	–	–	2.0	μs
ISO Propagation Delay (Note 7) High to Low; ($R_{ISO} = 510\ \Omega$, $C_{ISO} = 500\text{ pF}$) (Note 8) Low to High; ($R_{ISO} = 510\ \Omega$, $C_{ISO} = 500\text{ pF}$) (Note 9)	$t_{PD}(ISO)$	–	–	2.0 2.0	μs

- NOTES:**
1. ISO ramped from $0.8 V_{BB}$ to $0.4 V_{BB}$, Monitor Rx, Value of ISO voltage at which Rx transitions to $0.3 V_{DD}$.
 2. ISO ramped from $0.4 V_{BB}$ to $0.8 V_{BB}$, Monitor Rx, Value of ISO voltage at which Rx transitions to $0.7 V_{DD}$.
 3. Input Hysteresis, $V_{Hys}(ISO) = V_{UTP}(ISO) - V_{LTP}(ISO)$.
 4. ISO Pull-Up has >100 k Ω internal pull-up to V_{BB} .
 5. ISO has internal current limit.
 6. Time required ISO voltage to transition from $0.8 V_{BB}$ to $0.2 V_{BB}$.
 7. Changes in the value of C_{ISO} affect the rise and fall time but have minimal effect on Propagation Delay.
 8. Step Tx voltage from $0.2 V_{DD}$ to $0.8 V_{DD}$; Time measured from $V_{UTP}(ISO)$ until V_{ISO} reaches $0.3 V_{BB}$.
 9. Step Tx voltage from $0.8 V_{DD}$ to $0.2 V_{DD}$; Time measured from $V_{LTP}(ISO)$ until V_{ISO} reaches $0.7 V_{BB}$.

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