



Integrated Device Technology, Inc.

# 16-BIT 2:1 MUX/DEMUX SWITCH

**IDT74FST163233  
ADVANCE INFORMATION**

## FEATURES:

- Bus switches provide zero delay paths
- Extended commercial range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- Low switch on-resistance:  
FST163xxx –  $7\Omega$
- TTL-compatible input and output levels
- ESD > 2000V per MIL-STD-883, Method 3015;  
> 200V using machine model (C = 200pF, R = 0)
- Available in SSOP, TSSOP and TVSOP

## DESCRIPTION:

The FST163233 belongs to IDT's family of Bus switches. Bus switch devices perform the function of connecting or isolating two ports without providing any inherent current sink or source capability. Thus they generate little or no noise of

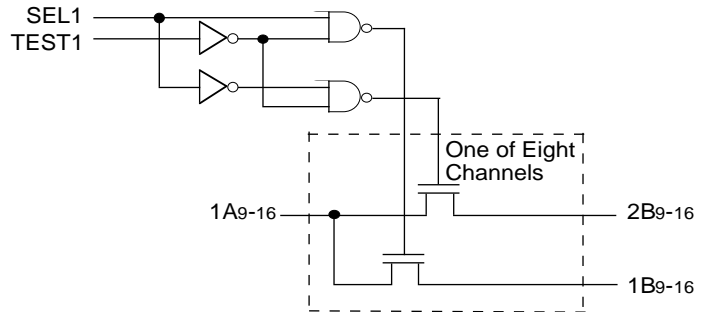
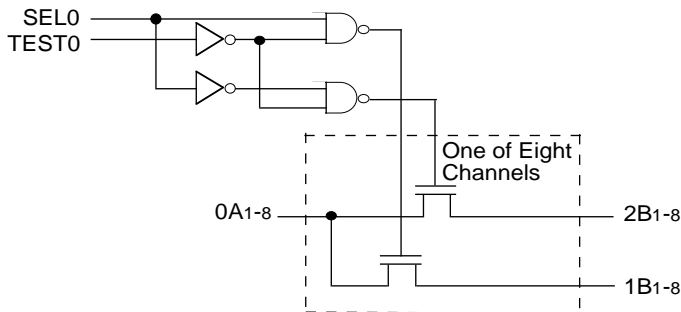
their own while providing a low resistance path for an external driver. These devices connect input and output ports through an n-channel FET. When the gate-to-source junction of this FET is adequately forward-biased the device conducts and the resistance between input and output ports is small. Without adequate bias on the gate-to-source junction of the FET, the FET is turned off, therefore with no VCC applied, the device has hot insertion capability.

The low on-resistance and simplicity of the connection between input and output ports reduces the delay in this path to close to zero.

The FST163233 provides three 16-bit TTL-compatible ports that support 2:1 multiplexing. The SEL<sub>0,1</sub> and TEST<sub>0,1</sub> pins provide switch enable and mux select control as shown below.

The A port can be connected to port 1B or port 2B or both ports 1B and 2B.

## FUNCTIONAL BLOCK DIAGRAM



3512 drw 01

## PIN DESCRIPTION

Pin Names	I/O	Description
A, 1B, 2B	I/O	Buses A, 1B, 2B
SEL <sub>0-1</sub> , TEST <sub>0-1</sub>	I	Control Pins for Mux and Switch Enable Functions

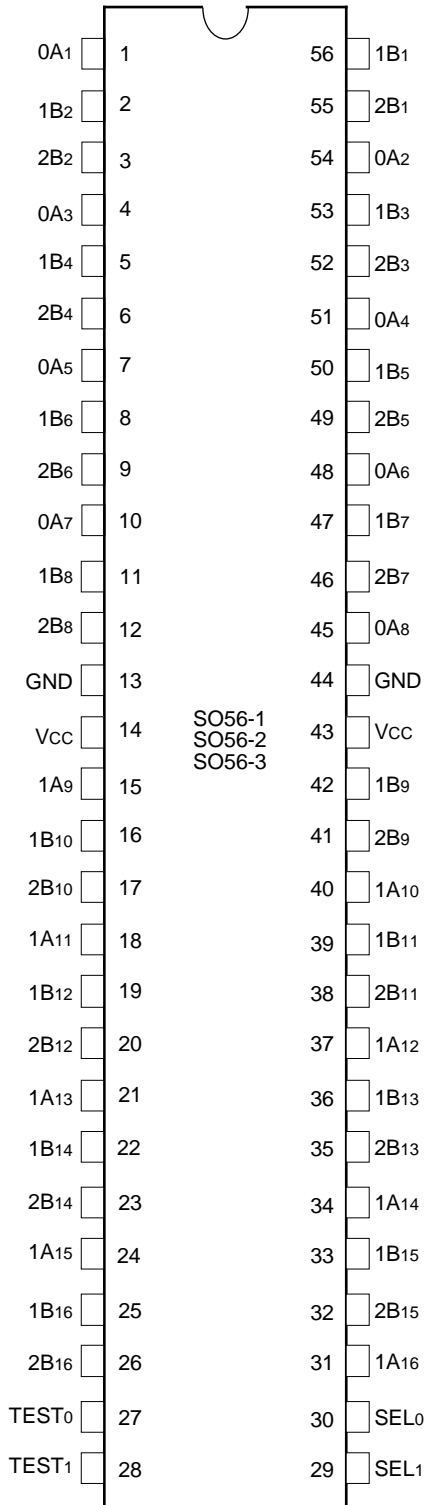
3512 tbl 01

The IDT logo is a registered trademark of Integrated Device Technology, Inc.

**COMMERCIAL TEMPERATURE RANGE**

**AUGUST 1996**

**PIN CONFIGURATION**



**SSOP/  
TSSOP/TVSOP  
TOP VIEW**

3512 drw 02

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Description	Max.	Unit
VTERM <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	Maximum Continuous Channel Current	128	mA

**NOTES:**

3512 tbl 02

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Vcc, Control and Switch terminals.

**CAPACITANCE<sup>(1)</sup>**

Symbol	Parameter	Conditions <sup>(2)</sup>	Typ.	Unit
CIN	Control Input Capacitance		4	pF
C <sub>I/O</sub>	Switch Input/Output Capacitance	Switch Off		pF

**NOTES:**

3512 tbl 03

- Capacitance is characterized but not tested
- T<sub>A</sub> = 25°C, f = 1MHz, V<sub>IN</sub> = 0V, V<sub>OUT</sub> = 0V

**FUNCTION TABLE**

SEL <sub>0</sub>	TEST <sub>0</sub>	Function
L	L	0A to 1B
H	L	0A to 2B
X	H	0A to 1B and 0A to 2B
SEL <sub>1</sub>	TEST <sub>1</sub>	Function
L	L	1A to 1B
H	L	1A to 2B
X	H	1A to 1B and 1A to 2B

3512 tbl 04

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Unit	
$V_{IH}$	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs	2.0	—	—	V	
$V_{IL}$	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs	—	—	0.8	V	
$I_{IH}$	Input HIGH Current	$V_{CC} = \text{Max.}$	$V_I = V_{CC}$	—	—	$\pm 1$	$\mu\text{A}$
$I_{IL}$	Input LOW Current		$V_I = \text{GND}$	—	—	$\pm 1$	
$I_{OZH}$	High Impedance Output Current (3-State Output pins)	$V_{CC} = \text{Max.}$	$V_O = V_{CC}$	—	—	$\pm 1$	$\mu\text{A}$
$I_{OZL}$			$V_O = \text{GND}$	—	—	$\pm 1$	
$I_{OS}$	Short Circuit Current	$V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$	—	300	—	mA	
$V_{IK}$	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$	—	-0.7	-1.2	V	
$R_{ON}$	Switch On Resistance <sup>(4)</sup>	$V_{CC} = \text{Min.}, V_{IN} = 0.0\text{V}$ $I_{ON} = 12\text{mA}$	—	5	7	$\Omega$	
		$V_{CC} = \text{Min.}, V_{IN} = 2.4\text{V}$ $I_{ON} = 8\text{mA}$	—	10	15	$\Omega$	
$I_{OFF}$	Input/Output Power Off Leakage	$V_{CC} = 0\text{V}, V_{IN}$ or $V_O \leq 4.5\text{V}$	—	—	$\pm 1$	$\mu\text{A}$	
$I_{CC}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, V_{IN} = \text{GND}$ or $V_{CC}$	—	0.1	3	$\mu\text{A}$	

**NOTES:**

3512 tbl 05

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- Measured by voltage drop between ports at indicated current through the switch.

## POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$\Delta I_{CC}$	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	1.5	mA
$I_{CCD}$	Dynamic Power Supply Current <sup>(4)</sup>	$V_{CC} = \text{Max.}$ Outputs Open Enable Pin Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	30	40	$\mu A/$ MHz/ Switch
$I_C$	Total Power Supply Current <sup>(6)</sup>	$V_{CC} = \text{Max.}$ Outputs Open 2 Select Pins Toggling (16 Switches Toggling) $f_i = 10\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	4.8	6.4	mA
			$V_{IN} = 3.4$ $V_{IN} = \text{GND}$	—	5.3	7.9	

### NOTES:

3512 tbl 06

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0V$ ,  $+25^\circ C$  ambient.
- Per TTL driven input ( $V_{IN} = 3.4V$ ). All other inputs at  $V_{CC}$  or  $\text{GND}$ .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$   
 $I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_i N)$   
 $I_{CC} = \text{Quiescent Current}$   
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = 3.4V)$   
 $D_H = \text{Duty Cycle for TTL Inputs High}$   
 $N_T = \text{Number of TTL Inputs at } D_H$   
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$   
 $f_i = \text{Input Frequency}$   
 $N = \text{Number of Switches Toggling at } f_i$   
 All currents are in milliamps and all frequencies are in megahertz.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial:  $T_A = -40^\circ C$  to  $+85^\circ C$ ,  $V_{CC} = 5.0V \pm 10\%$

Symbol	Description	Condition <sup>(1)</sup>	Min. <sup>(2)</sup>	Typ.	Max.	Unit
$t_{PLH}$ $t_{PHL}$	Data Propagation Delay A to B, B to A <sup>(3,4)</sup>	$C_L = 50\text{pF}$ $R_L = 500\Omega$	—	—	0.25	ns
$t_{BX}$	Switch Multiplex Delay SEL to A		1.5	—	6.5	ns
$t_{PZH}$ $t_{PZL}$	Switch Turn on Delay SEL, TEST to B		1.5	—	6.5	ns
$t_{PHZ}$ $t_{PLZ}$	Switch Turn off Delay SEL, TEST to B		1.5	—	7	ns
$ Q_{CI} $	Charge Injection, Typical <sup>(5,7)</sup>		—	1.5	—	pC
$ Q_{DCI} $	Charge Injection, Typical <sup>(6,7)</sup>		—	0.5	—	

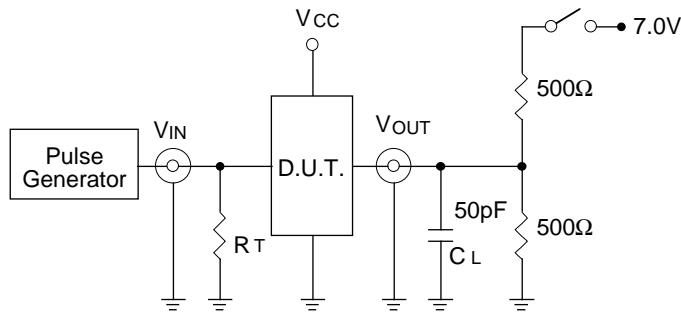
### NOTES:

3512 tbl 07

- See test circuit and waveforms.
- Minimum limits guaranteed but not tested.
- This parameter is guaranteed by design but not tested.
- The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 2.5ns for 50pF load. Since this time is constant and much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay on the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
- Measured at switch turn off, load = 50 pF in parallel with 10 M $\Omega$  scope probe,  $V_{IN} = 0.0$  volts.
- Measured at switch turn off through bus multiplexer, (e.g. - A to 1B => A to 2B), load = 50 pF in parallel with 10 M $\Omega$  scope probe,  $V_{IN}$  at A = 0.0 volts. Charge injection is reduced because the injection from the turn off of the A to 1B switch is compensated by the turn on of the A to 2B switch.
- Characterized parameter. Not 100% tested.

## TEST CIRCUITS AND WAVEFORMS

### TEST CIRCUITS FOR ALL OUTPUTS



3512 Ink 03

### SWITCH POSITION

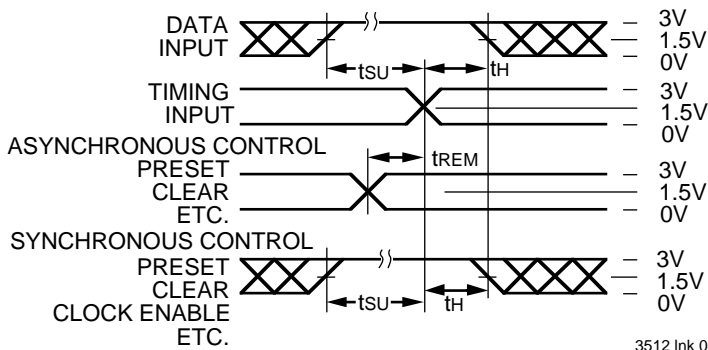
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

3512 Ink 08

#### DEFINITIONS:

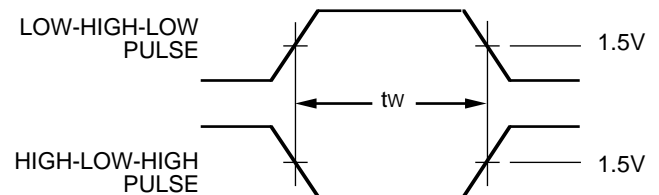
$C_L$  = Load capacitance: includes jig and probe capacitance.  
 $R_T$  = Termination resistance: should be equal to  $Z_{OUT}$  of the Pulse Generator.

### SET-UP, HOLD AND RELEASE TIMES



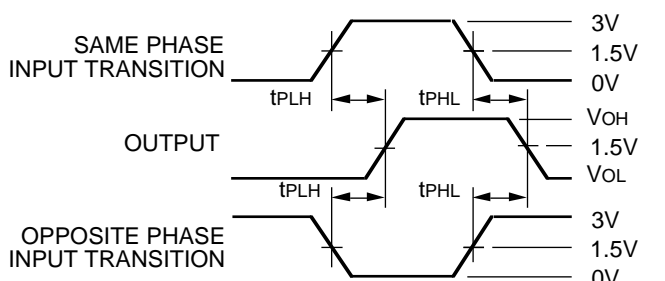
3512 Ink 04

### PULSE WIDTH



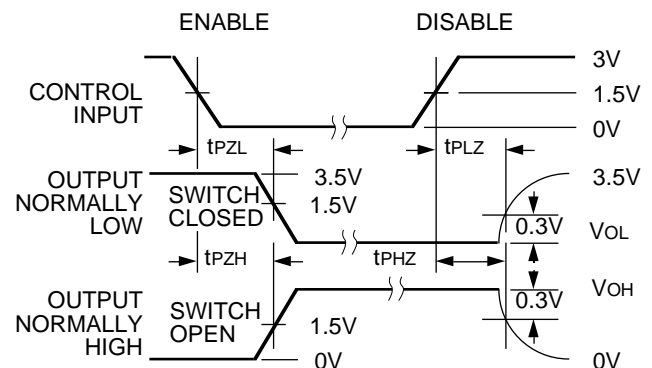
3512 Ink 05

### PROPAGATION DELAY



3512 Ink 06

### ENABLE AND DISABLE TIMES

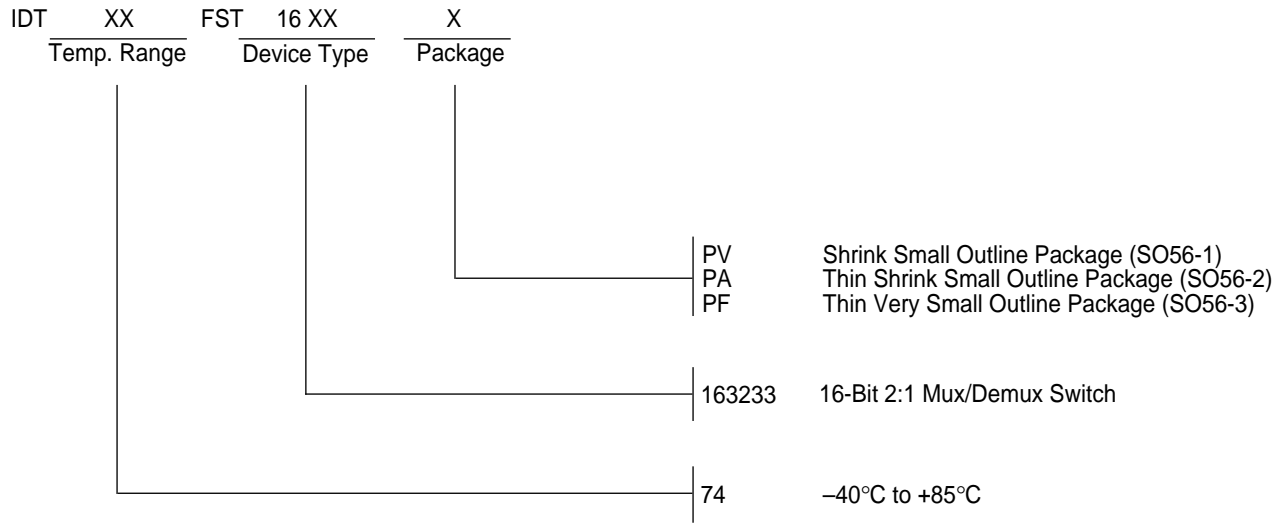


3512 Ink 07

#### NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
- Pulse Generator for All Pulses: Rate  $\leq$  1.0MHz;  $t_f \leq$  2.5ns;  $t_r \leq$  2.5ns

**ORDERING INFORMATION**



3512 drw 08

Integrated Device Technology, Inc. reserves the right to make changes to the specifications in this data sheet in order to improve design or performance and to supply the best possible product.

**Integrated Device Technology, Inc.**

2975 Stender Way, Santa Clara, CA 95054-3090

Telephone: (408) 727-6116

FAX 408-492-8674