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Designer's™ Data Sheet

SCANSWITCH™

NPN Bipolar Power Deflection Transistor For High and Very High Resolution Monitors

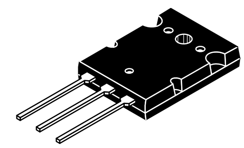
The MJL16218 is a state–of–the–art SWITCHMODE™ bipolar power transistor. It is specifically designed for use in horizontal deflection circuits for 20 mm diameter neck, high and very high resolution, full page, monochrome monitors.

- 1500 Volt Collector–Emitter Breakdown Capability
- Typical Dynamic Desaturation Specified (New Turn–Off Characteristic)
- Application Specific State–of–the–Art Die Design
- Fast Switching:
  175 ns Inductive Fall Time (Typ)
  2000 ns Inductive Storage Time (Typ)
- Low Saturation Voltage:
  0.2 Volts at 5.0 Amps Collector Current and 2.0 A Base Drive
- Low Collector–Emitter Leakage Current — 250 µA Max at 1500 Volts — V_{CES}
- High Emitter–Base Breakdown Capability For High Voltage Off Drive Circuits — 8.0 Volts (Min)

MJL16218*

*Motorola Preferred Device

**POWER TRANSISTOR
15 AMPERES
1500 VOLTS — V_{CES}
170 WATTS**



**CASE 340G–02, STYLE 2
TO–3PBL**

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Breakdown Voltage	V_{CES}	1500	Vdc
Collector–Emitter Sustaining Voltage	$V_{CEO(sus)}$	650	Vdc
Emitter–Base Voltage	V_{EBO}	8.0	Vdc
Collector Current — Continuous — Pulsed (1)	I_C I_{CM}	15 20	Adc
Base Current — Continuous — Pulsed (1)	I_B I_{BM}	7.0 14	Adc
Maximum Repetitive Emitter–Base Avalanche Energy	W (BER)	0.2	mJ
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derated above T_C = 25°C	P_D	170 39 1.49	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 125	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance — Junction to Case	$R_{\theta JC}$	0.67	°C/W
Lead Temperature for Soldering Purposes 1/8″ from the case for 5 seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.
(2) Proper strike and creepage distance must be provided.

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Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (2)					
Collector Cutoff Current (V_{CE} = 1500 V, V_{BE} = 0 V) (V_{CE} = 1200 V, V_{BE} = 0 V)	I_{CES}	— —	— —	250 25	μAdc
Emitter–Base Leakage (V_{EB} = 8.0 Vdc, I_C = 0)	I_{EBO}	—	—	25	μAdc
Emitter–Base Breakdown Voltage (I_E = 1.0 mA, I_C = 0)	$V_{(BR)EBO}$	8.0	11	—	Vdc
Collector–Emitter Sustaining Voltage (Table 1) (I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	650	—	—	Vdc
ON CHARACTERISTICS (2)					
Collector–Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 2.0 Adc) (I_C = 3.0 Adc, I_B = 0.6 Adc)	$V_{CE(sat)}$	— —	0.17 0.14	1.0 0.5	Vdc
Base–Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 1.0 Adc)	$V_{BE(sat)}$	—	0.9	1.5	Vdc
DC Current Gain (I_C = 1.0 A, V_{CE} = 5.0 Vdc) (I_C = 12 A, V_{CE} = 5.0 Vdc)	h_{FE}	— 4.0	24 6.0	— —	—
DYNAMIC CHARACTERISTICS					
Dynamic Desaturation Interval (I_C = 5.5 A, I_{B1} = 2.2 A, LB = 1.5 μH)	t_{ds}	—	350	—	ns
Output Capacitance (V_{CE} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)	C_{ob}	—	300	500	pF
Gain Bandwidth Product (V_{CE} = 10 Vdc, I_C = 0.5 A, f_{test} = 1.0 MHz)	f_T	—	0.8	—	MHz
SWITCHING CHARACTERISTICS					
Inductive Load (I_C = 6.0 A, I_B = 2.0 A), High Resolution Deflection Simulator Circuit Table 2					ns
Storage	t_{sv}	—	2000	3000	
Fall Time	t_{fi}	—	175	250	

(2) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

SAFE OPERATING AREA

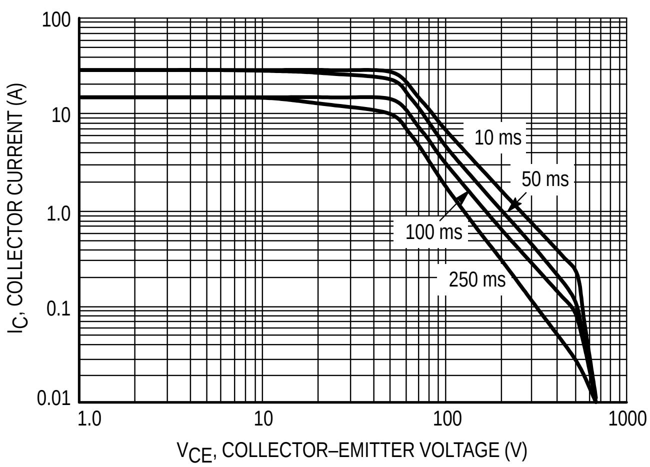


Figure 1. Maximum Forward Bias Safe Operating Area

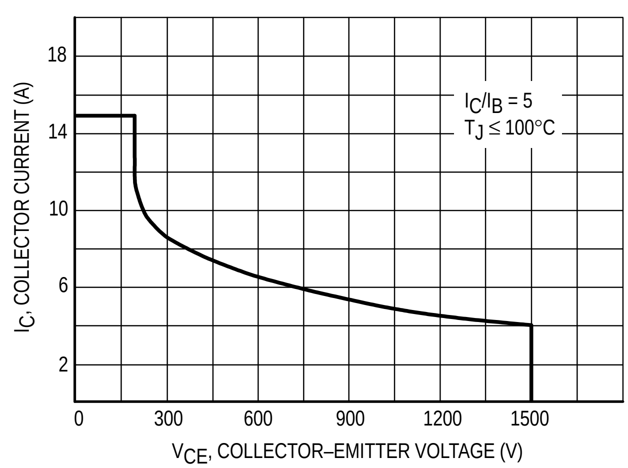


Figure 2. Maximum Reverse Bias Safe Operating Area

SAFE OPERATING AREA (continued)

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C – V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 1 may be found at any case temperature by using the appropriate curve on Figure 3.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

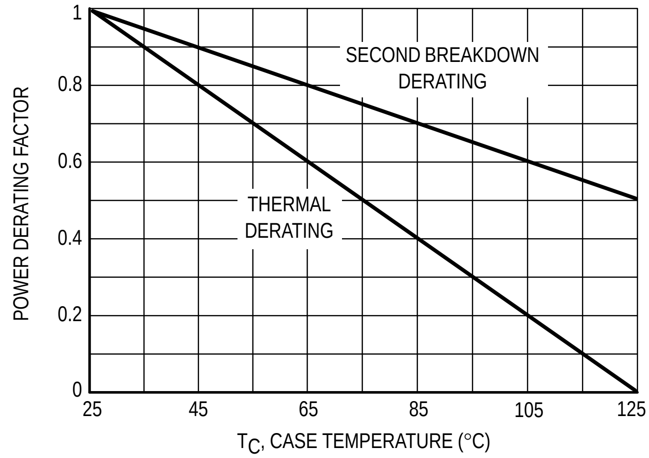


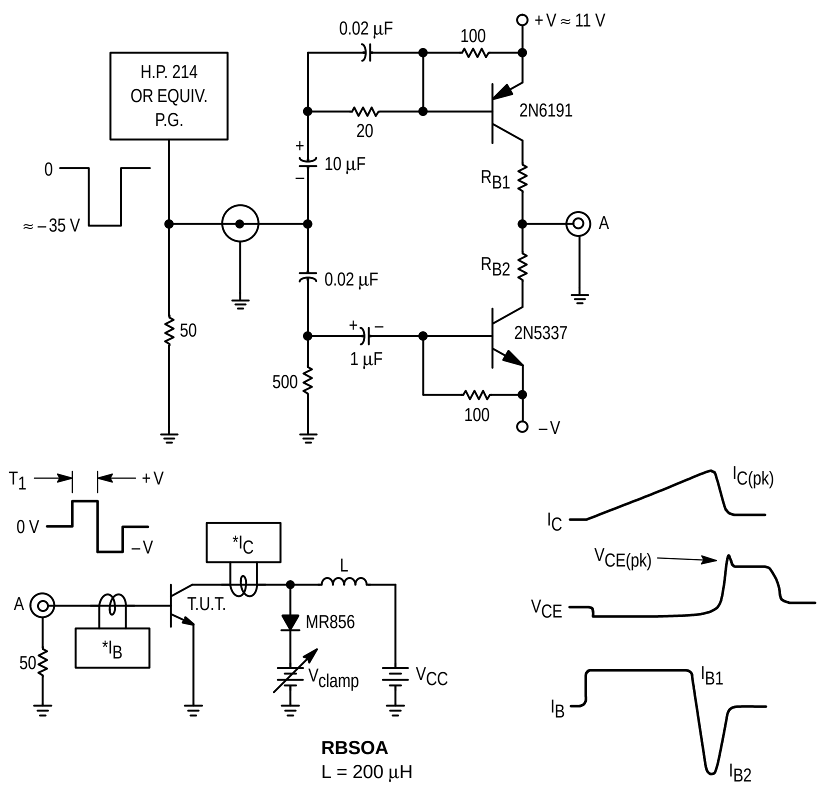
Figure 3. Power Derating

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base–to–emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc.

The safe level for these devices is specified as Reverse Biased Safe Operating Area and represents the voltage–current condition allowable during reverse biased turnoff. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 2 gives the RBSOA characteristics.

Table 1. RBSOA/$V_{(BR)CEO(SUS)}$ Test Circuit



$$T_1 \approx \frac{L_{coil}\ (I_{Cpk})}{V_{CC}}$$

T_1 adjusted to obtain $I_{C(pk)}$

$V_{(BR)CEO}$
L = 10 mH
$R_{B2} = \infty$
V_{CC} = 20 Volts

*Tektronix
P–6042 or
Equivalent

RBSOA
L = 200 µH
R_{B2} = 0
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}

Note: Adjust –V to obtain desired $V_{BE(off)}$ at Point A.

TYPICAL ELECTRICAL CHARACTERISTICS

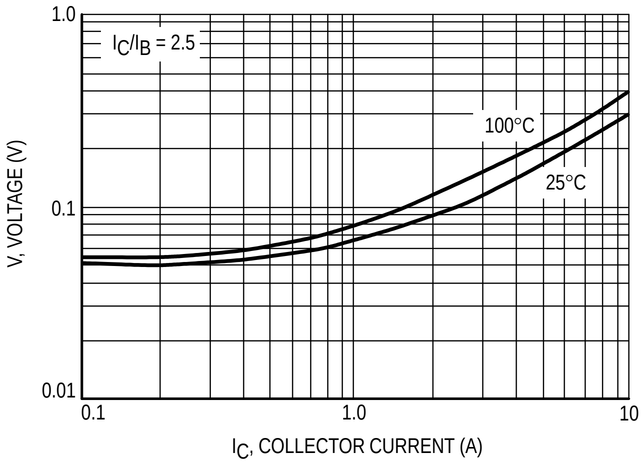


Figure 4. Typical Collector–Emitter Saturation Voltage

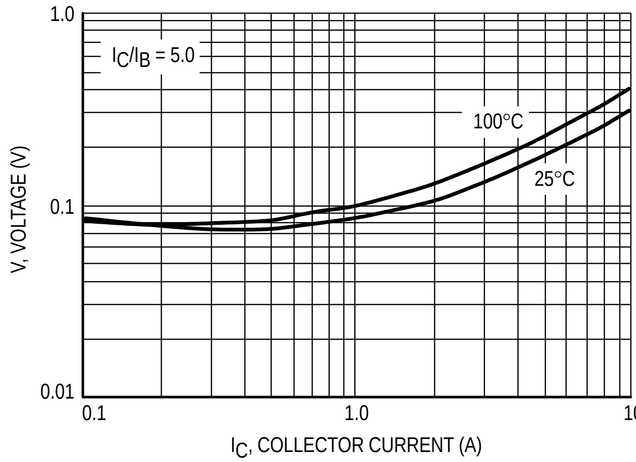


Figure 5. Typical Collector–Emitter Saturation Voltage

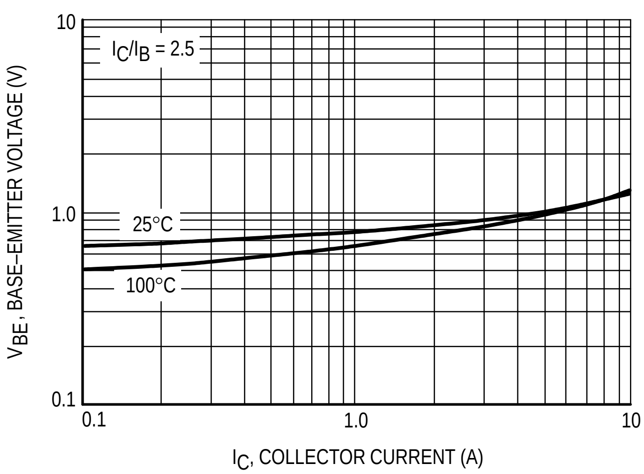


Figure 6. Typical Emitter–Base Saturation Voltage

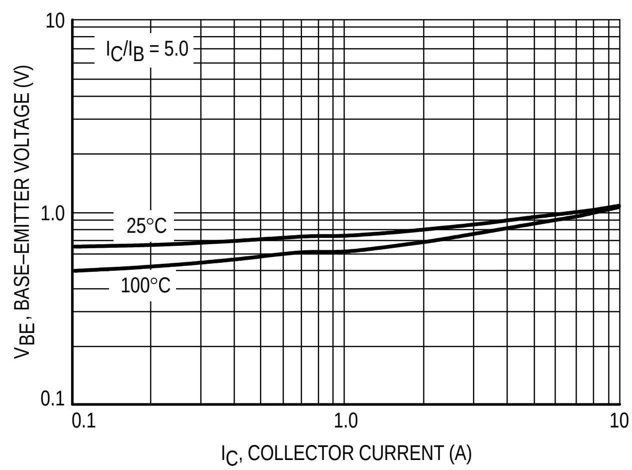


Figure 7. Typical Emitter–Base Saturation Voltage

TYPICAL ELECTRICAL CHARACTERISTICS (continued)

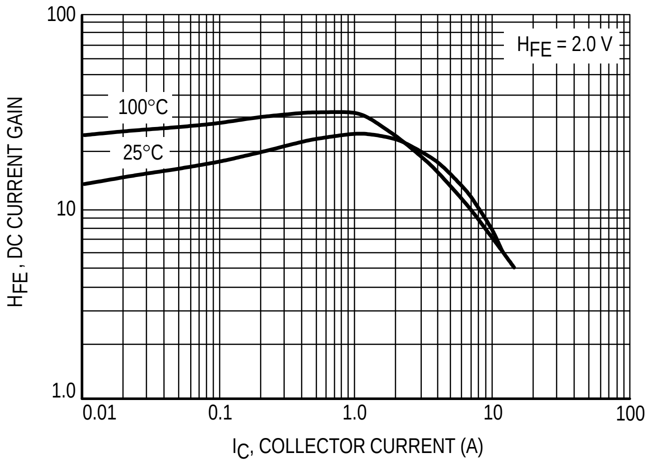


Figure 8. DC Current Gain

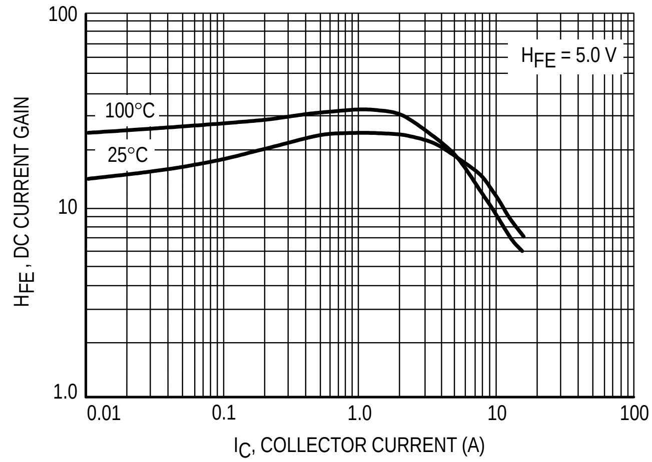


Figure 9. DC Current Gain

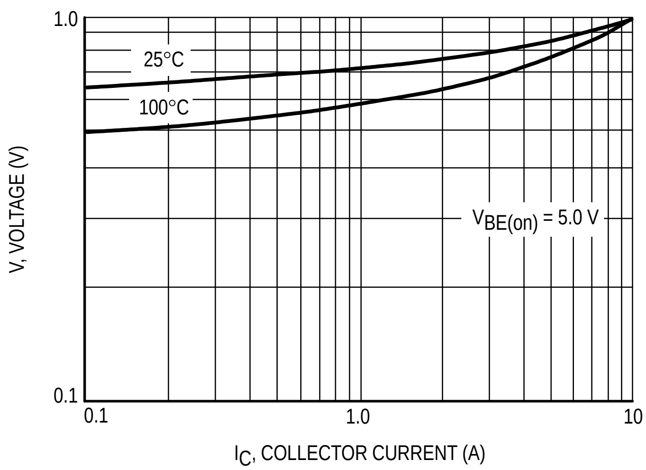
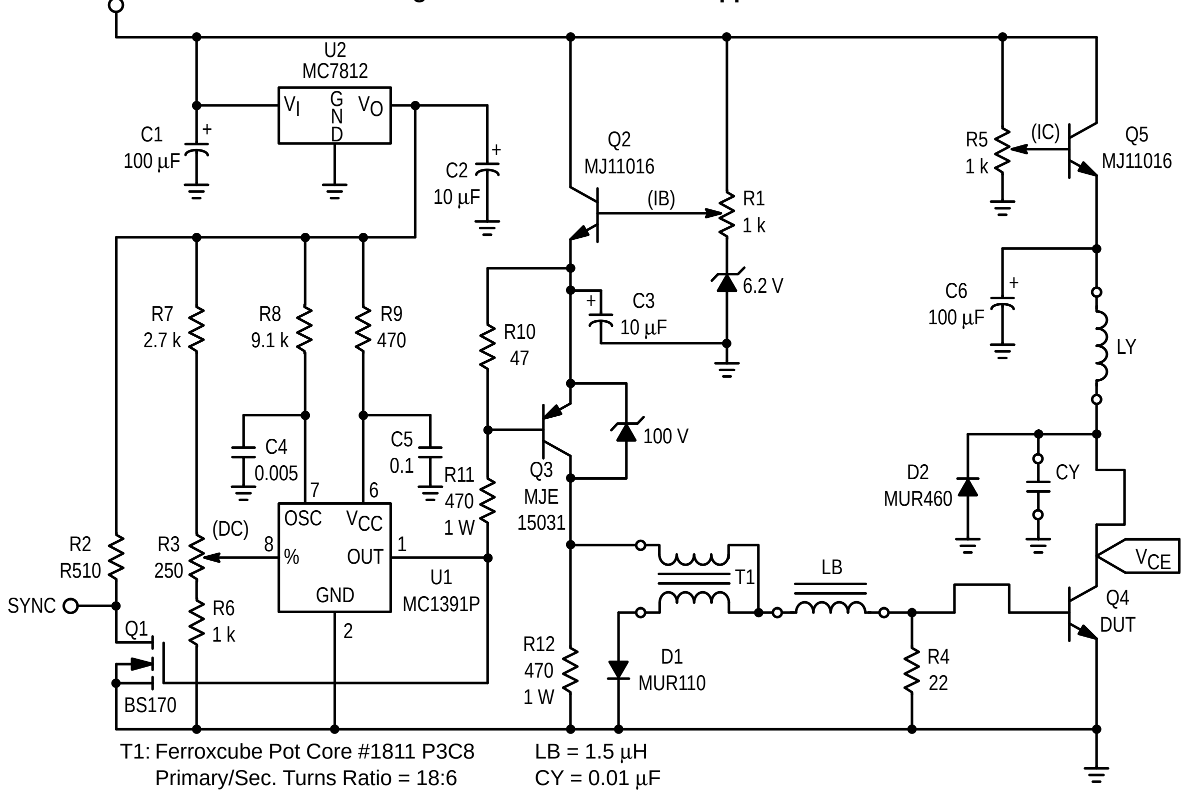


Figure 10. “On” Voltages

DYNAMIC DESATURATION

The SCANSWITCH series of bipolar power transistors are specifically designed to meet the unique requirements of horizontal deflection circuits in computer monitor applications. Historically, deflection transistor design was focused on minimizing collector current fall time. While fall time is a valid figure of merit, a more important indicator of circuit performance as scan rates are increased is a new characteristic, "dynamic desaturation." In order to assure a linear collector current ramp, the output transistor must remain in hard saturation during storage time and exhibit a rapid turn–off transition. A sluggish transition results in serious consequences. As the saturation voltage of the output transistor increases, the voltage across the yoke drops. Roll off in the collector current ramp results in improper beam deflection and distortion of the image at the right edge of the screen. Design changes have been made in the structure of the SCANSWITCH series of devices which minimize the dynamic desaturation interval. Dynamic desaturation has been defined in terms of the time required for the V_{CE} to rise from 1.0 to 5.0 volts (Figures 9 and 10) and typical performance at optimized drive conditions has been specified. Optimization of device structure results in a linear collector current ramp, excellent turn–off switching performance, and significantly lower overall power dissipation.

Table 2. High Resolution Deflection Application Simulator



T1: Ferroxcube Pot Core #1811 P3C8
Primary/Sec. Turns Ratio = 18:6
Gapped for L_P = 30 µH

LB = 1.5 µH
CY = 0.01 µF
LY = 13 µH

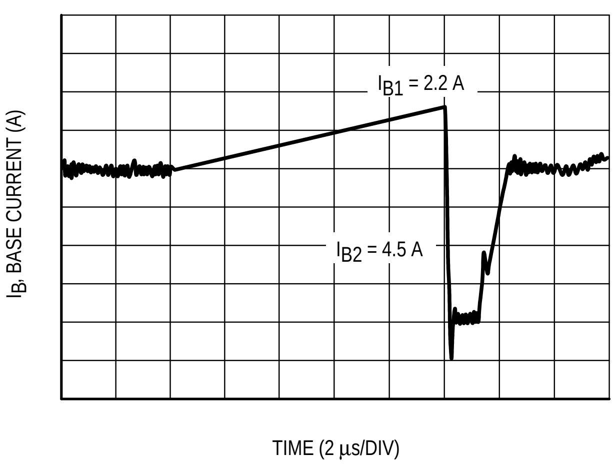


Figure 11. Deflection Simulator Circuit Base Drive Waveform

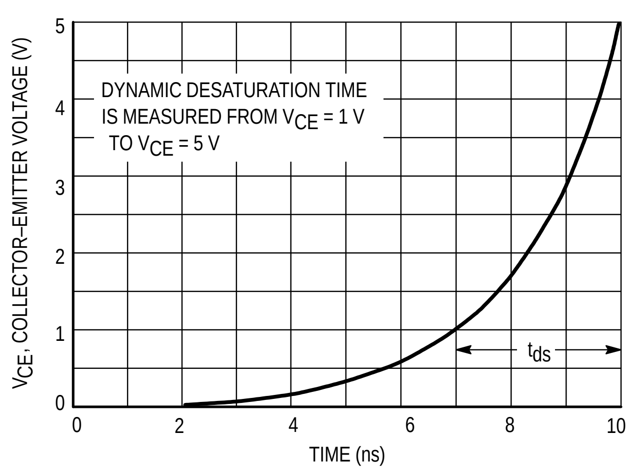
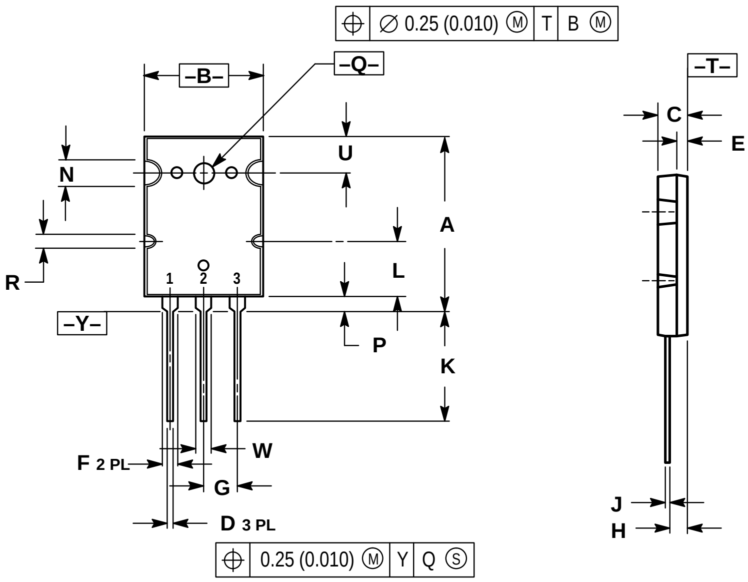


Figure 12. Definition of Dynamic Desaturation Measurement

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.8	2.9	1.102	1.142
B	19.3	20.3	0.760	0.800
C	4.7	5.3	0.185	0.209
D	0.93	1.48	0.037	0.058
E	1.9	2.1	0.075	0.083
F	2.2	2.4	0.087	0.102
G	5.45 BSC		0.215 BSC	
H	2.6	3.0	0.102	0.118
J	0.43	0.78	0.017	0.031
K	17.6	18.8	0.693	0.740
L	11.0	11.4	0.433	0.449
N	3.95	4.75	0.156	0.187
P	2.2	2.6	0.087	0.102
Q	3.1	3.5	0.122	0.137
R	2.15	2.35	0.085	0.093
U	6.1	6.5	0.240	0.256
W	2.8	3.2	0.110	0.125

STYLE 2:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

CASE 340G–02
TO–3PBL
ISSUE F

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