# MLX90121

## *13.56MHz RFID Transceiver*

## *Features and Benefits*

- ❑ Conforms with ISO14443B[1]
- ❑ Conforms with ISO15693
- ❑ Programmable encoder and decoder
- ❑ Low external component count

(1) RATP / Innovatron Technology

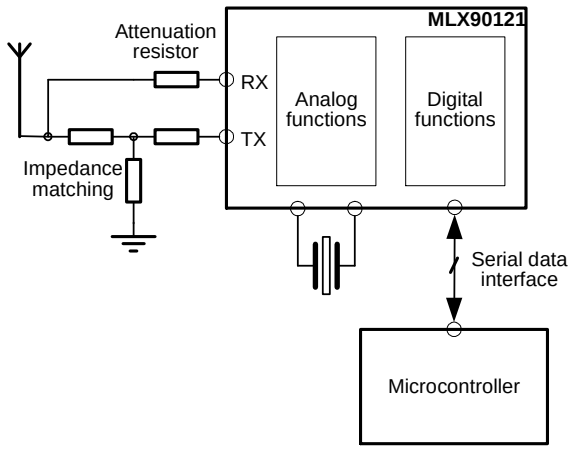
## *Applications*

- ❑ Portable data terminals
- ❑ Access control readers
- ❑ Contact-less payment terminals
- ❑ Smart label printer

## *Ordering Information*

| Part No. | Temperature Suffix | Package Code | Option code |
|---|---|---|---|
| MLX90121 | E (-40°C to 85°C) | FR (SSOP20, 209 mils) | FSK |

## *1. Functional Diagram*




## *2. Description*

The MLX90121 is an ISO compliant 13.56MHz RFID transceiver integrated circuit.

The main features include user selectable modulation depth in write mode, whereas single sub-carrier, FSK and PSK modulations are recognized in the read mode.

The receiver is based on a diode envelope detector, followed by an IF filter and amplifier. A logarithmic amplifier is used for single sub-carrier detection, ensuring fast and clean data recovery. The limiting output of the log amp is used for FSK and PSK recovery.

The transmitter uses a built in open drain output transistor, which can provide up to 250 miliwatts of RF power to a 50 ohms load with a 5 volts power supply using the recommended matching network. This is suitable for most short to mid range applications. A simplified antenna and matching network can be used, at the expense of a reduced reading range, for example in hand-held reader applications.

The chip is configured with a serial interface. A synchronization signal is available when the majority voting is used.

Digital part contains FSK (423 / 484kHz) and PSK (847kHz) decoders and a programmable encoder to facilitate data handling with a low cost microcontroller. The encoder can be programmed with 6 different patterns.

The chip can also be used as an analog front-end, in direct mode.

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## 3. Glossary of Terms

| | |
|---|---|
| RFID | Radio Frequency IDentification |
| ISO | International Organization for Standardization / International Electro-technical Commission. |
| ASK | Amplitude Shift Keying |
| FSK | Frequency Shift Keying |
| PSK | Phase Shift Keying |

## 4. Absolute Maximum Ratings

| Parameter | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage ($V_{DD}$ with respect to $V_{SS}$) | $V_{DD}$ | DC | -0.3 | 6 | V |
| Input voltage on any pin (except TX) | $V_{in}$ | | -0.3 | $V_{DD}$+0.3 | V |
| Maximum power dissipation (without heat sink) | $P_{max}$ | | | 500 | mW |
| Maximum junction temperature | $T_j$ | | | +150 | ºC |
| Storage temperature | $T_{stor}$ | | -55 | +150 | ºC |

Exceeding the absolute maximum ratings may cause permanent damage. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 5. MLX90121 Electrical Specifications

$T_A$ = -40 ºC to +85 ºC, or 0ºC to +70 ºC according to the version, $V_{DD}$ = 5Volts, unless otherwise noted.
On board resonator is used.

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **General DC Parameters** | | | | | | |
| Operating supply voltage range | $V_{DD}$ | $V_{DD}$ with respect to $V_{SS}$ | 2.7 | 5 | 5.5 | V |
| Standby current consumption | $I_{stb}$ | $V_{DD}$ = 5.5 V - $T_A$ = +85 ºC<br>*$T_A$ = +25 ºC* | | 3<br>*0.1* | 30<br>*10* | µA<br>*µA* |
| Idle mode current consumption | $I_{idle}$ | $V_{DD}$ = 5.5V - Analog section off<br>*$V_{DD}$ = 3V, XBUF output disabled* | | 3<br>*1* | 5<br>*3* | mA<br>*mA* |
| Transmit current | $I_{tr}$ | 50 Ohms load<br>*$V_{DD}$ = 3V* | | 80<br>*45* | 120<br>*70* | mA<br>*mA* |

## 6. MLX90121 Specific Specifications

DC Operating Parameters $T_A$ = -40°C to 85°C, or 0°C to +70°C according to the version, $V_{DD}$ = 5V (unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Transmitter specifications** | | | | | | |
| Peak voltage applied on drain of output transistor | | | | | 32 | V |
| Output transistor power dissipation | | With heat sink | | | 600 | mW |
| Output transistor ON resistance | | $I_d$ = 50 mA | | 2 | 5 | Ω |
| Output power for five volts operation | | See note 1 | | 250 | | mW |
| Amplitude modulation depth adjustment range, in 10% mode, with external resistor connected between RMOD pin and ground. | | See note 1 | 0 | | 90 | % |
| Amplitude modulation depth in 10% mode with nominal external resistor (10Ω) | | See note 1 | 8 | 10 | 14 | % |
| Minimum depth for 100% ASK | | See note 1 | 40 | | | dB |
| Rise time for 100% ASK | | 50 Ohms load - 5% to 60%<br>50 Ohms load - 5% to 90% | | 0.2<br>0.3 | 0.4<br>1.5 | µs<br>µs |
| Fall time for 100% ASK | | 50 Ohms load - 100% to 5% | | 0.6 | | µs |
| Rise and fall time for 10% modulation depth ( nominal external resistor used) | | 50 Ohms load | | 0.2 | | µs |
| | | | | | | |
| **Receiver specifications** | | | | | | |
| Small signal input impedance (RX) | | | | 100 | | kΩ |
| Input RF voltage range (RX – $V_{SS}$) | | With 4.7kΩ series external resistor | | 2 | 3 | $V_{pp}$ |
| Receiver sensitivity | | See note 2 | -35 | -45 | | dBm |
| FSK IF filter cut off points | | | | 200-1400 | | kHz |
| Gain, in FSK mode (FM output) | | | | 120 | | dB |

| | | | | | | |
|---|---|---|---|---|---|---|
| **Serial link and digital I/O** | | | | | | |
| Output current drive | $I_{ol}$ | $V_{ol} \leq 0.4$ Volt | 4 | | | mA |
| Output voltage low | $V_{ol}$ | $I_{ol\ max}$=4mA | 0 | 0.2 | 0.4 | V |
| Output voltage high | $V_{oh}$ | $I_{oh\ max}$=4mA | 4.6 | 4.8 | 5 | V |
| Input voltage high | $V_{ih}$ | | 0.7 * $V_{DD}$ | | $V_{DD}$ + 0.3 | V |
| Input voltage low | $V_{il}$ | | -0.3 | | 0.3 * $V_{DD}$ | V |
| CK pulse | $T_{CK}$ | "0" level pulse or "1" level pulse | 500 | | | ns |
| General setup time | $T_s$ | | 60 | | | ns |
| General hold time | $T_h$ | | 60 | | | ns |
| Pulse time between successive registers writing | $T_{mw}$ | | 5 | | | µs |
| **Crystal Oscillator** | | | | | | |
| Frequency range | $F_{xtal}$ | ISO compliant applications | | 13.56 | | MHz |
| Start-up time | $T_{start}$ | | | 2 | 5 | ms |
| Xtal series resistance | | | | 50 | 100 | Ω |
| | | | | | | |
| **External clock signal specifications** | | see note 3 | | | | |
| Min sine wave amplitude, AC coupled<br>Input on pin XTAL2 | | | 1 | | $V_{DD}$ | $V_{PP}$ |
| Min sine wave amplitude, DC coupled<br>Input on pin XTAL2 | | Input has to be centered around Vdd/2 | 1 | | $V_{DD}$ | $V_{PP}$ |
| | | | | | | |
| **XBUF output specifications** | | | | | | |
| XBUF Low Level (Col) | | 1K load resistor | | 0.1 | | V |
| XBUF High Level (Coh) | | 1K load resistor | | 4.8 | | V |
| Rise and fall times (10%-90%) | | 1K load resistor//12pF | | 3 | | ns |

***Notes***

1. Parameter measured using recommended output matching network.

2. This parameter is measured using a base band signal for all specified modulation modes. The measurement is made at the DOUT output with the input diode detector bypassed.

3. The external clock symmetry is of paramount importance. It has a direct influence on the transmitter output power. When using a sine wave as external clock input, it must not show visible distortion. In case a square wave is used, its duty cycle has to be equal to 50%.

# 7. General Description

***Power supply***

The 90121 requires a nominal 3 or 5 volts external power supply. Operation is guaranteed between 2.7 and 5.5 Volts. The current drain depends on the antenna impedance and the output matching network configuration. Care must be taken about the power supply: power supply ripple and noise will severely degrade the overall system performance.

***Transmitter***

The output transistor is a low Ron MOSFET. The drain is directly accessible on the TX pin. A recommended application schematic optimized to drive a resistive fifty ohms antenna with a five volts power supply is provided as a part of this specification. A simple resonant circuit or/and a simpler matching network can be connected to the output. In that case, the general performance and harmonic suppression will be reduced. 100 % modulation is achieved by means of gating the square wave drive of the output transistor. A variable modulation depth is obtained by means of switching a resistor in series with the output transistors' source connection. An external resistor provides the default modulation depth setting. Increasing this external resistor will increase the modulation depth.

***Receiver***

The receiver input is typically connected to the antenna through an external resistor. The modulation from the tag is then recovered by means of a diode envelope detector.

***FSK and PSK recovery***

The demodulated input signal is amplified and band pass filtered. The signal is then hard limited by a logarithmic amplifier, and fed to the digital section. PSK decoded, FSK decoded or a direct FSK signal can be used for further decoding.

***Majority Voting***

Both FSK/PSK or ASK can use the Majority Voting function that will filter for noise and jitter, that will correct distorted signals and will hence improve performance.

***Reference clock and internal oscillator***

The reference clock may be obtained externally by applying a suitable clock signal to the XTAL1 pin. A sine wave centered at VCC/2 or a CMOS logic compatible signal is an acceptable external system clock. The built-in reference oscillator will work either with a quartz crystal or a ceramic resonator. The nominal system clock frequency is 13.56 MHz.

***Reset defaults and power management***

After a power on reset has been performed, the device is put in its default configuration. There are three power modes available. In the transmission mode, the device is fully powered. In the idle mode, only the reference oscillator is running. This allows for a fast start up. In the power down mode, the device internal bias system is completely switched off, offering essentially a zero state.

***Serial communication interface***

The communication interface normally uses 6 wires:

- CK: serial clock input
- DIN: data input
- DOUT: data output
- DSYNC: synchronization output for DOUT
- MODE: configuration or communication selection input
- RTB: reception or transmission selection input.

## 8. Applications Information

This schematic has been optimized to drive a fifty ohms resistive antenna, using a five volts power supply.

***Functional description***

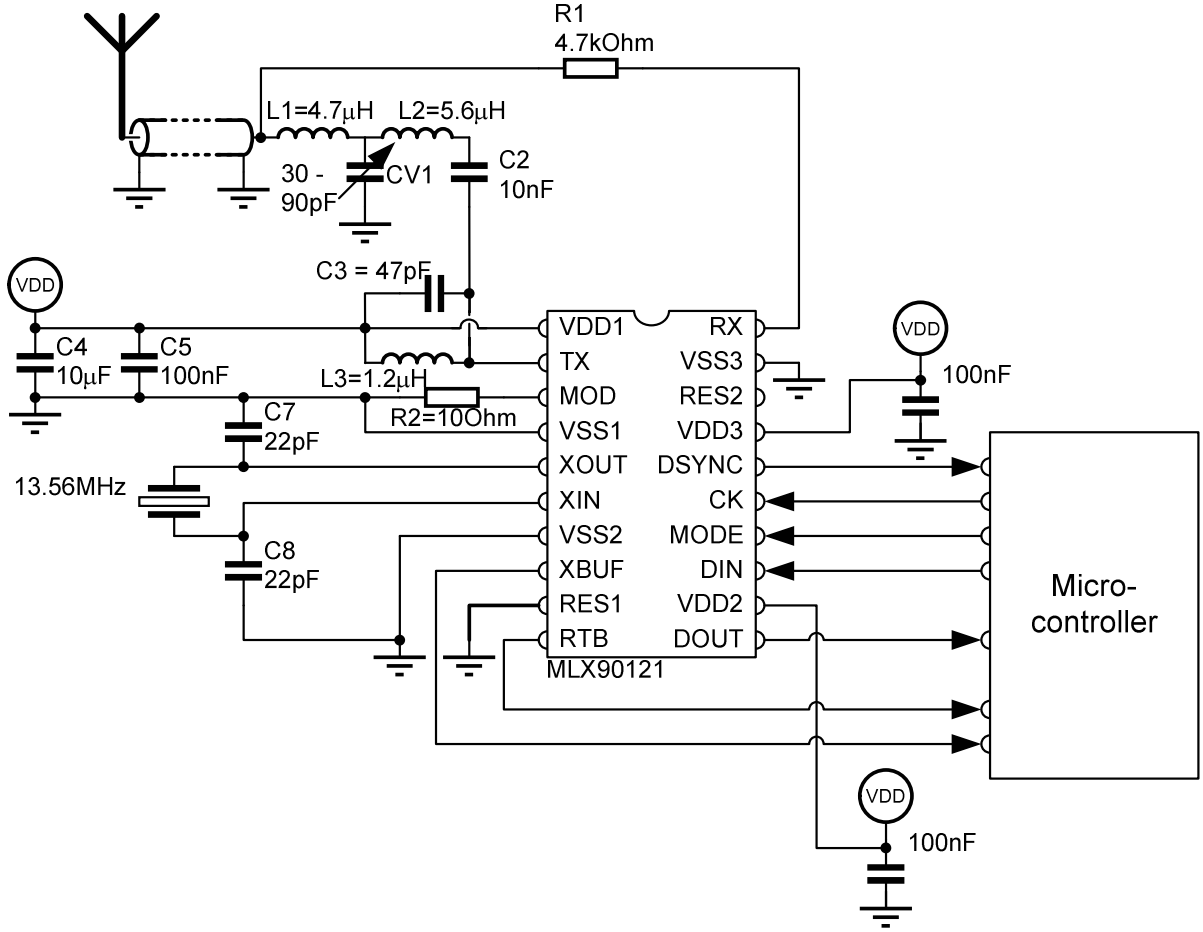
The transmitter output TX is connected to the supply by means of a choke L3. C3 is added to avoid a high dV/dt at the TX output in case of a sudden interruption of the current in the choke. C3 is chosen high enough to protect the chip, but low enough to keep the resonance of L3-C3 well above 13.56 MHz.

The transmitter signal is coupled with DC blocking capacitor C2 to the antenna matching network, which is a T network made up by L2, CV1 and L1. CV1 allows a proper matching between the 50Ohm antenna and the output impedance of the transmitter stage.

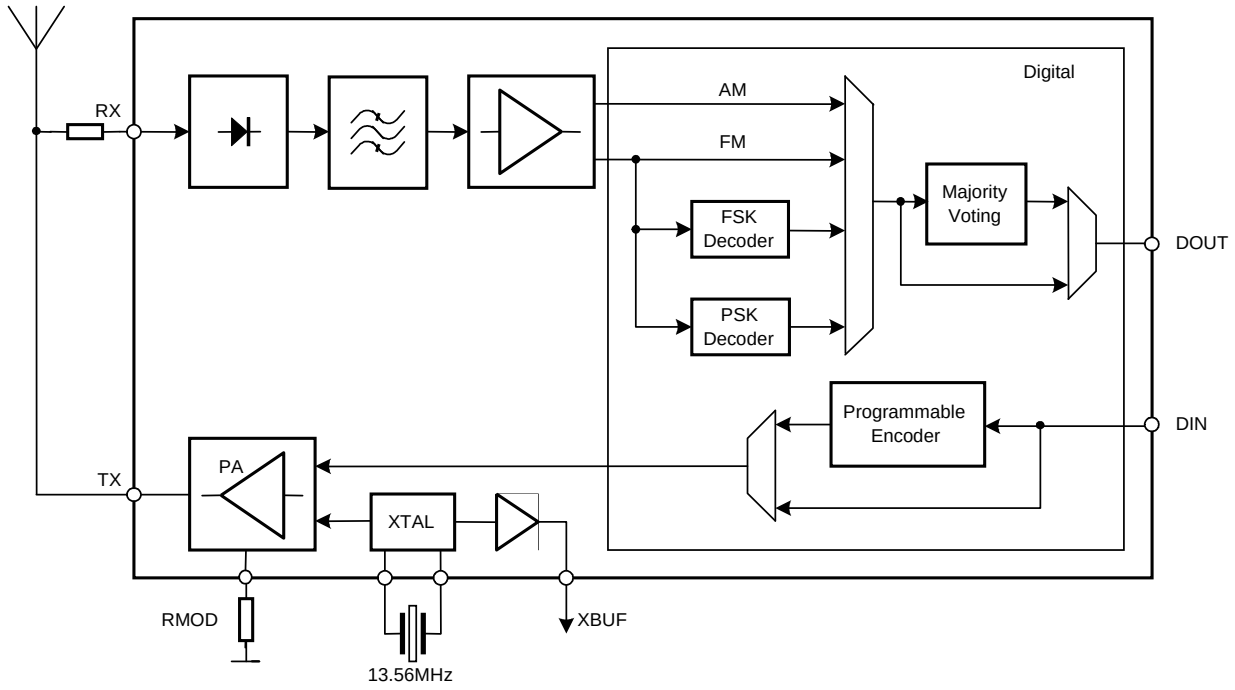
The receiver part of the chip gets its signal directly from the antenna by means of R1. It limits the voltage swing at the RX pin to a level in between the supplies.

One should take care to properly decouple the power supplies of the chip. Especially the Vdd1 supply which is used for the transmitter output. Any amplitude noise on that supply is AM modulated on the carrier and will hence be perceived as noise by the receiver part. The same holds for any phase noise that gets introduced into the quartz oscillator.

For the signal that goes to- and from the microcontroller: one should take care to keep them as far as possible from the analog parts and the quartz oscillator. To do a first evaluation, it is highly recommended to use the MLX90121 evaluation board that can be ordered from Melexis. The clock for the microcontroller can also be derived from the XBUF pin. This pin provides a 13.56MHz buffered clock or 13.56MHz divided by 2.



## 9. Block Diagram




## 10. Digital Interface

The MLX90121 is driven by four signals: MODE and RTB pins are used to select the operating mode and DIN and CK pins are used to configure the chip and to transmit data.

The MLX90121 has two signal outputs. DOUT contains the decoded response of the transponder and DSYNC is used as a synchronization output by the microcontroller.

| Pin Name | I/O | Function |
|---|---|---|
| MODE | I | 0 = Configuration Mode, 1 = Communication Mode |
| RTB | I | 0 = Transmission Mode, 1 = Reception Mode |
| DIN | I | Data Input for Transmission or Configuration |
| CK | I | Clock and Trigger |
| DOUT | O | Data Output from Reception or Configuration |
| DSYNC | O | Data Synchronization Clock for Transmission or Reception |

***Function Summary***

| MODE | RTB | Function |
|---|---|---|
| 0 | 0 | Configuration |
| 1 | 0 | Transmission |
| 0 | 1 | Reserved (*) |
| 1 | 1 | Reception |

(*) the reserved mode is for manufacturing purpose only and should not be applied by the user.

# 11. Operating Modes

## 11.1. Definitions

There are two main operating modes:

- MODE = 0 : Configuration Mode
- MODE = 1 : Communication Mode

The configuration mode allows writing in the configuration registers. It will configure all parameters in the transceiver.

The communication mode allows communicating with a transponder. Different options are available:

- Direct transmission: The transmission protocol is handled by an external microcontroller.
- Hardware transmission: The low level protocol is handled by an internal programmable encoder. It allows using a low cost microcontroller.
- Direct reception: The reception protocol is handled by an external microcontroller.
- Hardware reception: FSK/PSK decoders and Majority Voting can be enabled to allow using a low cost microcontroller.

## 11.2. Configuration Mode

### *Registers Addresses*

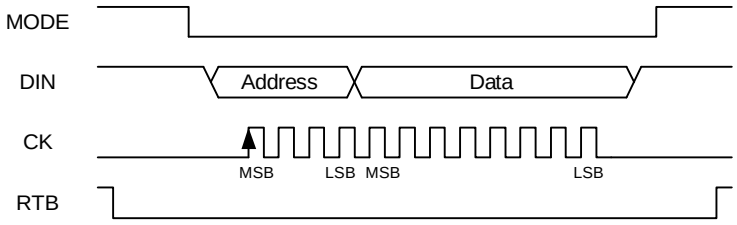
For configuration purposes, users have access to 13 eight bit registers, which can be addressed using a 4 bit address.

| Address | Register name |
|---|---|
| 0 | AnalogConfig |
| 1 | PowerState |
| 2 | Reserved (*) |
| 3 | DigitalConfig |
| 4 | EncoderSym0 |
| 5 | EncoderSym1 |
| 6 | EncoderSym2 |
| 7 | EncoderSym3 |
| 8 | EncoderSym4 |
| 9 | EncoderSym5 |
| 10 | EncoderTimeRef |
| 11 | DecoderTimeRef |
| 12 | LTC |

(*) the reserved register is for manufacturing purpose only and should not be used.

### *Write Configuration Registers*

First the MODE line is asserted low to enable the configuration mode. Then data is fed serially into the chip with the CK and DIN lines. Data on the DIN line is read on the rising edge of CK. The first four bits on DIN are the register address and the eight following bits are the data. Address and data fields are written MSB (Most Significant Bit) first.

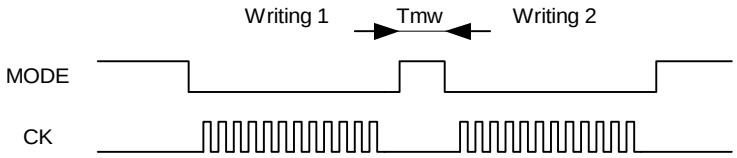



After sending address and data, the MODE line is asserted high and the chip is ready to receive the next register configuration.

| Signal | Assign |
|---|---|
| MODE | 0 |
| RTB | 0 |
| DIN | 4-bit Address + 8-bit Data |
| CK | 12 clock pulses |
| DOUT | x |
| DSYNC | x |

***Notes***

1. If a register does not contain eight bits, write '0' in the unused bit.
2. When MODE is asserted high, the chip is in communication mode. If the encoder is disabled (by default), DIN has to be kept at '1' to avoid any modulation on the antenna.
3. In case of successive registers writings, it is mandatory to have MODE asserted high for at least $T_{mw}$ = 5µs in between each access, as shown in the following diagram.




## *11.3. Communication Modes*

### *11.3.1. Transmission*

#### *11.3.1.a. Analog Setup*

For the transmission, the modulation depth has to be chosen. This is done by the TModIndex bit of the AnalogConfig register, which selects the modulation index: 10% or 100%.

The modulation index can be further tuned by means of the external RMOD resistor.

### *11.3.1.b. Direct Transmission*

Before analog processing, data transmission can be either direct or pre-processed by means of hardware accelerators. Direct transmission can be performed with the following setup:

| Signal | Assign |
|---|---|
| MODE | 1 |
| RTB | 0 |
| DIN | Data to transmit |
| CK | 0 |
| OUT | x |
| DSYNC | x |

Data has to be transmitted in real time by the microcontroller on DIN input. The modulation is done when DIN is asserted low, so by default DIN has to be asserted high. If a configuration register has to be written, keep DIN high when MODE is asserted low. In configuration mode, the field is held without modulation independently of DIN.

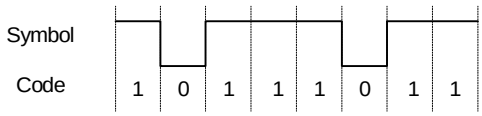
### *11.3.1.c. Hardware Encoding Transmission*

This programmable encoder allows predefining six different patterns of 8 bits. The encoder is selected by setting the bit EncoderEn in the DigitalConfig register.

#### *Symbol Setup*

The six symbols are called EncoderSym0 to EncoderSym5. There is a seventh symbol which is hard-coded to 0xFF (11111111).

A symbol is built with 8 bits as shown in the following figure.




#### *ISO Examples*

The ISO15693 protocol, mode 1 out of 4, is implemented using six symbols as shown in the following table. Start of frame (SOF), end of frame (EOF) and pulses are all encoded using one symbol.

| ISO15693 (1 out of 4) | | |
|---|---|---|
| Symbol | Name | Code |
| Sym0 | Pulse1 | 10111111 |
| Sym1 | Pulse2 | 11101111 |
| Sym2 | Pulse3 | 11111011 |
| Sym3 | Pulse4 | 11111110 |
| Sym4 | SOF | 01111011 |
| Sym5 | EOF | 11011111 |

The ISO15693 protocol, mode 1 out of 256, is implemented using three symbols. Start of frame (SOF), end of frame (EOF) and pulses encoding result of the combination of these three symbols.

| ISO15693 (1 out of 256) | |
|---|---|
| Symbol | Code |
| Sym0 | 11111111 |
| Sym1 | 11110000 |
| Sym2 | 00001111 |

| ISO15693 (1 out of 256) | |
|---|---|
| Name | Combination |
| SOF | Sym2+2*Sym0+Sym1 |
| EOF | Sym0+Sym2 |
| Pulse 1 to 256 | 255*Sym0+Sym1 |

***Note***

- The position of the symbol Sym1 encodes pulses from 1 to 256. For example: Pulse1 = Sym1 + 255*Sym0 and Pulse45 = 44*Sym0 + Sym1 + 211*Sym0.

The ISO14443 -B protocol is implemented with only two symbols. This allows fast addressing with only one CK pulse.

| ISO14443-B | | |
|---|---|---|
| **Symbol** | **Name** | **Code** |
| Sym0 | L | 00000000 |
| Sym1 | H | 11111111 |

***Time Reference Setup***

The time reference is defined in the EncoderTimeRef register. The time reference contains the value of one bit time. Hence $Symbol\_Time = 8 * Bit\_Time$

The bit time is defined by the EncTimeRef parameter. EncTimeRef is an integer value, it is calculated as follows:

$$EncTime\,\mathrm{Re}\,f = \left( \frac{Bit\_Time}{1/3.39Mhz} \right) - 1$$

EncTimeRef is coded on 5 bits. This means that Bit_Time_max = 9.44µs and Symbol_Time_max = 75.52µs.

***ISO Examples***

| Norm | Symbol Time | Bit Time | EncTimeRef |
|---|---|---|---|
| ISO15693 (1 out of 4) | 75.52 µs | 9.44 µs | 0x1F (11111) |
| ISO15693 (1 out of 256) | 18.88 µs | 2.36 µs | 0x07 (00111) |
| ISO14443B | 9.44 µs | 1.18 µ | 0x03 (00011) |

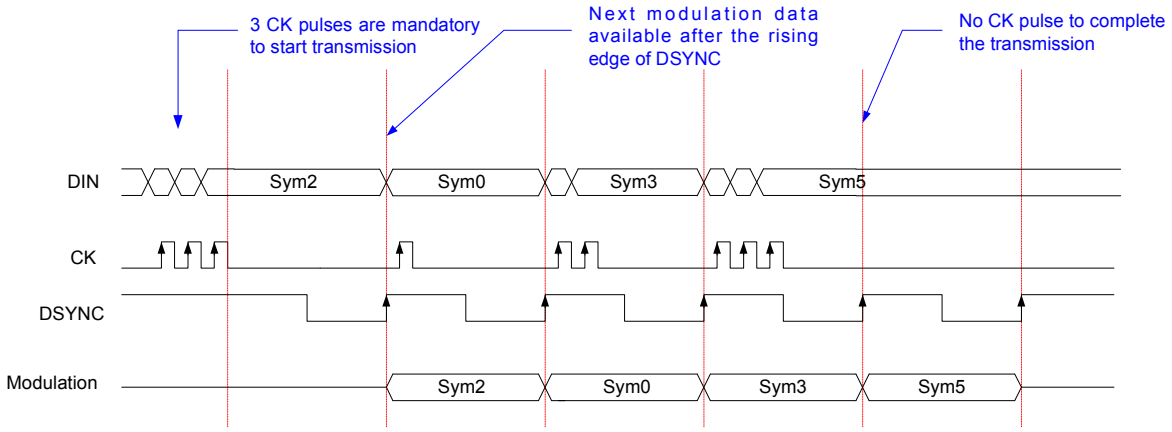
### *Symbol Transmission*

CK and DIN inputs are used to transmit symbols. On each rising edge of the CK signal, DIN is sampled to encode the address of the corresponding symbol. This means that each address of the seven available symbols can be encoded with a maximum of three bits (meaning three CK pulses). To reduce the usage of the microcontroller for fast protocol, Sym0 and Sym1 can be transmitted with only one bit and, Sym2 and Sym3 with two bits, as shown in the following table.

| Symbol | First Symbol<br>3 bits are needed to initiate Transmission | Subsequent Symbols<br>Reduced encoding possible (minimum 1 bit) |
|---|---|---|
| Sym0 | 000 | 0 |
| Sym1 | 001 | 1 |
| Sym2 | 010 | 10 |
| Sym3 | 011 | 11 |
| Sym4 | 100 | 100 |
| Sym5 | 101 | 101 |
| Sym6 (*) | 110 | 110 |

(*) Symbol 6 is hard coded to 0xFF (11111111).

To initiate a transmission, it is necessary to send the first symbol with three CK pulses to initialize the communication. On every rising edge of DSYNC, the following symbol is sent. To complete the transmission, no more CK pulse should be sent after EOF symbol.




| Signal | Assign |
|---|---|
| MODE | 1 |
| RTB | 0 |
| DIN | Symbol to transmit |
| CK | Clock |
| DOUT | x |
| DSYNC | Symbol Synchronization |

### *11.3.2. Reception*

#### *11.3.2.a. Analog Setup*

For a proper reception, the analog chain has to be configured according to the following parameters in the AnalogConfig register:

- ByPassAll: It bypasses the analog filters in the analog chain. Must be enabled for AM reception.
- RSub-carrier: It selects the reception sub-carrier frequency – See table.

| RSub-carrier | Sub-carrier |
|---|---|
| 0 | 423 / 484 kHz |
| 1 | 847 kHz |

***ISO Examples***

| Standard | ByPassAll | RSub-carrier |
|---|---|---|
| ISO15693-Single Sub-carrier | 1 | 0 |
| ISO15693-Dual Sub-carrier | 0 | 0 |
| ISO14443-B | 0 | 1 |

### *11.3.2.b. Direct Reception*

After analog processing, data reception can be either direct or pre-processed by hardware accelerators, according to the configuration of the SelDOUT parameter in the DigitalConfig register.

| SelDout | Output | Hardware | ISO Standard |
|---|---|---|---|
| 00 | AM (direct) | -- | ISO15693-Single Sub-carrier |
| 01 | FM (direct) | -- | -- |
| 10 | FSK (423/484 kHz) | FSK decoder | ISO15693-Dual Sub-carrier |
| 11 | PSK (847 kHz) | PSK decoder | ISO14443-B |

***Note***

- The output phase of PSK decoder is either normal or inverted.

Direct reception is achieved with the following setup.

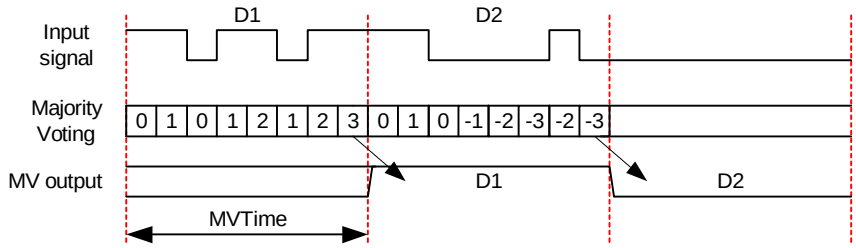
| Signal | Assign |
|---|---|
| MODE | 1 |
| RTB | 1 |
| DIN | 1 |
| CK | 0 |
| DOUT | Received data |
| DSYNC | x |

### *11.3.2.c. Reception with Majority Voting (MV)*

Majority voting allows to:

- Filter noisy signal,
- Compensate for jitter,
- Correct distorted signals.

At the beginning of the time slot (MVTime), an up / down counter is reset. When the input signal is asserted high, it is counting up and when the input signal is asserted low, it is counting down. At the end of time slot, the counter value is checked and the output value is set accordingly (low if counter is negative; high if counter is positive).




***Majority Voting Setup***

The following parameters in the DigitalConfig register have to be set when using majority voting.

- MVEn: it enables the majority voting function.
- DecTimeRef: it defines the duration of the time slot (MVTime)

$$DecTime\,\mathrm{Re}\,f = \left(\frac{MVTime}{1/6.78Mhz}\right) - 1$$

$$MVTime\_\max = 37.76\mu s$$

***ISO examples***

| Norm | MVTime | DecTimeRef |
|---|---|---|
| ISO15693 Single Sub-carrier – high baud rate | 18.88µs (half bit) | 127 |
| ISO15693 Dual Sub-carrier – high baud rate | 18.73µs (half bit) | 126 |
| ISO15693 Single Sub-carrier – low baud rate | 37.6µs (quarter bit) | 255 |
| ISO15693 Dual Sub-carrier – low baud rate | 37.46µs (quarter bit) | 253 |
| ISO1444-B | 9.44µs (full bit) | 63 |

***Note***

- For Manchester coding, majority voting is on half bit portions only.

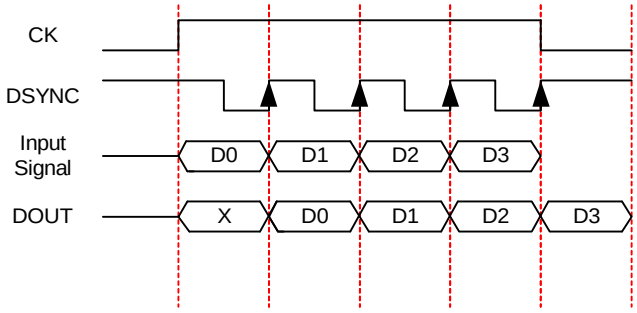
In addition, the MVMode parameter in the DigitalConfig register allows giving more weight to low input levels.

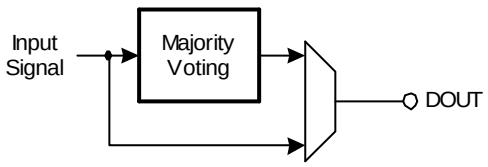
***Note***

- It is highly recommended to use Majority Voting for all ISO standard configurations.

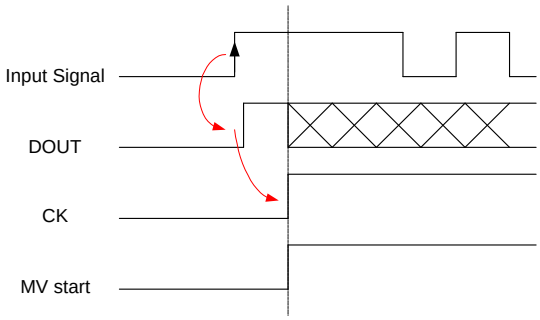
***MV Reception***

To start a reception with majority voting function, assert CK high at the beginning of the response. Then take data on every falling edge of DSYNC. Reception is stopped by asserting CK low on the last rising edge of DSYNC. Data output are delayed by DecTimeRef (see next figure).



***Example in ISO1569-Dual Sub-carrier***



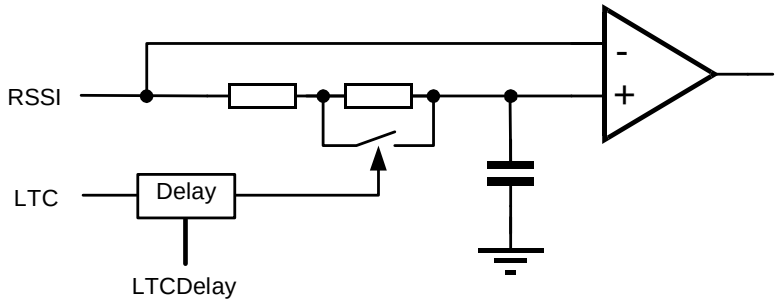

| Standard | Reference for input signal |
|---|---|
| ISO15693-Single Sub-carrier | Rising edge |
| ISO15693-Dual Sub-carrier | Rising edge |
| ISO14443-B | Rising / Falling edge |

***Data Slicer***

LTC is an internal signal which controls the time constant of the comparator. This signal is switched to ensure a proper decoding in ASK modes in order to improve the reading performances.

LTC is controlled according to the following parameters in the LTC register:

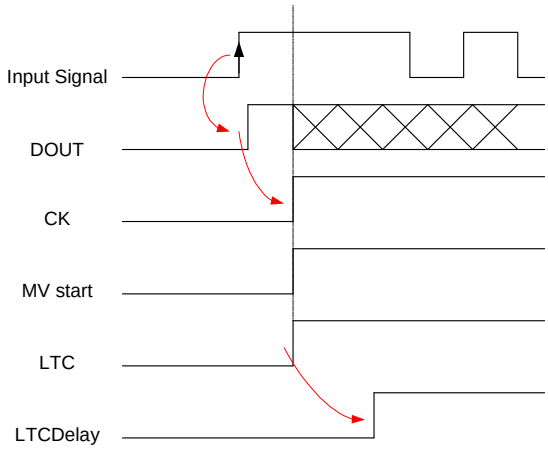
- LTCEn: it enables the LTC circuit.
- LTCDelay: delay to switch the time constant (see next table).




***Recommended delay for ISO standard***

| Standard | DelayTime | LTCDelay |
|---|---|---|
| ISO15693-Single Sub-carrier | 4.72µs | 0x1F |

***Example in ISO15693-Single Sub-carrier***



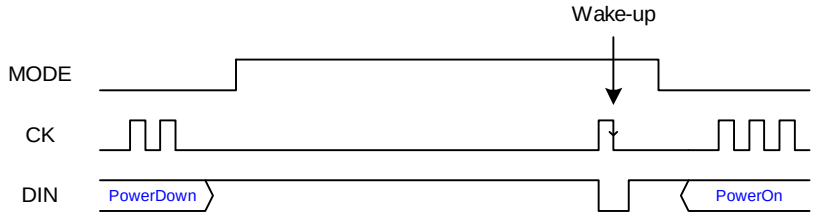

## 11.4. Power Modes

This chip has three power modes. To select one of these modes write the PowerState parameter in the PowerState register.

| PowerState | Power Mode | Symbol |
|---|---|---|
| 00 | Low Power | $I_{idle}$ |
| 01 | Transmitter On | $I_{tr}$ |
| 11 | Power Down | $I_{stb}$ |

***Power Down***

If the Power Down mode is selected, the crystal oscillator will be turned off. Therefore, it will be impossible to write the PowerState register to wake up the chip. To wake up the chip, it is necessary to send a falling edge on CK when DIN is low. During Power Down mode, keep DIN high to avoid glitches on CK.




***Notes***

- After a wake-up, the chip has to be set in Transmitter On or Low Power mode by updating the PowerState register, after $T_{start}$.

***Low Power***

The oscillator is still on but all analog circuitry is off.

## 11.5. BUF Output

The XBUF pin can be used to clock a device or a microcontroller. By default the output is enabled with a frequency of 6.78MHz. The frequency can be doubled to 13.56MHz by setting the bit XBUFSel. When the output is not used, it is recommended to disable the clock by setting the bit XBUFEnB.

## 12. Configuration Registers

The following tables explain the meaning of the bit configurations in the 13 registers.

| **Register : AnalogConfig**<br>**Address : 0** | | | |
|---|---|---|---|
| **Bit** | **Default** | **Name** | **Function** |
| 7 | 0 | XBUFSel | XBUF frequency selection (0 = 6.78MHz, 1 = 13.56MHz ) |
| 6 | 0 | XBUFEnB | XBUF Enable (0= Enabled, 1 = Disabled) |
| 5 | 0 | TModIndex | Transmission Modulation Index (0 = 100%, 1= 10%) |
| 4 | 0 | RSub-carrier | Reception Sub-carrier (0 = 450K , 1 = 847K) – See notes |
| 3 | 0 | Reserved | Do not use – Should always be configured at 0 |
| 2 | 0 | ByPassAll | Bypass analog chain (0= Connected, 1 = Bypassed) – See notes |
| 1:0 | 0 | Reserved | Do not use - Should always be configured at 11 |

***Notes***

| **ByPassAll** | **Demodulation** |
|---|---|
| 0 | FSK / PSK |
| 1 | ASK |

| **RSub-carrier** | **Sub-carrier frequency** |
|---|---|
| 0 | 423 / 484 kHz |
| 1 | 847 kHz |

| **Register : PowerState**<br>**Address : 1** | | | |
|---|---|---|---|
| Bit | Default | Name | Function |
| 7:2 | 0 | Reserved | Do not use |
| 1:0 | 0 | PowerState | Chip Power State – See notes |

***Notes***

| **Power State [1:0]** | | **Mode** |
|---|---|---|
| 0 | 0 | Idle (oscillator on) |
| 0 | 1 | Transmitter On |
| *1* | *0* | *Unused* |
| 1 | 1 | Power Down (oscillator off) |

| Register : Reserved<br>Address : 2 | | | |
|---|---|---|---|
| **Bit** | **Default** | **Name** | **Function** |
| 7:0 | 0 | Reserved | Do not use |

| Register : DigitalConfig<br>Address : 3 | | | |
|---|---|---|---|
| **Bit** | **Default** | **Name** | **Function** |
| *7:6* | *0* | -- | *Unused* |
| 5 | 0 | Reserved | Do not use |
| 4 | 0 | MVMode | Majority Voting Mode (0 = ISO15693 / ISO14443B) |
| 3 | 0 | MVEn | Majority Voting Enable (0 = Disabled, 1 = Enabled) |
| 2:1 | 0 | SelDout | Reception Output Selection (see table) |
| 0 | 0 | EncoderEn | Hardware Encoder Enable (0 = Disabled, 1 = Enabled) |

***Notes***

| SelDout | Output |
|---|---|
| 00 | AM (DATA): '1' = sub carrier ; '0' = no sub carrier |
| 01 | FM (LIMITER): rough digital signal |
| 10 | FSK decoded: '1' when f = 423kHz, '0' when f = 484kHz |
| 11 | PSK decoded |

| Register : EncoderSym<br>Address : 4 to 9 | | | |
|---|---|---|---|
| **Bit** | **Default** | **Name** | **Function** |
| 7:0 | 0 | EncoderSym0 | Encoder Symbol 0 |
| 7:0 | 0 | EncoderSym1 | Encoder Symbol 1 |
| 7:0 | 0 | EncoderSym2 | Encoder Symbol 2 |
| 7:0 | 0 | EncoderSym3 | Encoder Symbol 3 |
| 7:0 | 0 | EncoderSym4 | Encoder Symbol 4 |
| 7:0 | 0 | EncoderSym5 | Encoder Symbol 5 |

***Notes***

- Symbol 6 is hard-coded to 0xFF (11111111).

| Register : EncoderTimeRef<br>Address : A | | | |
|---|---|---|---|
| **Bit** | **Default** | **Name** | **Function** |
| *7:5* | *0* | -- | *Unused* |
| 4:0 | 0 | EncTimeRef | Encoder Time Reference |

| Register : DecoderTimeRef<br>Address : B | | | |
|---|---|---|---|
| **Bit** | **Default** | **Name** | **Function** |
| 7:0 | 0 | DecTimeRef | Decoder Time Reference |

| Register : LTC<br>Address : C | | | |
|---|---|---|---|
| **Bit** | **Default** | **Name** | **Function** |
| *7:6* | *0* | -- | *Unused* |
| 5:1 | 0 | LTCDelay | LTC Delay |
| 0 | 0 | LTCEn | LTC Enable (0=Disabled, 1 = Enabled) |

## 13. Configuration Registers: ISO Configuration Examples

| | **Norm** | **ISO15693** | | **ISO14443** |
|---|---|---|---|---|
| **Address** | **Register** | **ASK**<br>High Baud Rate<br>100% modulation | **FSK**<br>High Baud Rate<br>10% modulation | **B Type** |
| 0 | AnalogConfig | 47 | 63 | 73 |
| 1 | PowerState* | 01 | 01 | 01 |
| 2 | Reserved | 00 | 00 | 00 |
| 3 | DigitalConfig | 09 | 0D | 0F |
| 4 | EncoderSym0 | BF | BF | 00 |
| 5 | EncoderSym1 | EF | EF | FF |
| 6 | EncoderSym2 | FB | FB | 00 |
| 7 | EncoderSym3 | FE | FE | 00 |
| 8 | EncoderSym4 | 7B | 7B | 00 |
| 9 | EncoderSym5 | DF | DF | 00 |
| 10 | EncoderTimeRef | 1F | 1F | 03 |
| 11 | DecoderTimeRef | 7F | 7E | 3F |
| 12 | LTC | 3F | 00 | 00 |

***Notes***

- All values are in hexadecimal notation.
- Transmitter is switched on.

## *14. Standard information regarding manufacturability of Melexis products with different soldering processes*

Our products are classified and qualified regarding soldering technology, solderability and moisture sensitivity level according to following test methods:

**Reflow Soldering SMD's (Surface Mount Devices)**

- IPC/JEDEC J-STD-020
  Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices
  (classification reflow profiles according to table 5-2)
- EIA/JEDEC JESD22-A113
  Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing
  (reflow profiles according to table 2)

**Wave Soldering SMD's (Surface Mount Devices) and THD's (Through Hole Devices)**

- EN60749-20
  Resistance of plastic- encapsulated SMD's to combined effect of moisture and soldering heat
- EIA/JEDEC JESD22-B106 and EN60749-15
  Resistance to soldering temperature for through-hole mounted devices

**Iron Soldering THD's (Through Hole Devices)**

- EN60749-15
  Resistance to soldering temperature for through-hole mounted devices

**Solderability SMD's (Surface Mount Devices) and THD's (Through Hole Devices)**

- EIA/JEDEC JESD22-B102 and EN60749-21
  Solderability

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

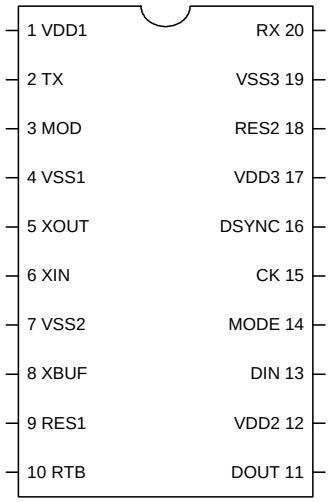
Melexis is contributing to global environmental conservation by promoting **lead free** solutions. For more information on qualifications of **RoHS** compliant products (RoHS = European directive on the Restriction Of the use of certain Hazardous Substances) please visit the quality page on our website: http://www.melexis.com/quality.asp.

## *15. ESD Precautions*

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD).
Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

## 16. Package Information

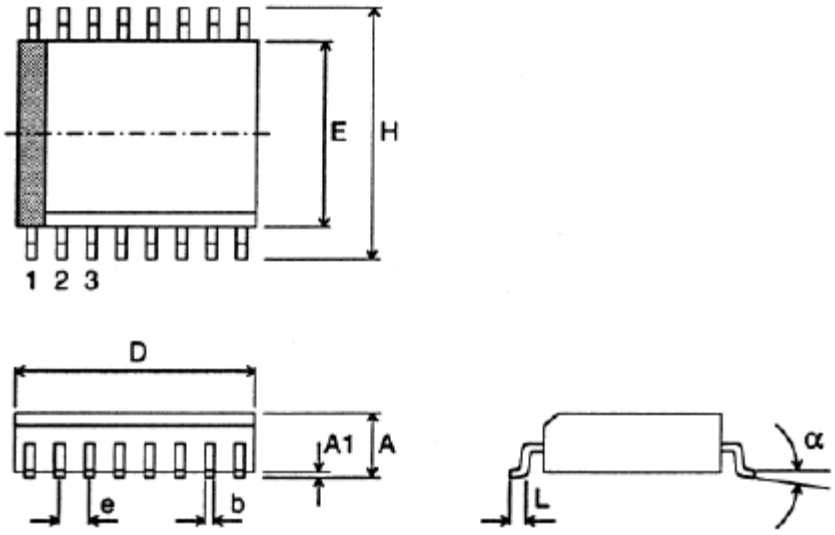
The device is packaged in a 20 pin lead free SSOP package.




| Pin # | Symbol | Pin Type | Description |
|---|---|---|---|
| 1 | VDD1 | Supply | Transmitter power supply |
| 2 | TX | Analog | Output transistor drain connection |
| 3 | MOD | Analog | External resistor to set modulation depth |
| 4 | VSS1 | Supply | Transmitter section ground |
| 5 | XOUT | Dig-Out | Output of crystal resonator |
| 6 | XIN | Dig-In | Input of crystal resonator and external system clock input |
| 7 | VSS2 | Supply | Digital section ground |
| 8 | XBUF | Dig-Out | Buffered output of crystal oscillator |
| 9 | RES1 | Reserved | Should be grounded for normal operation |
| 10 | RTB | Dig-In | Receive/Transmit selection |
| 11 | DOUT | Dig-Out | Data output |
| 12 | VDD2 | Supply | Digital section power supply |
| 13 | DIN | Dig-In | Data input for registers or modulation |
| 14 | MODE | Dig-In | Configuration/Communication selection |
| 15 | CK | Dig-In | Serial clock input |
| 16 | DSYNC | Dig-Out | Data synchronization output |
| 17 | VDD3 | Supply | Receiver section power supply |
| 18 | RES2 | Reserved | Should be left unconnected for normal operation |
| 19 | VSS3 | Supply | Receiver section ground |
| 20 | RX | Ana-In | Receiver input |

Moisture Sensitivity Level is MSL3, according as per IPC/JEDEC J-STD-20.

The mechanical dimensions of this package are depicted on the following page.




**Shrink Small Outline Package (SSOP)**

SSOP 20, 24, 28

| Package type | | D | E | H | A | A 1 | e | b | L | α | Package Code |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SSOP 20 | min | 6.60 | 5.00 | 7.40 | | 0.05 | 0.65 | 0.22 | 0.63 | 0° | FR20 |
| | max | 7.50 | 5.60 | 8.20 | 2.13 | 0.25 | | 0.38 | 1.03 | 8° | |
| SSOP 24 | min | 7.90 | 5.00 | 7.40 | | 0.05 | 0.65 | 0.22 | 0.63 | 0° | FR24 |
| | max | 8.50 | 5.60 | 8.20 | 2.13 | 0.25 | | 0.38 | 1.03 | 8° | |
| SSOP 28 | min | 9.90 | 5.00 | 7.40 | | 0.05 | 0.65 | 0.22 | 0.63 | 0° | FR28 |
| | max | 10.50 | 5.60 | 8.20 | 2.13 | 0.25 | | 0.38 | 1.03 | 8° | |

**Dimension: mm, coplanarity < 0,1 mm, original dimension: inch**

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