## **General Purpose Amplifier**

## **NPN Silicon**

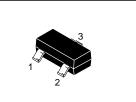
#### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V <sub>CEO</sub>	40	Vdc
Emitter-Base Voltage	V <sub>EBO</sub>	4.0	Vdc
Collector Current — Continuous	Ι <sub>C</sub>	100	mAdc

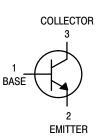
#### THERMAL CHARACTERISTICS

Characteristic	Symbol	Мах	Unit
Total Device Dissipation FR–5 Board <sup>(1)</sup>	PD	225	mW
T <sub>A</sub> = 25°C Derate above 25°C		1.8	mW/°C
Thermal Resistance Junction to Ambient	$R_{\thetaJA}$	556	°C/W
Total Device Dissipation Alumina Substrate, <sup>(2)</sup> $T_A = 25^{\circ}C$	PD	300	mW
Derate above 25°C		2.4	mW/°C
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	417	°C/W
Junction and Storage Temperature	T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C

# MMBTA20LT1



CASE 318-08, STYLE 6 SOT-23 (TO-236AB)



## DEVICE MARKING

 $\mathsf{MMBTA20LT1} = \mathsf{1C}$ 

**ELECTRICAL CHARACTERISTICS** ( $T_A = 25^{\circ}C$  unless otherwise noted)

Characteristic		Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Breakdown Voltage $(I_C = 1.0 \text{ mAdc}, I_B = 0)$	V <sub>(BR)CEO</sub>	40	_	Vdc
Emitter–Base Breakdown Voltage $(I_E = 100 \ \mu Adc, I_C = 0)$	V <sub>(BR)EBO</sub>	4.0	_	Vdc
Collector Cutoff Current ( $V_{CB} = 30 \text{ Vdc}, I_E = 0$ )	I <sub>CBO</sub>	—	100	nAdc

1. FR–5 = 1.0  $\times$  0.75  $\times$  0.062 in.

2. Alumina = 0.4  $\times$  0.3  $\times$  0.024 in. 99.5% alumina.

#### **ELECTRICAL CHARACTERISTICS** ( $T_A = 25^{\circ}C$ unless otherwise noted) (Continued)

Characteristic		Min	Max	Unit
ON CHARACTERISTICS				
DC Current Gain (I <sub>C</sub> = 5.0 mAdc, V <sub>CE</sub> = 10 Vdc)	h <sub>FE</sub>	40	400	—
Collector–Emitter Saturation Voltage $(I_C = 10 \text{ mAdc}, I_B = 1.0 \text{ mAdc})$	V <sub>CE(sat)</sub>	_	0.25	Vdc
SMALL-SIGNAL CHARACTERISTICS				
Current–Gain — Bandwidth Product ( $I_C = 5.0 \text{ mAdc}$ , $V_{CE} = 10 \text{ Vdc}$ , f = 100 MHz)	f <sub>T</sub>	125	_	MHz
Output Capacitance (V <sub>CB</sub> = 10 Vdc, I <sub>E</sub> = 0, f = 1.0 MHz)	C <sub>obo</sub>	—	4.0	pF

#### EQUIVALENT SWITCHING TIME TEST CIRCUITS

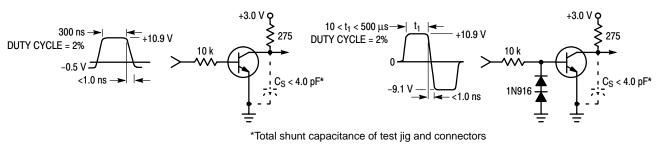
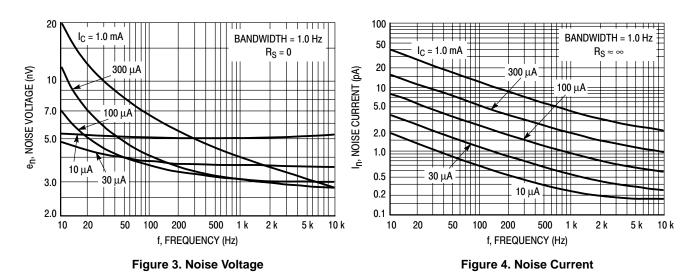


Figure 1. Turn–On Time

Figure 2. Turn-Off Time

**TYPICAL NOISE CHARACTERISTICS** 



 $(V_{CE} = 5.0 \text{ Vdc}, T_A = 25^{\circ}C)$ 

#### NOISE FIGURE CONTOURS

 $(V_{CE}=5.0~Vdc,~T_{A}=25^{\circ}C)$ 

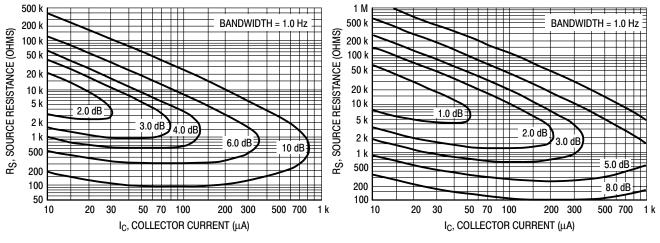
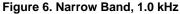
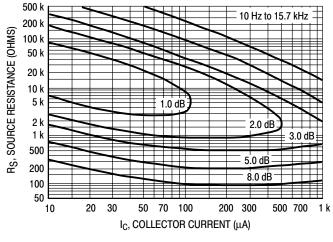
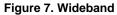


Figure 5. Narrow Band, 100 Hz







Noise Figure is defined as:

$$\mathsf{NF} \,=\, 20 \, \mathsf{log_{10}} \Big( \frac{\mathsf{e_n}^2 \,+\, \mathsf{4KTR}_S \,+\, \mathsf{I_n}^{\,\, 2} \mathsf{R_S}^2}{\mathsf{4KTR}_S} \Big)^{1/2}$$

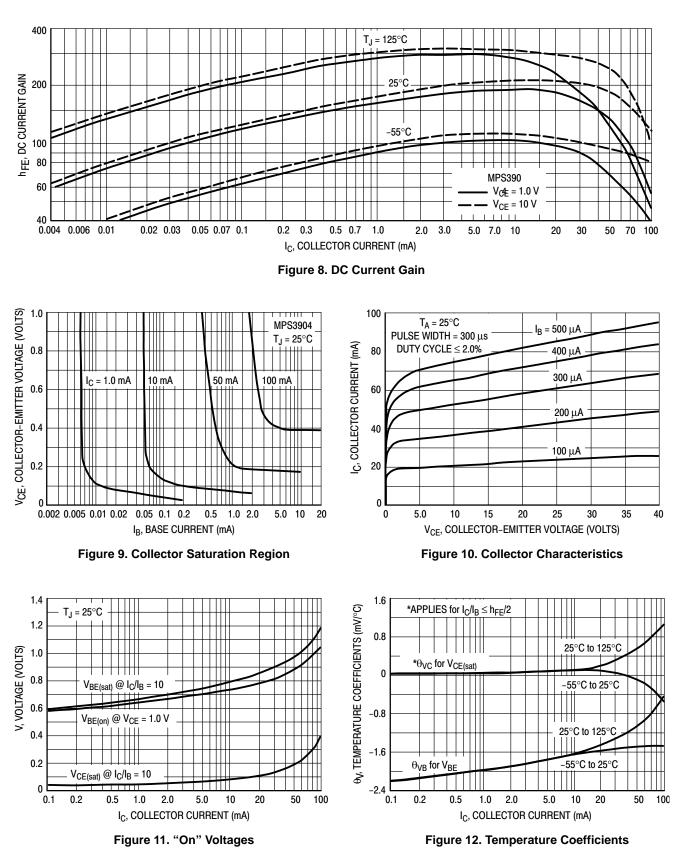
 $e_n$  = Noise Voltage of the Transistor referred to the input. (Figure 3)

 $I_n$  = Noise Current of the Transistor referred to the input. (Figure 4)

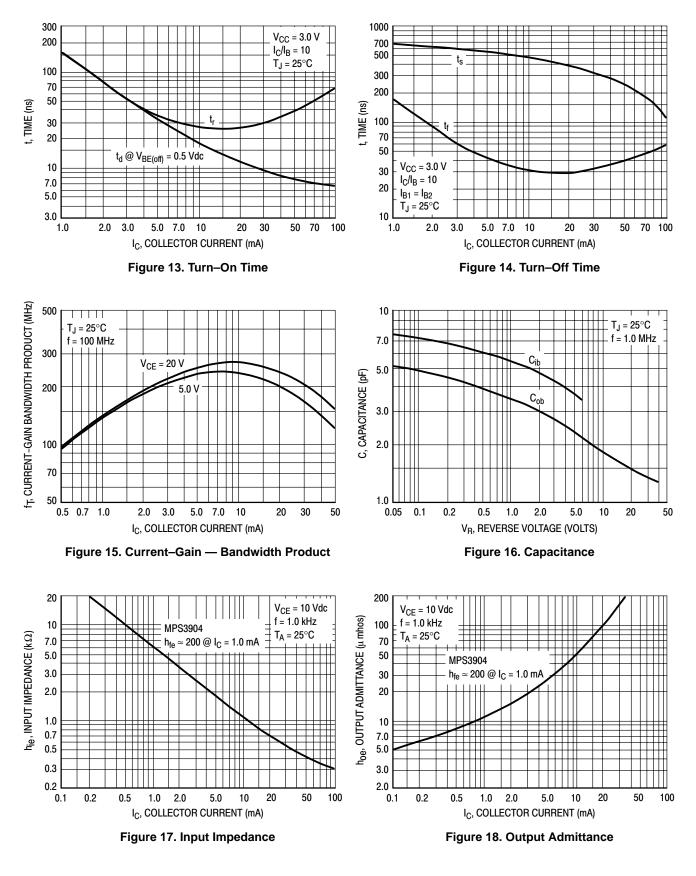
K = Boltzman's Constant (1.38 x 10<sup>-23</sup> j/°K)

- T = Temperature of the Source Resistance ( $^{\circ}$ K)
- R<sub>S</sub> = Source Resistance (Ohms)

#### **TYPICAL STATIC CHARACTERISTICS**



#### **TYPICAL DYNAMIC CHARACTERISTICS**



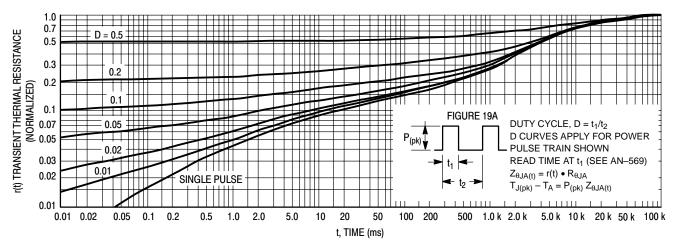


Figure 19. Thermal Response

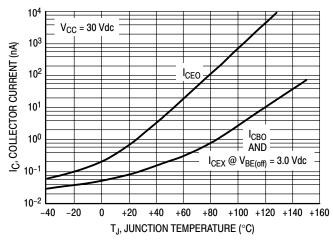


Figure 19A.

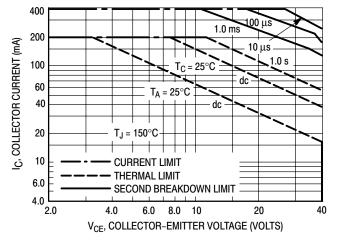


Figure 20.

#### DESIGN NOTE: USE OF THERMAL RESPONSE DATA

A train of periodical power pulses can be represented by the model as shown in Figure 19A. Using the model and the device thermal response the normalized effective transient thermal resistance of Figure 19 was calculated for various duty cycles.

To find  $Z_{\theta JA(t)}$ , multiply the value obtained from Figure 19 by the steady state value  $R_{\theta JA}$ .

Example:

The MPS3904 is dissipating 2.0 watts peak under the following conditions:

 $t_1 = 1.0 \text{ ms}, t_2 = 5.0 \text{ ms}. (D = 0.2)$ 

Using Figure 19 at a pulse width of 1.0 ms and D = 0.2, the reading of r(t) is 0.22.

The peak rise in junction temperature is therefore

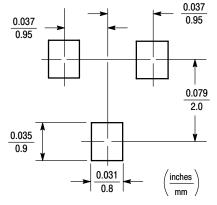
 $\Delta T = r(t) \ge P_{(pk)} \ge R_{\theta JA} = 0.22 \ge 2.0 \ge 200 = 88^{\circ}C.$ For more information, see AN–569.

The safe operating area curves indicate  $I_C-V_{CE}$  limits of the transistor that must be observed for reliable operation. Collector load lines for specific circuits must fall below the limits indicated by the applicable curve.

The data of Figure 20 is based upon  $T_{J(pk)} = 150^{\circ}$ C;  $T_{C}$  or  $T_{A}$  is variable depending upon conditions. Pulse curves are valid for duty cycles to 10% provided  $T_{J(pk)} \le 150^{\circ}$ C.  $T_{J(pk)}$  may be calculated from the data in Figure 19. At high case or ambient temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

### INFORMATION FOR USING THE SOT-23 SURFACE MOUNT PACKAGE MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



SOT-23 SOT-23 POWER DISSIPATION

The power dissipation of the SOT–23 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by  $T_{J(max)}$ , the maximum rated junction temperature of the die,  $R_{\theta JA}$ , the thermal resistance from the device junction to ambient, and the operating temperature,  $T_A$ . Using the values provided on the data sheet for the SOT–23 package,  $P_D$  can be calculated as follows:

$$P_{D} = \frac{T_{J(max)} - T_{A}}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature  $T_A$  of 25°C, one can calculate the power dissipation of the device which in this case is 225 milliwatts.

$$P_{D} = \frac{150^{\circ}C - 25^{\circ}C}{556^{\circ}C/W} = 225 \text{ milliwatts}$$

The 556°C/W for the SOT–23 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 225 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT–23 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad<sup>™</sup>. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

#### SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

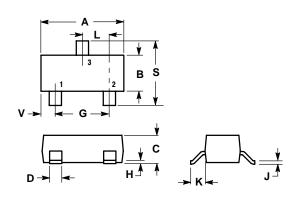
- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.\*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

\* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

#### PACKAGE DIMENSIONS

SOT-23 (TO-236) CASE 318-08 **ISSUE AF** 

NOTES



1. DIMENSIONING AND TOLERANCING PER ANSI

Y14.5M, 1982. CONTROLLING DIMENSION: INCH. 2

MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS, MINIMUM LEAD THICKNESS 3. IS THE MINIMUM THICKNESS OF BASE MATERIAL

	INCHES		MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.1102	0.1197	2.80	3.04
В	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
Н	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0140	0.0285	0.35	0.69
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60

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