PA69

FEATURES

- A UNIQUE (Patent Pending) TECHNIQUE FOR VERY LOW QUIESCENT CURRENT < 1 mA
- OVER 200 V/µS SLEW RATE
- WIDE SUPPLY VOLTAGE
  - SINGLE SUPPLY: 10V to 200V
  - SPLIT SUPPLIES: +/- 10V to +/- 100V
- OUTPUT CURRENT- 50mA cont. ; 100mA Pk
- UP TO 23 WATT DISSIPATION CAPABILITY
- OVER 200 kHz POWER BANDWIDTH
- LOW COST

APPLICATIONS

- PIEZOELECTRIC POSITIONING AND ACTUATION
- ELECTROSTATIC DEFLECTION
- DEFORMABLE MIRROR ACTUATORS
- CHEMICAL AND BIOLOGICAL STIMULATORS

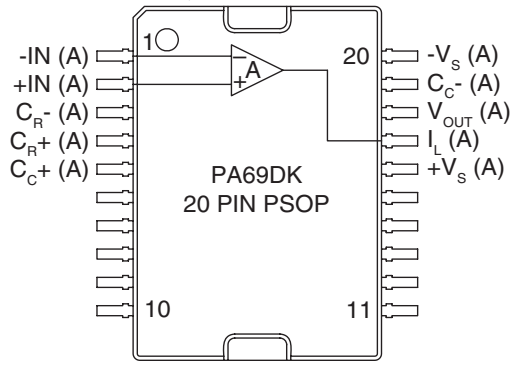
DESCRIPTION

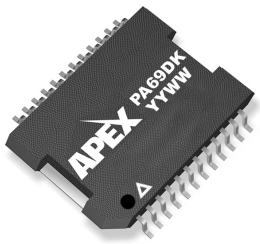
The PA69 is a high voltage, high speed Precision IC power op amp with performance and unique features not found previously in any commercially available OpAmp .

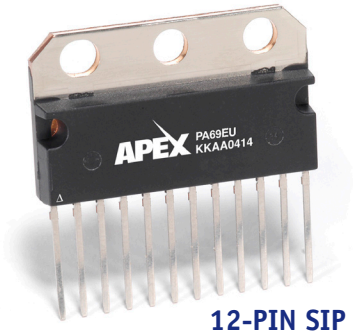
Novel input stage design of this amplifier provides extremely high slew rates in pulse applications while maintaining low quiescent current of under 1mA. This novel input stage also has the effect of adding variables to the power response and slew rate characteristics of the amplifier. To a lesser degree, there are also input related effects on open loop gain and phase. It is important to note that slew rate for the PA69 is independent of supply current. However the slew rate is a strong function of input voltage amplitude. **It should be noted that the package tab needs to be connected to a stable reference such as GND for high slew rates. Please refer to special considerations section for details.**

The output stages are well protected with user defined current limit although the Safe Operating Area (SOA) must be observed for reliable protection. Proper heatsinking is required for maintaining maximum reliability. External phase compensation provides the user with great flexibility in trading gain, stability and bandwidth.

EXTERNAL CONNECTIONS - EU PACKAGE



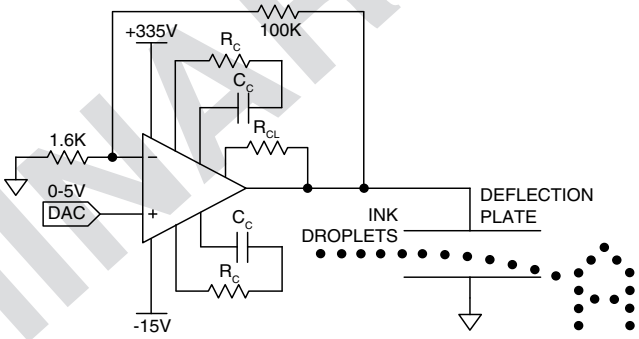




24-PIN PSOP
PACKAGE STYLE DK

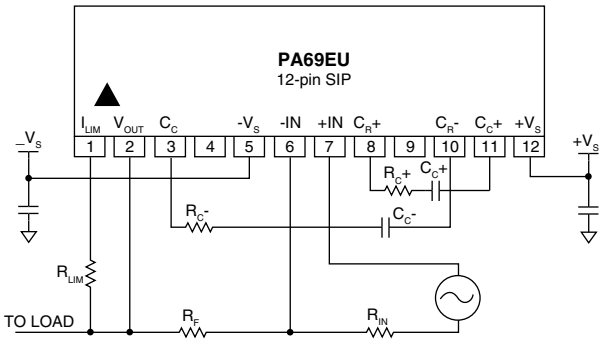
12-PIN SIP
PACKAGE STYLE EU
LEAD FORM EW

TYPICAL APPLICATION



The PA69 is ideally suited to driving continuous drop ink jet systems, in both piezo actuation and deflection applications. The deflection amplifier shown above achieves accurate droplet displacement at high speeds to deposit crisp, clear lot code information on product containers. The external compensation networks have been optimized to match the gain of the circuit and the complex impedance of the load. The combination of high voltage and high speed allow repeatable low cost deflection of droplets for high production environments.

EXTERNAL CONNECTIONS - EU PACKAGE



ABSOLUTE MAXIMUM RATINGS

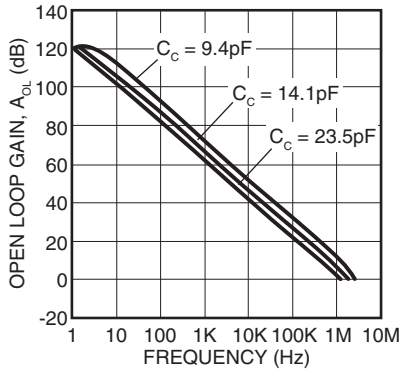
SUPPLY VOLTAGE, $+V_S$ to $-V_S$	200V
OUTPUT CURRENT, peak	100mA, within SOA
POWER DISSIPATION, internal, DC	23W
INPUT VOLTAGE, Differential	±15V
INPUT VOLTAGE, Common Mode	±Vs
TEMPERATURE, pin solder, 10s	300
TEMPERATURE, junction[2]	150°C.
TEMPERATURE RANGE, storage	–55 to 125°C.
OPERATING TEMPERATURE, case	-40 to 125°C

SPECIFICATIONS

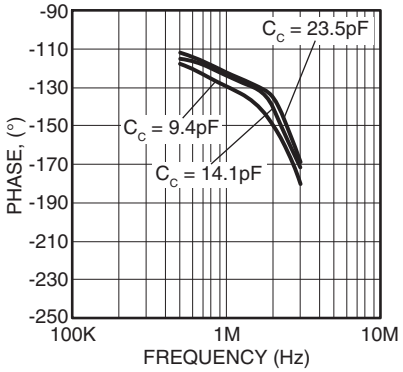
PARAMETER	TEST CONDITIONS[1]	MIN	TYP	MAX	UNITS
INPUT					
OFFSET VOLTAGE			8	25	mV
OFFSET VOLTAGE vs. temperature	0 to 125°C (Case Temperature)		-63		µV/°C
OFFSET VOLTAGE vs. supply					µV/V
BIAS CURRENT, initial[3]			8.5		pA
BIAS CURRENT vs. supply					pA/V
OFFSET CURRENT, initial			12		pA
INPUT RESISTANCE, DC			10^6		Ω
INPUT CAPACITANCE					pF
COMMON MODE VOLTAGE RANGE, pos.			$+V_S$ - 2		V
COMMON MODE VOLTAGE RANGE, neg.			$-V_S$ + 5.5		V
COMMON MODE REJECTION, DC			90		dB
NOISE	1MHz bandwidth, 1kΩR_S				µV RMS
GAIN					
OPEN LOOP @ 15Hz			120		dB
GAIN BANDWIDTH PRODUCT @ 1MHz			1		MHz
PHASE MARGIN	Full temperature range		50		°
OUTPUT					
VOLTAGE SWING	I_O = 10mA		$\|V_S\|$ - 2		V
VOLTAGE SWING	I_O = 50mA		$\|V_S\|$ - 10		V
CURRENT, continuous, DC			50		mA
SLEW RATE	**Package Tab connected to GND**		200		V/µS
SETTLING TIME, to 0.1%	2V Step		TBD		µS
POWER BANDWIDTH, $200V_{P-P}$	$+V_S$ = 100V, $-V_S$ = -100V		200		kHz
POWER SUPPLY					
VOLTAGE		±10		±100	V
CURRENT, quiescent			0.7	2.5	mA
THERMAL					
RESISTANCE, AC, junction to case[5]	Full temperature range, f ≥ 60Hz				°C/W
RESISTANCE, DC, junction to case	Full temperature range, f < 60Hz		5.5		°C/W
RESISTANCE, junction to air	Full temperature range				°C/W
TEMPERATURE RANGE, case		–40		85	°C

NOTES:
1. Unless otherwise noted: TC = 25°C, DC input specifications are ± value given, power supply voltage is typical rating.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate power dissipation to achieve high MTTF.
3. Doubles for every 10°C of temperature increase.
4. $+V_S$ and $-V_S$ denote the positive and negative supply voltages yo the output stage.
5. Rating applies if output current alternates between both output transistors at a rate faster than 60Hz.

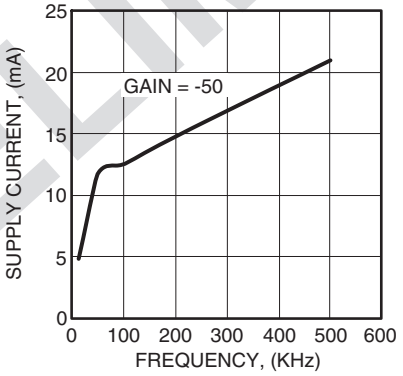
OPEN LOOP GAIN



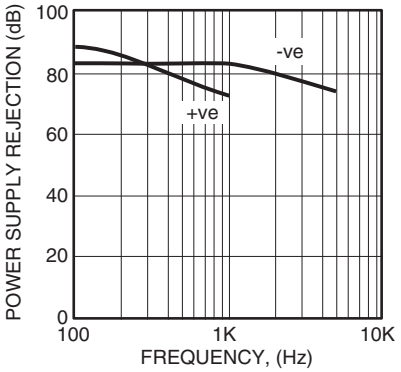
PHASE RESPONSE



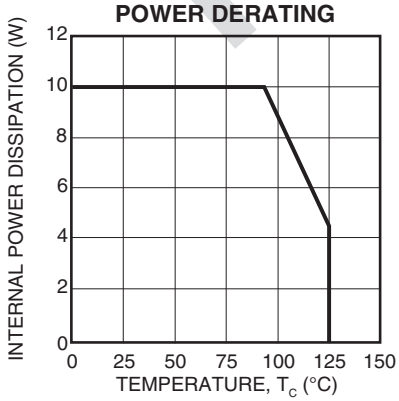
SUPPLY CURRENT vs. FREQUENCY



POWER SUPPLY REJECTION



POWER DERATING



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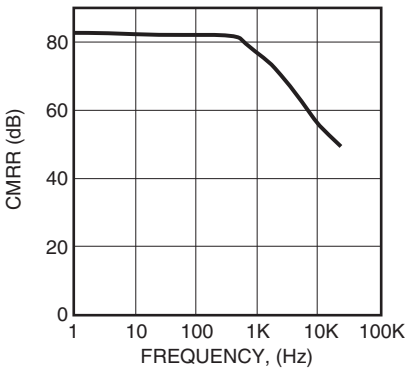


GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, power supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit, heat sink selection, Apex's complete Application Notes library, Technical Seminar Workbook and Evaluation Kits.

SPECIAL CONSIDERATIONS

It is very important to realize that in order to achieve high frequency performance the heat sink tab has to be tied to a stable, low impedance reference, i.e. power supply or GND. An AC connection through a 0.1µF capacitor is also sufficient. Internal to the PA69, the heatsink tab is electrically isolated to more than 350V . This may help allay some electrical isolation concerns in tying the heat sink to Vs or GND.

CURRENT LIMIT

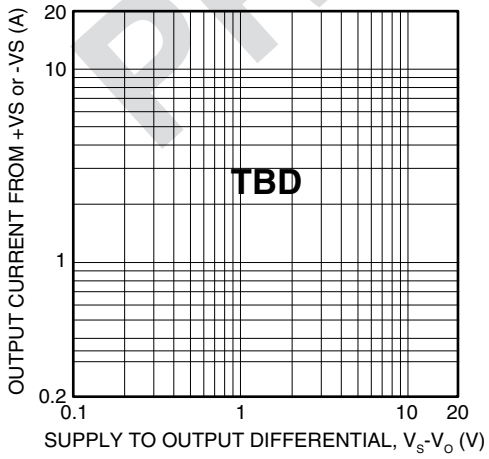
For proper operation, the current limit resistor, Rlim, must be connected as shown in the external connections diagram. For maximum reliability and protection, the resistor should be set as high as possible. The value of the resistor is calculated as follows, with Ilim in A; the maximum practical value is 1500Ω.

$$Rlim = 0.7 / Ilim$$

SAFE OPERATING AREA

The MOSFET output stage of the PA69 is not limited by second breakdown considerations as in bipolar output stages. Only thermal considerations and current handling capabilities limit the SOA. The output stage is protected against transient flyback by the parasitic body diodes of the output stage MOSFET structure. However, for protection against sustained high energy flyback external fast-recovery diodes must be used.

SAFE OPERATING AREA



POWER SUPPLY BYPASSING

Bypass capacitors to power supply terminals +Vs and –Vs must be connected physically close to the pins to prevent local parasitic oscillation in the output stage of the PA69. Use electrolytic capacitors at least 1µF. Bypass the electrolytic capacitors with high quality ceramic capacitors (X7R) 0.1µF or greater.

SUPPLY CURRENT

The PA69 features a class A/B driver stage to drive the output MOSFETs and an innovative input stage to achieve very high slew rates. The supply current drawn by the PA69, even with no load, varies with the slew rate of the output signal.

STABILITY

The PA69 is externally compensated and performance can be tailored to the application. Use the graphs of small signal response and power response as a guide. Due to the innovative design of the PA69, two compensation networks are required. The values of these components should be the same to provide symmetric slew rate characteristics. The compensation capacitor Cc must be rated at 500V working voltage. NPO capacitors are recommended. The compensation networks CcRc must be mounted closely to the amplifier pins x & y and z & w to avoid spurious oscillation.

The PA69 may require an external 33 pF capacitor (minimum breakdown of 200 V) between CC- (pin 3) and –Vs (pin 5) to prevent oscillations in the falling edge of the output. This capacitor is provided with the evaluation kit. Please refer to EK60 datasheet for details.