



# PBSS4220PANS

20 V, 2 A NPN/NPN low  $V_{CEsat}$  BISS double transistor

14 December 2015

Product data sheet

## 1. General description

NPN/NPN low  $V_{CEsat}$  Breakthrough In Small Signal (BISS) double transistor in a leadless medium power DFN2020D-6 (SOT1118D) Surface-Mounted Device (SMD) plastic package with visible and solderable side pads.

PNP/PNP complement: PBSS5220PAPS

## 2. Features and benefits

- Very low collector-emitter saturation voltage  $V_{CEsat}$
- High collector current capability  $I_C$  and  $I_{CM}$
- High collector current gain  $h_{FE}$  at high  $I_C$
- Reduced Printed-Circuit Board (PCB) requirements
- Exposed heat sink for excellent thermal and electrical conductivity
- High energy efficiency due to less heat generation
- Suitable for Automatic Optical Inspection (AOI) of solder joints
- AEC-Q101 qualified

## 3. Applications

- Load switch
- Battery-driven devices
- Power management
- Charging circuits
- LED lighting
- Power switches (e.g. motors, fans)

## 4. Quick reference data

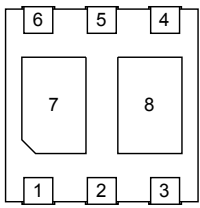
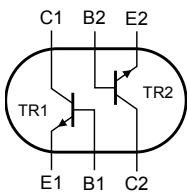
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per transistor</b>						
$V_{CEO}$	collector-emitter voltage	open base	-	-	20	V
$I_C$	collector current		-	-	2	A
$I_{CM}$	peak collector current	single pulse; $t_p \leq 1$ ms	-	-	3	A

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per transistor</b>						
R <sub>CEsat</sub>	collector-emitter saturation resistance	I <sub>C</sub> = 1 A; I <sub>B</sub> = 50 mA; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02 ; T <sub>amb</sub> = 25 °C	-	-	170	mΩ

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	E1	emitter TR1	 <p>Transparent top view <b>DFN2020D-6 (SOT1118D)</b></p>	 <p>sym140</p>
2	B1	base TR1		
3	C2	collector TR2		
4	E2	emitter TR2		
5	B2	base TR2		
6	C1	collector TR1		
7	C1	collector TR1		
8	C2	collector TR2		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PBSS4220PANS	DFN2020D-6	DFN2020D-6: plastic, thermally enhanced ultra thin and small outline package; no leads; 6 terminals; body 2 x 2 x 0.65 mm	SOT1118D

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PBSS4220PANS	3M

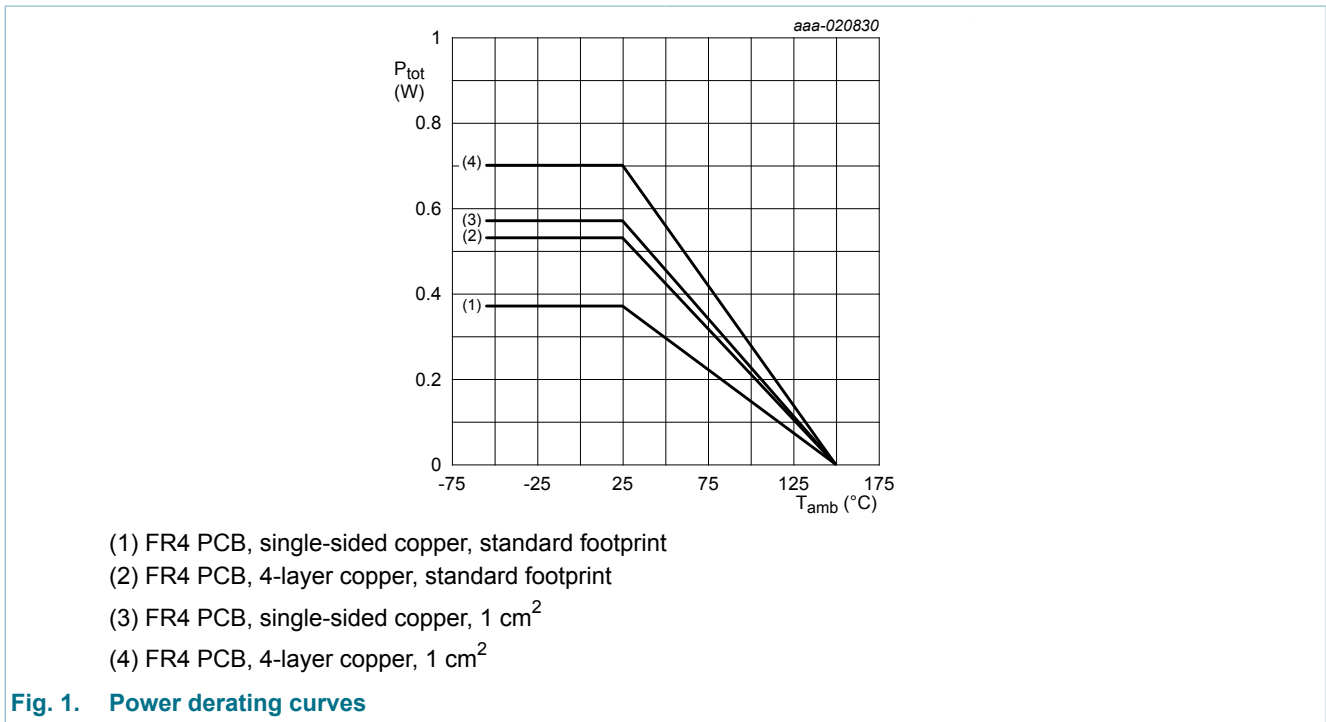
## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
<b>Per transistor</b>						
V <sub>CB0</sub>	collector-base voltage	open emitter		-	20	V
V <sub>CEO</sub>	collector-emitter voltage	open base		-	20	V
V <sub>EBO</sub>	emitter-base voltage	open collector		-	7	V
I <sub>C</sub>	collector current			-	2	A
I <sub>CM</sub>	peak collector current	single pulse; t <sub>p</sub> ≤ 1 ms		-	3	A
I <sub>B</sub>	base current			-	0.3	A
I <sub>BM</sub>	peak base current	single pulse; t <sub>p</sub> ≤ 1 ms		-	1	A
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C	[1]	-	370	mW
			[2]	-	570	mW
			[3]	-	530	mW
			[4]	-	700	mW
<b>Per device</b>						
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C	[1]	-	510	mW
			[2]	-	780	mW
			[3]	-	730	mW
			[4]	-	960	mW
T <sub>j</sub>	junction temperature			-	150	°C
T <sub>amb</sub>	ambient temperature			-55	150	°C
T <sub>stg</sub>	storage temperature			-65	150	°C

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 Printed-Circuit Board (PCB), single sided copper, tin-plated; mounting pad for collector 1 cm<sup>2</sup>.
- [3] Device mounted on an FR4 Printed-Circuit Board (PCB), 4-layer copper, tin-plated and standard footprint.
- [4] Device mounted on an FR4 Printed-Circuit Board (PCB), 4-layer copper, tin-plated; mounting pad for collector 1 cm<sup>2</sup>.

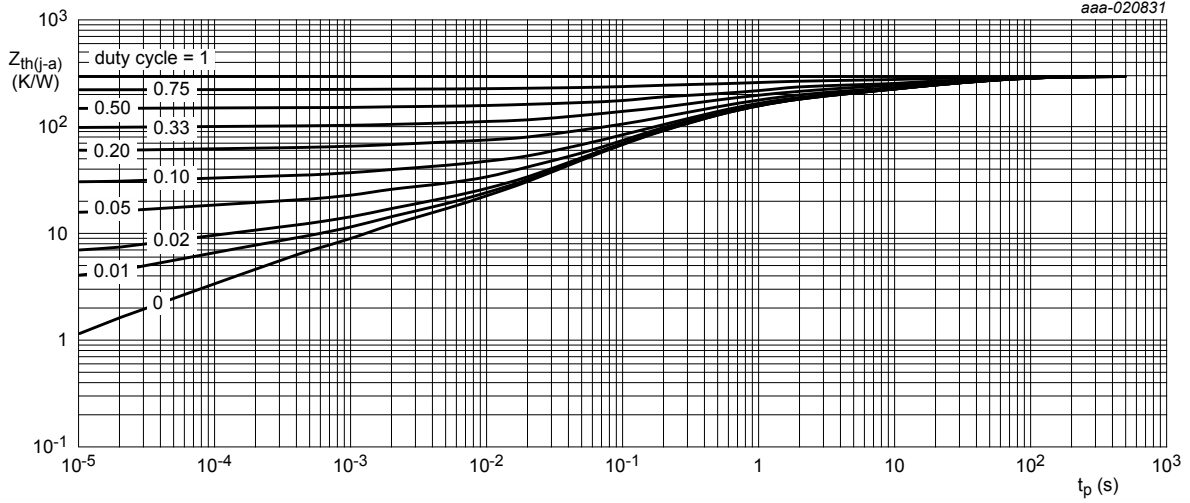


## 9. Thermal characteristics

Table 6. Thermal characteristics

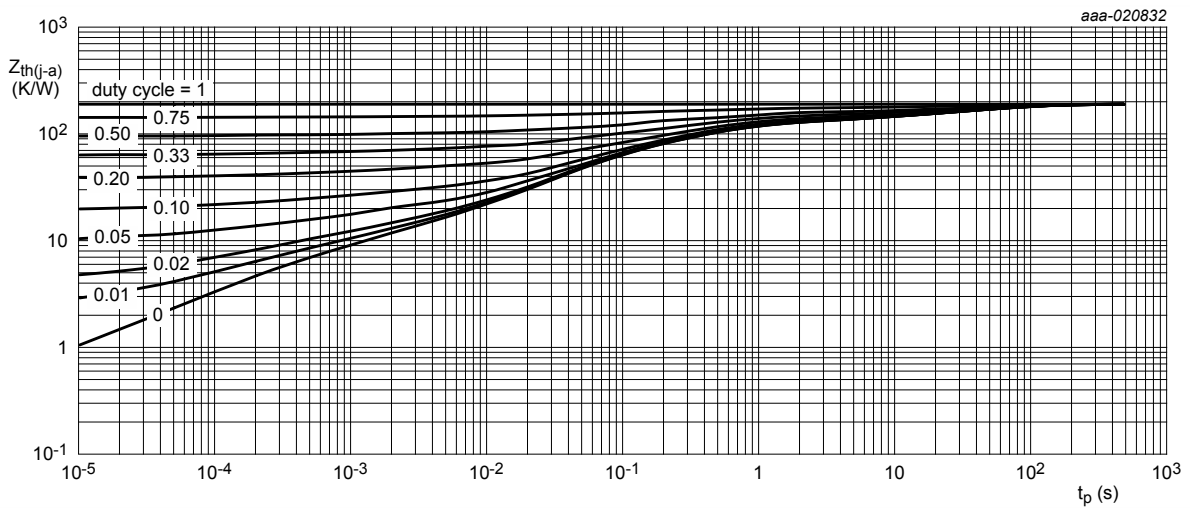
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
<b>Per transistor</b>							
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air	[1]	-	-	338	K/W
			[2]	-	-	219	K/W
			[3]	-	-	236	K/W
			[4]	-	-	179	K/W
<b>Per device</b>							
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air	[1]	-	-	246	K/W
			[2]	-	-	161	K/W
			[3]	-	-	172	K/W
			[4]	-	-	131	K/W

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.
- [3] Device mounted on an FR4 Printed-Circuit Board (PCB), 4-layer copper, tin-plated and standard footprint.
- [4] Device mounted on an FR4 Printed-Circuit Board (PCB), 4-layer copper, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.



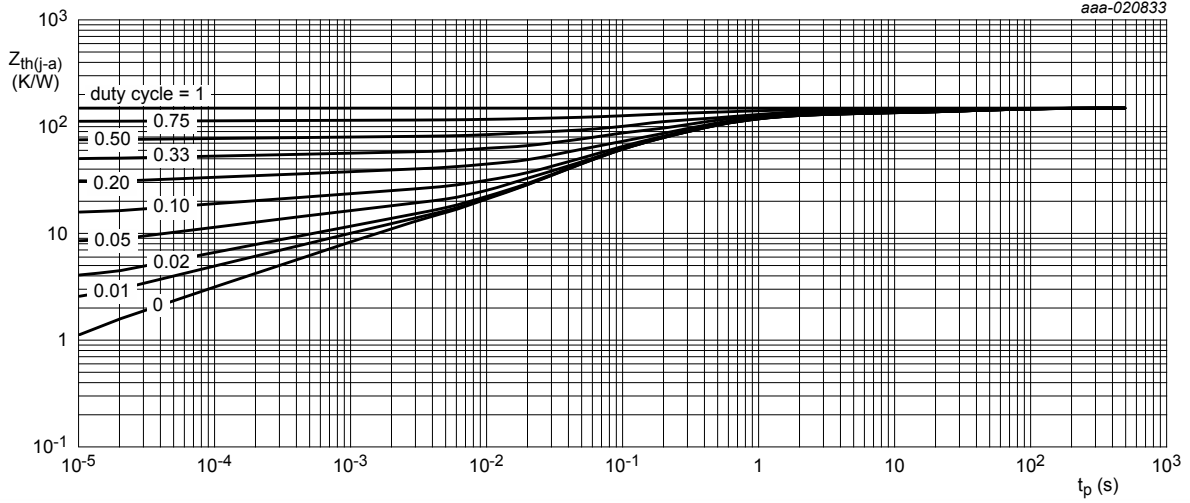
FR4 PCB, standard footprint

Fig. 2. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



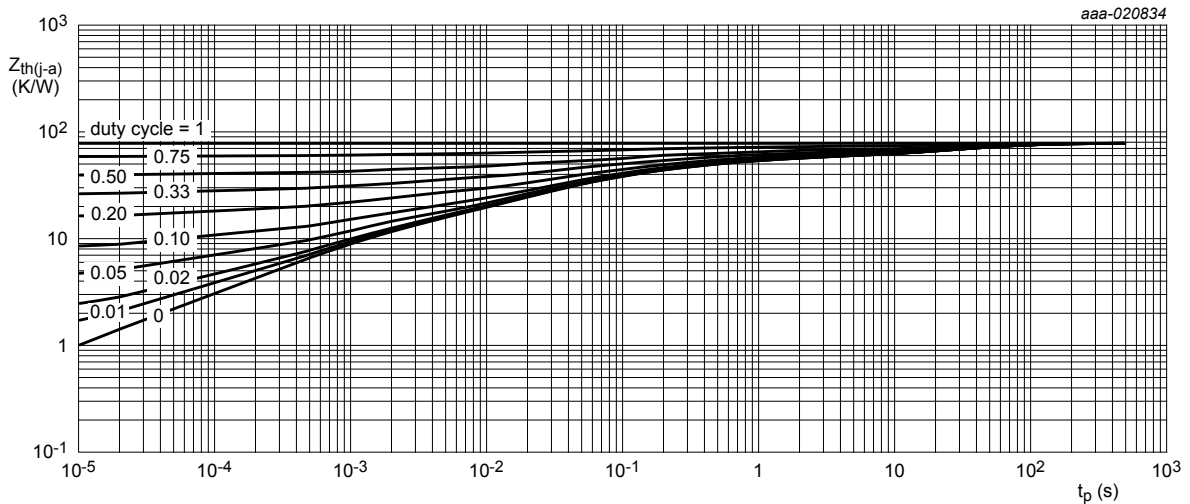
FR4 PCB, mounting pad for collector  $1\text{ cm}^2$

Fig. 3. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, 4-layer copper, standard footprint

**Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values**



FR4 PCB, 4-layer copper, mounting pad for collector 1 cm<sup>2</sup>

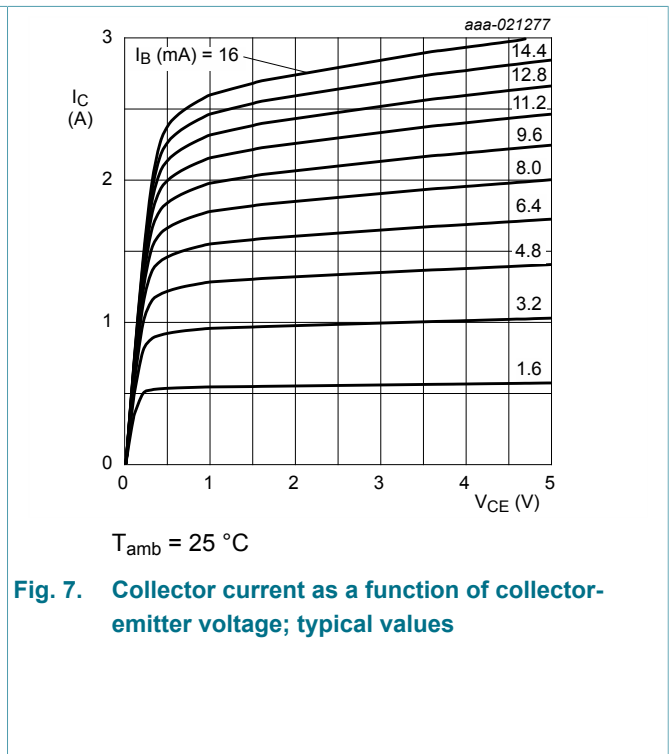
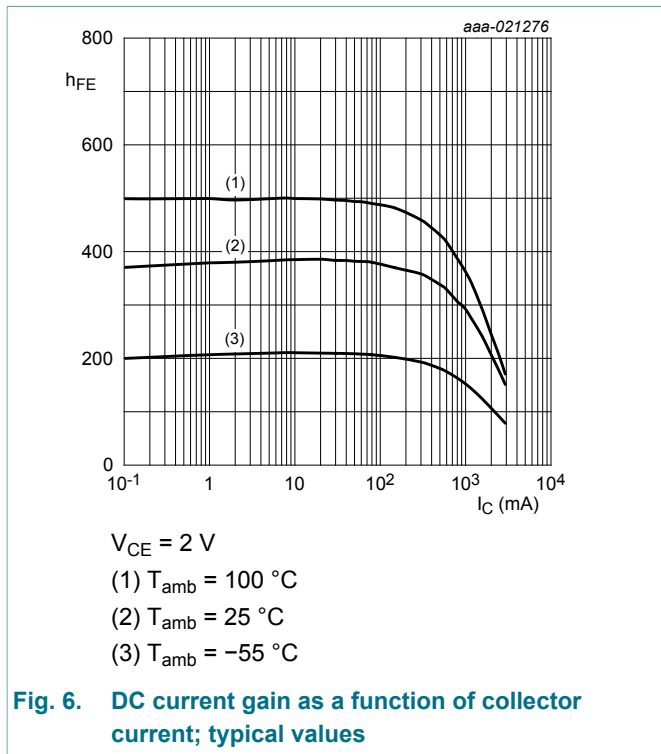
**Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values**

## 10. Characteristics

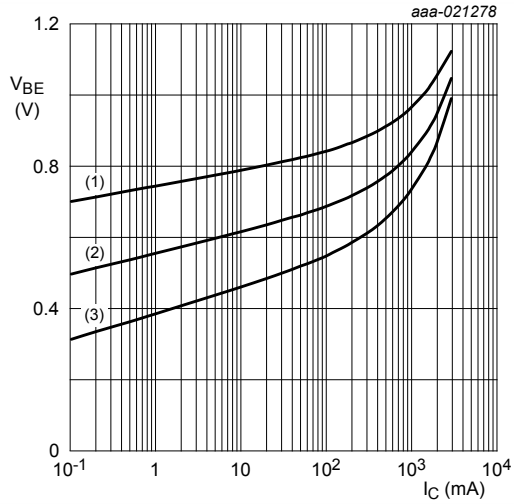
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per transistor</b>						
I <sub>CBO</sub>	collector-base cut-off current	V <sub>CB</sub> = 16 V; I <sub>E</sub> = 0 A; T <sub>amb</sub> = 25 °C	-	-	100	nA
		V <sub>CB</sub> = 16 V; I <sub>E</sub> = 0 A; T <sub>j</sub> = 150 °C	-	-	50	μA
I <sub>CES</sub>	collector-emitter cut-off current	V <sub>CE</sub> = 16 V; V <sub>BE</sub> = 0 V; T <sub>amb</sub> = 25 °C	-	-	100	nA
I <sub>EBO</sub>	emitter-base cut-off current	V <sub>EB</sub> = 5 V; I <sub>C</sub> = 0 A; T <sub>amb</sub> = 25 °C	-	-	100	nA
h <sub>FE</sub>	DC current gain	V <sub>CE</sub> = 2 V; I <sub>C</sub> = 100 mA; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02; T <sub>amb</sub> = 25 °C	250	450	-	
		V <sub>CE</sub> = 2 V; I <sub>C</sub> = 500 mA; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02; T <sub>amb</sub> = 25 °C	230	400	-	
		V <sub>CE</sub> = 2 V; I <sub>C</sub> = 1 A; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02; T <sub>amb</sub> = 25 °C	200	350	-	
		V <sub>CE</sub> = 2 V; I <sub>C</sub> = 2 A; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02	150	260	-	
V <sub>CEsat</sub>	collector-emitter saturation voltage	I <sub>C</sub> = 0.5 A; I <sub>B</sub> = 50 mA; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02 ; T <sub>amb</sub> = 25 °C	-	60	90	mV
		I <sub>C</sub> = 1 A; I <sub>B</sub> = 50 mA; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02 ; T <sub>amb</sub> = 25 °C	-	125	170	mV
		I <sub>C</sub> = 2 A; I <sub>B</sub> = 200 mA; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02 ; T <sub>amb</sub> = 25 °C	-	240	320	mV
R <sub>CEsat</sub>	collector-emitter saturation resistance	I <sub>C</sub> = 1 A; I <sub>B</sub> = 50 mA; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02 ; T <sub>amb</sub> = 25 °C	-	-	170	mΩ
V <sub>BEsat</sub>	base-emitter saturation voltage	I <sub>C</sub> = 0.5 A; I <sub>B</sub> = 50 mA; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02 ; T <sub>amb</sub> = 25 °C	-	0.92	1	V
		I <sub>C</sub> = 1 A; I <sub>B</sub> = 50 mA; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02; T <sub>amb</sub> = 25 °C	-	0.96	1.1	V
		I <sub>C</sub> = 2 A; I <sub>B</sub> = 200 mA; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02; T <sub>amb</sub> = 25 °C	-	1.18	1.3	V
V <sub>BE</sub>	base-emitter voltage	I <sub>C</sub> = 0.5 A; V <sub>CE</sub> = 2 V; pulsed; t <sub>p</sub> ≤ 300 μs; δ <sub>factor</sub> ≤ 0.02; T <sub>amb</sub> = 25 °C	-	0.77	0.9	V
t <sub>d</sub>	delay time	I <sub>C</sub> = 1 A; I <sub>Bon</sub> = 50 mA; I <sub>Boff</sub> = -50 mA; T <sub>amb</sub> = 25 °C	-	10	-	ns
t <sub>r</sub>	rise time		-	50	-	ns
t <sub>on</sub>	turn-on time		-	60	-	ns
t <sub>s</sub>	storage time		-	310	-	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_f$	fall time		-	60	-	ns
$t_{off}$	turn-off time		-	370	-	ns
$f_T$	transition frequency	$V_{CE} = 10\text{ V}; I_C = 500\text{ mA}; f = 100\text{ MHz}; T_{amb} = 25\text{ }^\circ\text{C}$	-	120	-	MHz
$C_c$	collector capacitance	$V_{CB} = 10\text{ V}; I_E = 0\text{ A}; i_e = 0\text{ A}; f = 1\text{ MHz}; T_{amb} = 25\text{ }^\circ\text{C}$	-	13.5	-	pF

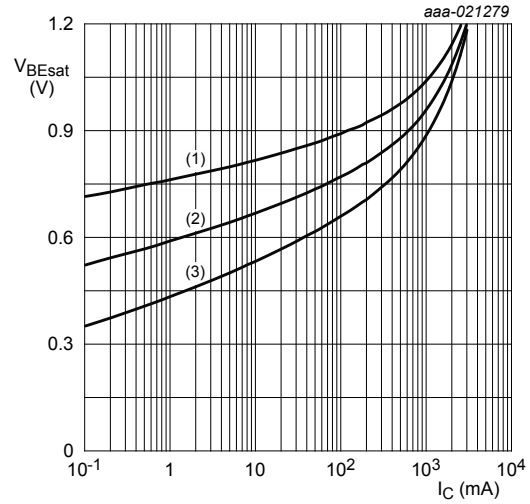






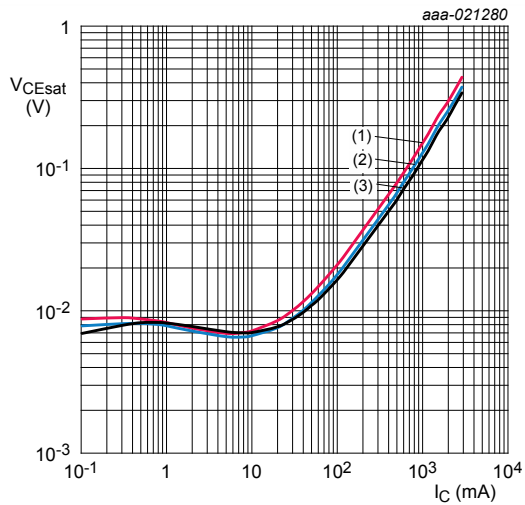
$V_{CE} = 2\text{ V}$   
 (1)  $T_{amb} = -55^\circ\text{C}$   
 (2)  $T_{amb} = 25^\circ\text{C}$   
 (3)  $T_{amb} = 100^\circ\text{C}$

**Fig. 8. Base-emitter voltage as a function of collector current; typical values**



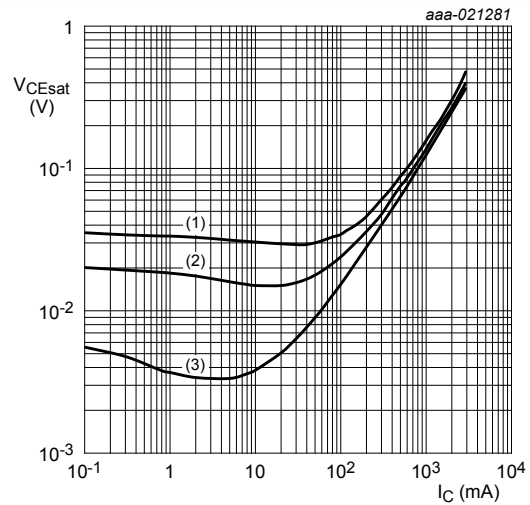
$I_C/I_B = 20$   
 (1)  $T_{amb} = -55^\circ\text{C}$   
 (2)  $T_{amb} = 25^\circ\text{C}$   
 (3)  $T_{amb} = 100^\circ\text{C}$

**Fig. 9. Base-emitter saturation voltage as a function of collector current; typical values**



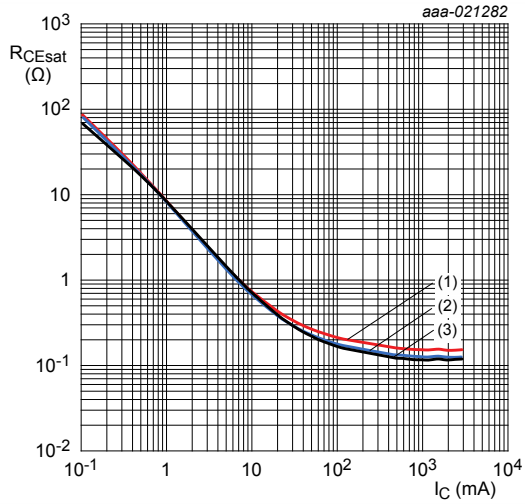
$V_{CE} = 2\text{ V}$   
 (1)  $T_{amb} = 100^\circ\text{C}$   
 (2)  $T_{amb} = 25^\circ\text{C}$   
 (3)  $T_{amb} = -55^\circ\text{C}$

**Fig. 10. Collector-emitter saturation voltage as a function of collector current; typical values**



$T_{amb} = 25^\circ\text{C}$   
 (1)  $I_C/I_B = 100$   
 (2)  $I_C/I_B = 50$   
 (3)  $I_C/I_B = 10$

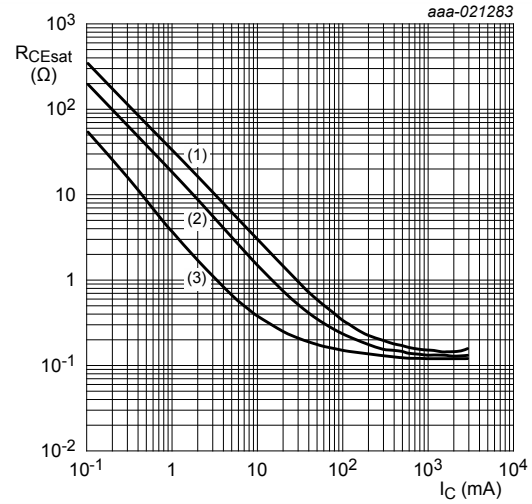
**Fig. 11. Collector-emitter saturation voltage as a function of collector current; typical values**



$I_C/I_B = 20$

- (1)  $T_{amb} = 100\text{ °C}$
- (2)  $T_{amb} = 25\text{ °C}$
- (3)  $T_{amb} = -55\text{ °C}$

Fig. 12. Collector-emitter saturation resistance as a function of collector current; typical values



$T_{amb} = 25\text{ °C}$

- (1)  $I_C/I_B = 100$
- (2)  $I_C/I_B = 50$
- (3)  $I_C/I_B = 10$

Fig. 13. Collector-emitter saturation resistance as a function of collector current; typical values

### 11. Test information

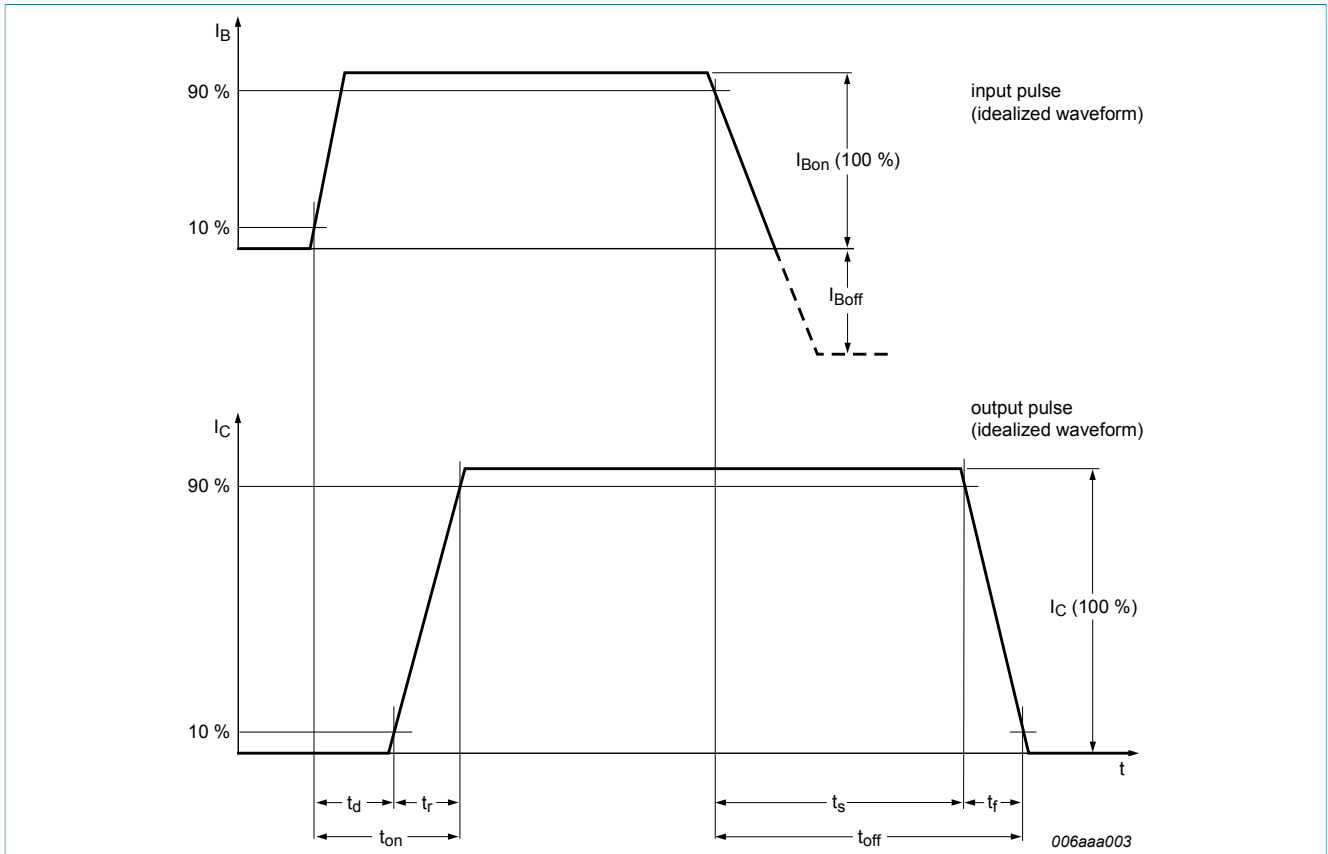


Fig. 14. BISS transistor switching time definition

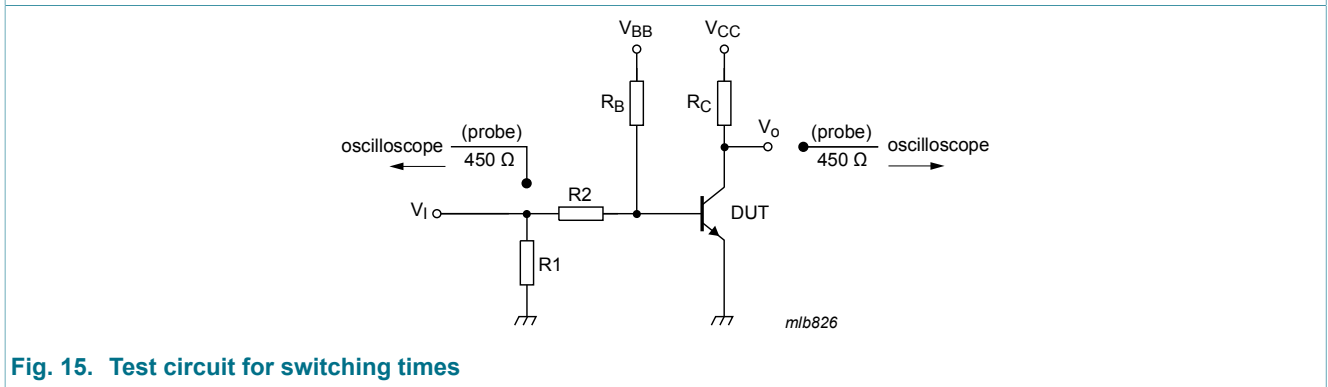


Fig. 15. Test circuit for switching times

#### 11.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

## 12. Package outline

DFN2020D-6: plastic, thermally enhanced ultra thin and small outline package; no leads; 6 terminals; body 2 x 2 x 0.65 mm

SOT1118D

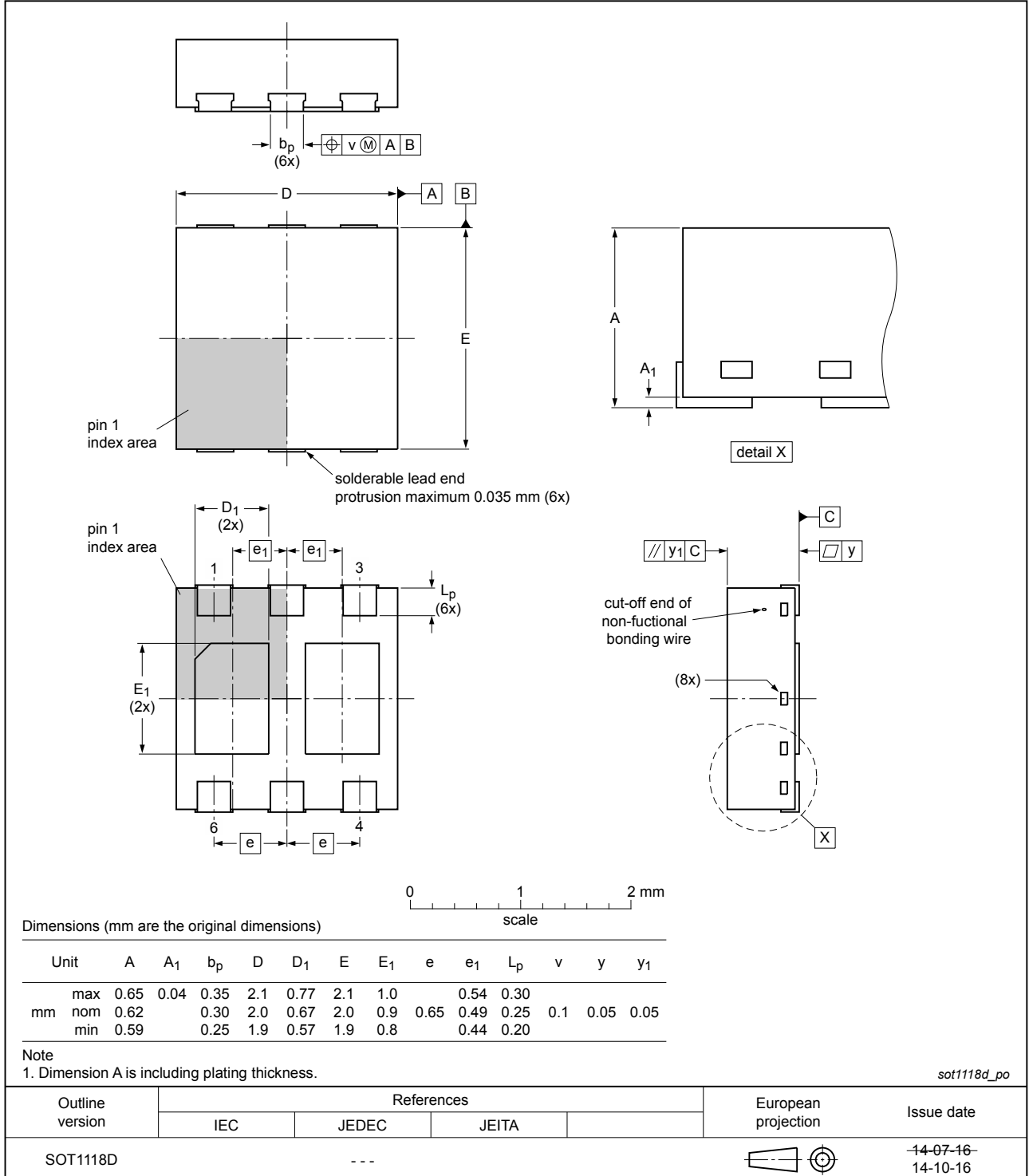
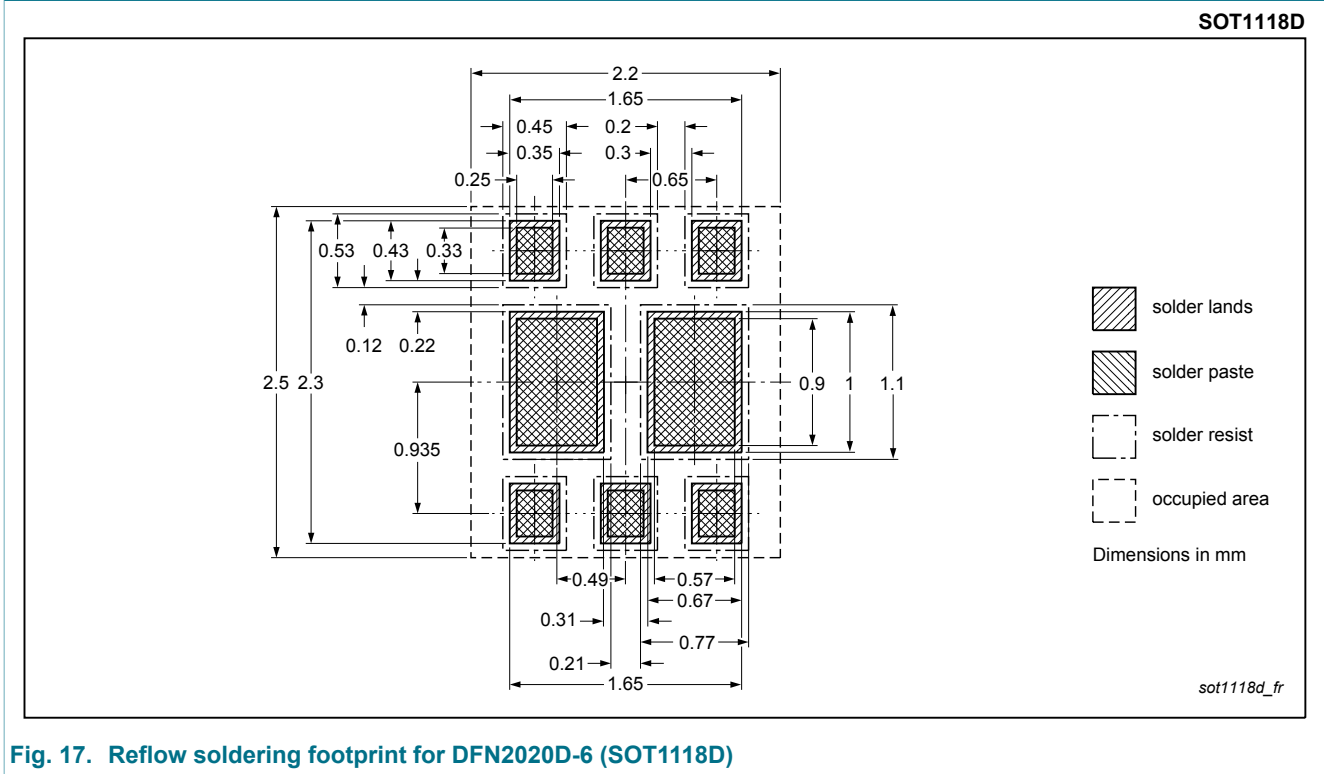


Fig. 16. Package outline DFN2020D-6 (SOT1118D)

### 13. Soldering



**Fig. 17. Reflow soldering footprint for DFN2020D-6 (SOT1118D)**

## 14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PBSS4220PANS v.1	20151214	Product data sheet	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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