To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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DATA SHEET

RENESAS

MOS INTEGRATED CIRCUIT

μPD8827B

7500 PIXELS × 3 COLOR CCD LINEAR IMAGE SENSOR

DESCRIPTION

The μPD8827B is a high-speed and high sensitive color CCD (Charge Coupled Device) linear image sensor which changes optical images to electrical signal and has the function of color separation. The μPD8827B has the high speed voltage amplifiers and the high speed registers. In addition, the positioning error, which occurs when some manuscripts are fed, is small since the RGB pixel line space is also small (2 lines). So, it is possible that the image of the high density is read at high speed. Therefore, it is suitable for 600 dpi/A3 high-speed color digital copiers, color scanners and so on, by the use of the plastic package with heat sink that has high heat radiation.

FEATURES

- Valid photocell : 7500 pixels × RGB 3 lines
- Photocell's size : 9.325 μm
- Line spacing : 18.65 μm (2 lines) Red line - Green line, Green line - Blue line
- Color filter : Primary colors (red, green and blue), Pigment filter
  Light resistance 10^7 lx•hour with standard sunlight and ultraviolet cut filter (L40)
- On-chip micro lens : Stripe type lens on RGB pixel rows
- Resolution : 24 dot/mm A3 (297 × 420 mm) size (shorter side)
- Data rate : 70 MHz Max. (35 MHz/ch max.)
- Output type : 2 outputs in phase
- Power supply : +10 V
- Drive clock level : CMOS output under 5 V operation
- On-chip circuits : Reset feed-through level clamp circuits
  Voltage amplifiers

ORDERING INFORMATION

Part Number	Package
μPD8827BCZ-A	CCD linear image sensor 40-pin plastic DIP with heat sink (15.24 mm (600))

Remark "-A" indicates Pb-free (This product does not contain Pb in external electrode and other parts).

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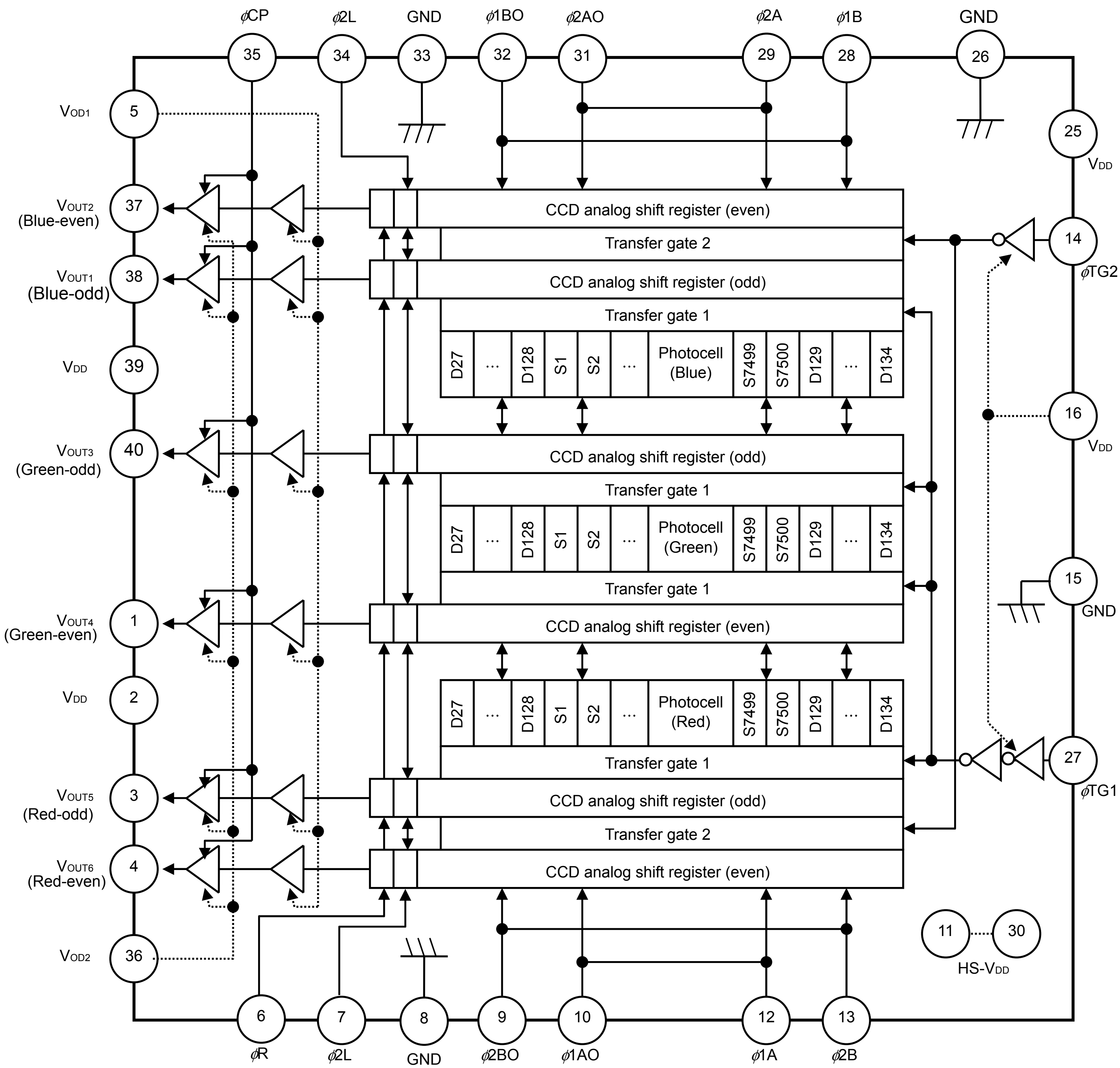
Date Published March 2010 NS
Printed in Japan

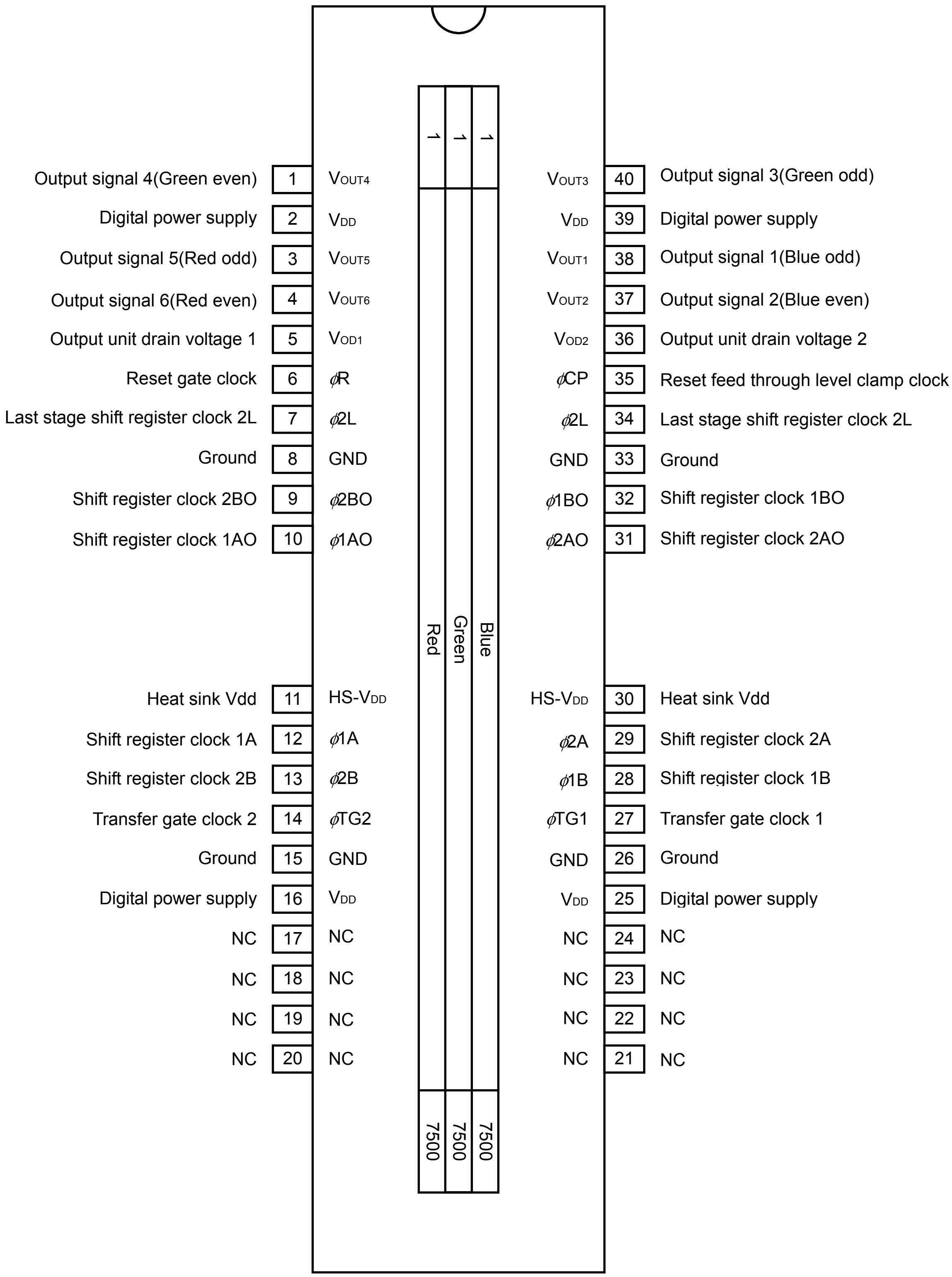
The mark <R> shows major revised points.
The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

BLOCK DIAGRAM

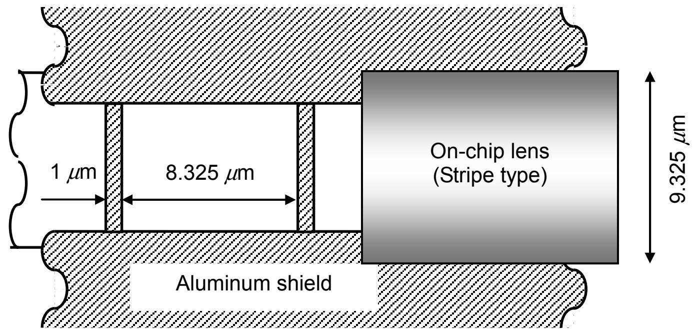


PIN CONFIGURATION (Top View)

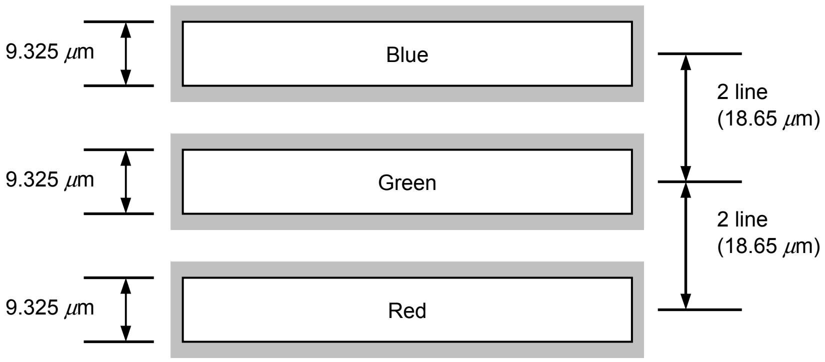
CCD linear image sensor 40-pin plastic DIP with heat sink (15.24 mm (600))



PHOTOCELL STRUCTURE DIAGRAM



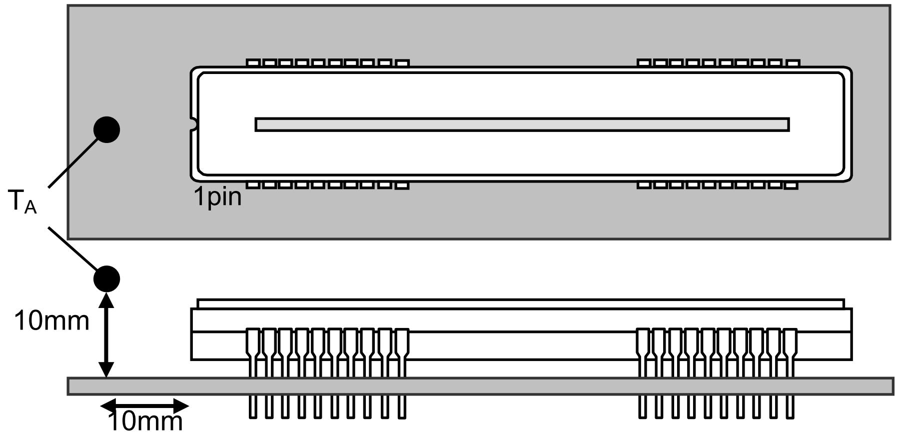
LINE SPACE



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Output drain voltage	V_{OD1}, V_{OD2}	–0.3 to +12.0	V
Digital power supply	V_{DD}	–0.3 to +12.0	V
Heat sink V_{DD}	HS-V_{DD}	–0.3 to +12.0	V
Shift register clock voltage	$V_{\phi 1}$, $V_{\phi 2}$,$V_{\phi 10}$, $V_{\phi 20}$	–0.3 to +8.0	V
Last stage shift register clock voltage	$V_{\phi 2L}$	–0.3 to +8.0	V
Reset gate clock voltage	$V_{\phi R}$	–0.3 to +8.0	V
Reset feed-through level clamp clock voltage	$V_{\phi CP}$	–0.3 to +8.0	V
Transfer gate clock voltage	$V_{\phi TG1}$, $V_{\phi TG2}$	–0.3 to +8.0	V
Operating ambient temperature Note	T_A	0 to +60	˚C
Storage temperature	T_{stg}	–40 to +100	˚C

Note The operating ambient temperature T_A is defined as an atmosphere temperature in a point 10 mm away on the circuit board, and 10 mm away from the short side of package (pin 1 side). Refer to below figure. Use it at the condition without dewy condensation.



Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Output drain voltage	V_{OD1}, V_{OD2}	9.7	10.0	10.3	V
Digital power supply	V_{DD}	9.7	10.0	10.3	V
Heat sink V_{DD}	HS-V_{DD}	9.7	10.0	10.3	V
Shift register clock high level	$V\phi_{1H}$, $V\phi_{2H}$, $V\phi_{10H}$, $V\phi_{20H}$	4.75	5.0	6.0	V
Shift register clock low level	$V\phi_{1L}$, $V\phi_{2L}$, $V\phi_{10L}$, $V\phi_{20L}$	-0.3	0.0	0.5	V
Last stage shift register clock high level	$V\phi_{2LH}$	4.75	5.0	6.0	V
Last stage shift register clock low level	$V\phi_{2LL}$	-0.3	0.0	0.5	V
Reset gate clock high level	$V\phi_{RH}$	4.75	5.0	5.5	V
Reset gate clock low level	$V\phi_{RL}$	-0.3	0.0	0.5	V
Reset feed-through level clamp clock high level	$V\phi_{CPH}$	4.75	5.0	6.0	V
Reset feed-through level clamp clock low level	$V\phi_{CPL}$	-0.3	0.0	0.5	V
Transfer gate clock high level	$V\phi_{TG1H}$, $V\phi_{TG2H}$	4.75	5.0	6.0	V
Transfer gate clock low level	$V\phi_{TG1L}$, $V\phi_{TG2L}$	-0.3	0.0	0.5	V
Shift register clock amplitude	$V\phi_{1p-p}$,$V\phi_{2p-p}$,$V\phi_{10p-p}$,$V\phi_{20p-p}$	4.75	5.0	6.5	V
Last stage shift register clock amplitude	$V\phi_{2Lp-p}$	4.75	5.0	6.5	V
Reset gate clock amplitude	$V\phi_{Rp-p}$	4.75	5.0	6.0	V
Reset feed-through level clamp clock amplitude	$V\phi_{CPp-p}$	4.75	5.0	6.5	V
Transfer gate clock amplitude	$V\phi_{TG1p-p}$, $V\phi_{TG2p-p}$	4.75	5.0	6.5	V
Data rate	$2xf\phi_R$	0.2	2.0	70	MHz

<R>

ELECTRICAL CHARACTERISTICS

T_A = +25°C, V_{OD1} = V_{OD2} = V_{DD} = +10 V, $f_{\phi R}$ = 1 MHz, Data rate = 2 MHz, Storage time = 10 ms, Input clock = 5 Vp-p

Light source (except Response2): 3200 K halogen lamp + C-500S (Infrared cut filter, t = 1 mm) + HA-50 (Heat absorbing filter, t = 3 mm)

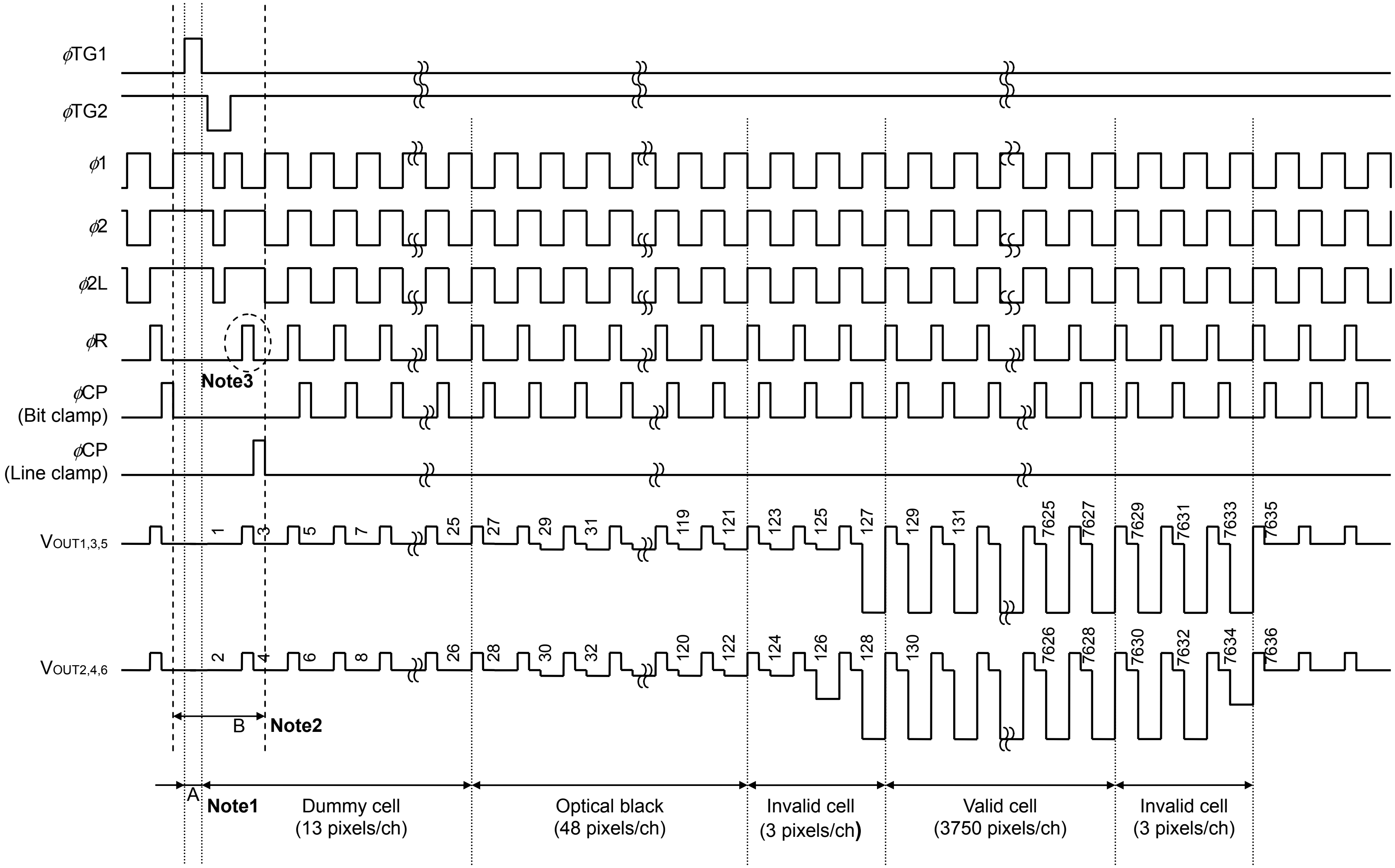
Parameter		Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Saturation voltage		V_{sat}		1.5	2.0	–	V
Saturation exposure	Red	SE(R)		–	0.05	–	lx•s
	Green	SE(G)		–	0.04	–	lx•s
	Blue	SE(B)		–	0.08	–	lx•s
Photo response non-uniformity		PRNU	V_{OUT} = 1.0 V	–	6	18	%
Average dark signal		ADS	Light shielding	–	1.0	5.0	mV
Dark signal non-uniformity		DSNU	Light shielding	–	2.0	12.0	mV
Total power consumption		P_W		–	900	1170	mW
	Power consumption (V_{OD1})	P_{OD1}		–	250	325	mW
	Power consumption (V_{OD2})	P_{OD2}		–	580	755	mW
	Power consumption (V_{DD})	P_{DD}		–	70	90	mW
Output impedance		Z_O		–	0.2	0.4	kΩ
Response1	Red	R_R	3200 k + C500S + HA50	26.25	37.5	48.75	V/lx•s
	Green	R_G		32.97	47.1	61.23	V/lx•s
	Blue	R_B		17.64	25.2	32.76	V/lx•s
Response2 (Corresponding value from Response1)	Red	R_R	A light source + CM500S	–	(34.5)	–	V/lx•s
	Green	R_G		–	(45.7)	–	V/lx•s
	Blue	R_B		–	(22.0)	–	V/lx•s
Response peak	Red			–	610	–	nm
	Green			–	535	–	nm
	Blue			–	460	–	nm
Image lag		IL	V_{OUT} = 0.5 V	–	1	30	mV
Offset level		V_{OS}		4.0	5.0	6.0	V
Output fall delay time		t_d		–	6	–	ns
Register imbalance		RI	V_{OUT} = 1.0 V	–	1.0	7.0	%
Total transfer efficiency		TTE	V_{OUT} = 1 V, $f_{\phi 1,2}$ = 35 MHz $V_{p\text{-}p\phi 1,2}$ = 4.75 V	92	98	–	%
Dynamic range		DR1	V_{sat} / DSNU	–	1000	–	times
		DR2	V_{sat} / σdark	–	800	–	times
Reset feed-through noise		RFTN	Light shielding	–1.5	–0.2	+0.5	V
Light shielding random noise		σdark	Light shielding, Bit clamp	–	2.5	–	mV
Shot noise		σshot	V_{OUT} = 1.0 V	–	14.5	–	mV

INPUT PIN CAPACITANCE (V_{OD1} = V_{OD2} = V_{DD} = +10 V)

Parameter	Symbol	Pin name	Pin No.	MIN.	TYP.	MAX.	Unit
Shift register clock pin capacitance Note	$C_{\phi 1}$	φ1AO	10	140	160	180	pF
		φ1A	12	140	160	180	
		φ1B	28	140	160	180	
		φ1BO	32	140	160	180	
		TOTAL		560	640	720	
	$C_{\phi 2}$	φ2BO	9	140	160	180	pF
		φ2B	13	140	160	180	
		φ2A	29	140	160	180	
		φ2AO	31	140	160	180	
		TOTAL		560	640	720	
Last stage shift register clock pin capacitance	$C_{\phi 2L}$	φ2L	7	6	8	10	pF
			34	6	8	10	
Reset gate clock pin capacitance	$C_{\phi R}$	φR	6	11	13	15	pF
Reset feed-through level clamp clock pin capacitance	$C_{\phi CP}$	φCP	35	12	14	16	pF
Transfer gate clock pin capacitance	$C_{\phi TG1}$	φTG1	27	7	9	11	pF
	$C_{\phi TG2}$	φTG2	14	11	13	15	pF

Note $C_{\phi 1}$ and $C_{\phi 2}$ are equivalent capacitance with driving device, including the co-capacitance between φ1 and φ2. Pin 10, 12, 28 and 32 (φ1) are connected inside of the device. Pin 9, 13, 29 and 31(φ2) are also connected.

TIMING CHART 1

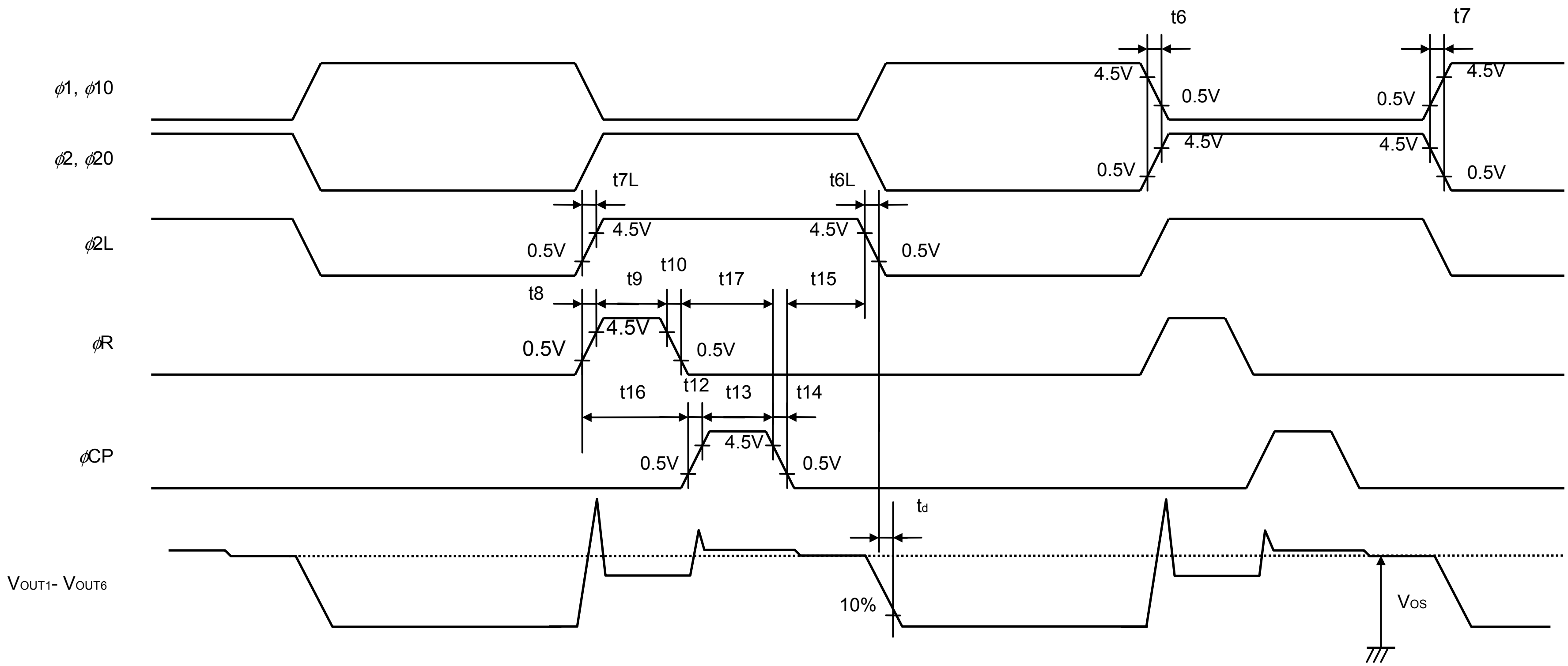


Note1: Set the φR and φCP to low level during this period A.

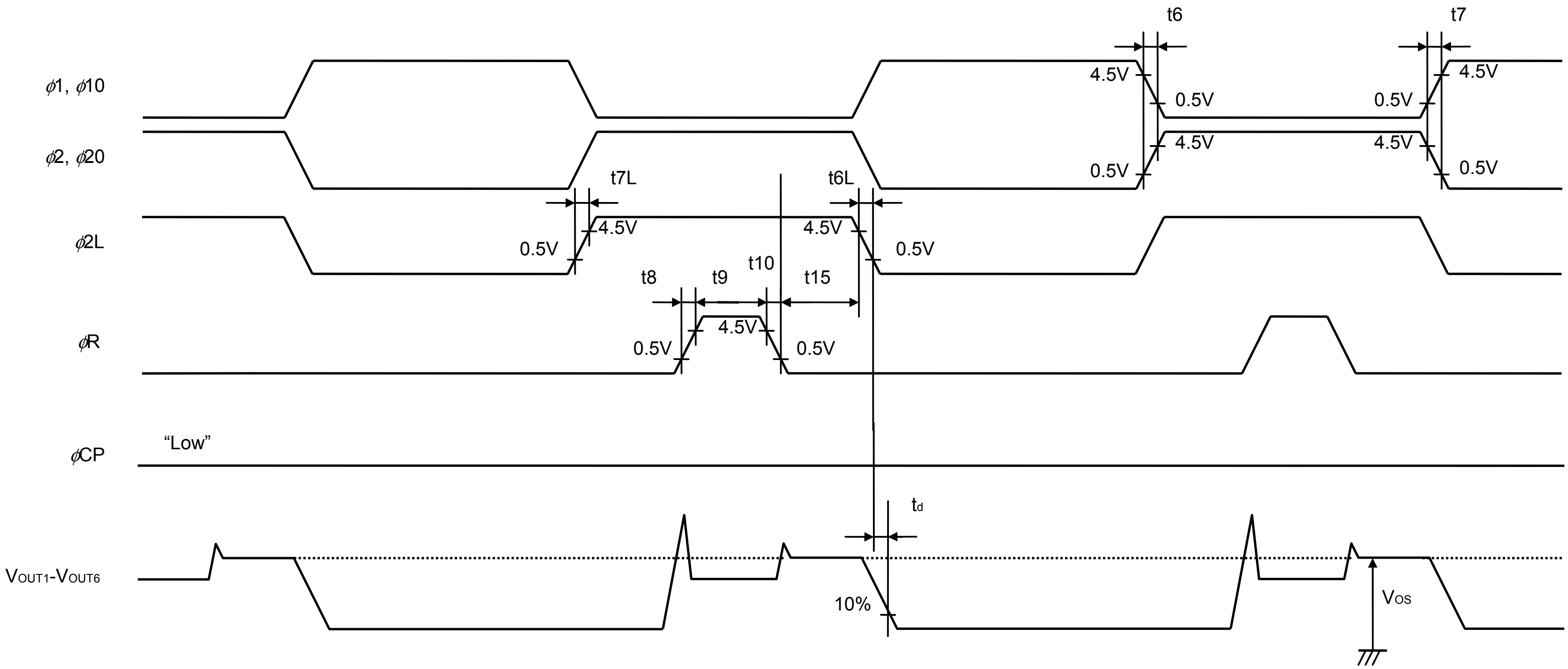
Note2 : Refer to TIMING CHART 4 during this period B.

Note3: In the case of Bit clamp mode, it is possible to omit this pulse inside the dotted line.

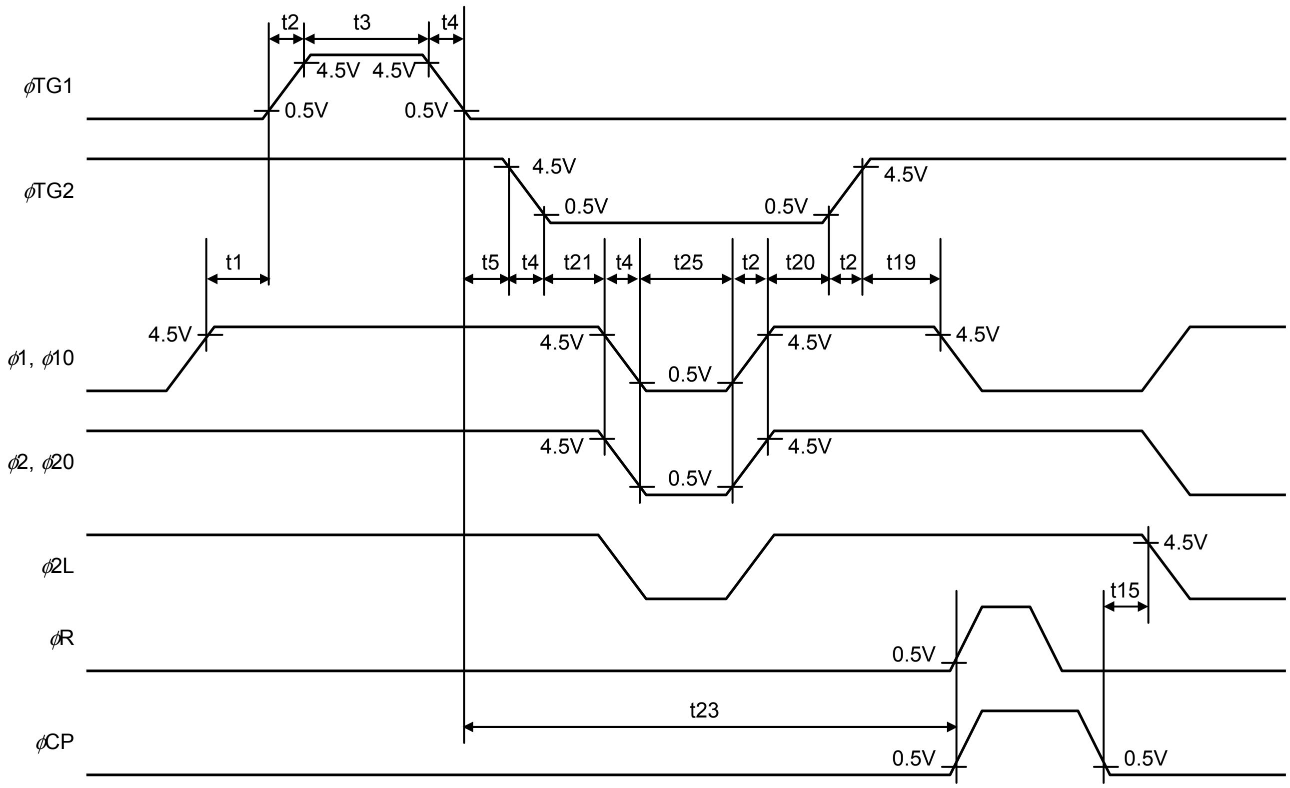
TIMING CHART 2 (Bit Clamp)



TIMING CHART 3 (Line Clamp)



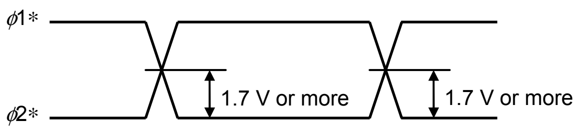
TIMING CHART4 (The period B of TIMING CHART 1)



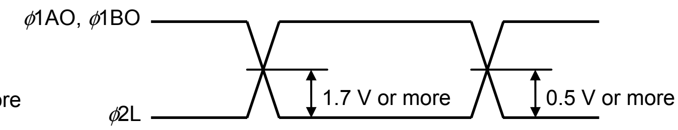
Symbol	MIN.	TYP.	MAX.	Unit
t1	100	200	2000	ns
t2, t4	0	10	-	ns
t3	1000	1100	5000	ns
t5	0	200	1000	ns
t6, t7	0	10	-	ns
t6L, t7L	0	3	-	ns
t8, t10	0	3	-	ns
t9	2	125	-	ns
t12, t14	0	3	-	ns
t13	8	125	-	ns
t15	0	250	-	ns
t16	0	125	-	ns
t17	2	125	-	ns
t19	300	400	2000	ns
t20	100	200	2000	ns
t21	300	400	2000	ns
t23	300	400	-	ns
t25	1500	1600	5000	ns

CROSS POINTS

(ϕ1∗, ϕ2∗) CROSS POINTS

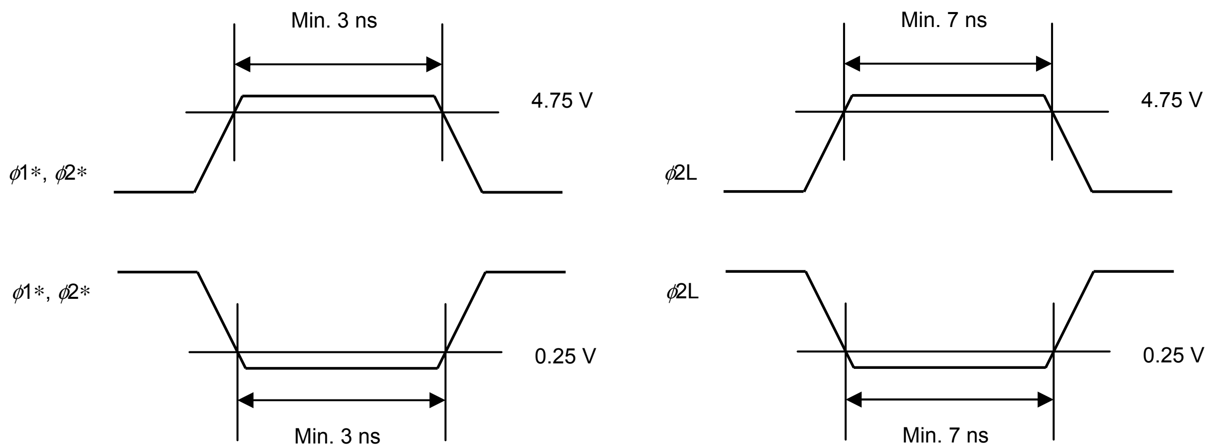


(ϕ1AO, ϕ2L) (ϕ1BO, ϕ2L) CROSS POINTS



Remark Adjust cross points of (ϕ1A, ϕ2A), (ϕ1B, ϕ2B), (ϕ1AO, ϕ2AO), (ϕ1BO, ϕ2BO), (ϕ1AO, ϕ2L) and (ϕ1BO,ϕ2L) with an input resistance of each pin.

CLOCK HIGH/LOW LEVEL WIDTH



DEFINITIONS OF CHARACTERISTICS

1. Saturation voltage: V_{sat}

The output signal voltage at which the response linearity is lost

2. Saturation exposure: SE

Product of intensity of illumination (lx) and storage time (s) when saturation of output voltage occurs

3. Photo response non-uniformity: PRNU

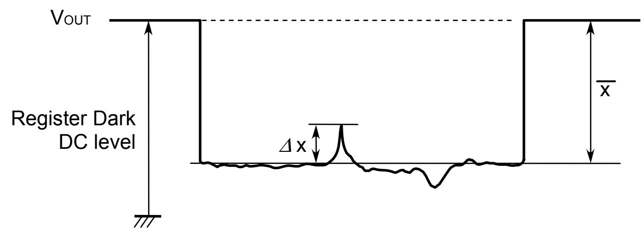
The output signal non-uniformity of all the valid pixels when the photosensitive surface is applied with the light of uniform illumination. This is calculated by the following formula, and it is defined by each six of them.

$$\text{PRNU (\%)} = \frac{\Delta x}{\overline{x}} \times 100$$

$$\overline{x} = \frac{\sum_{j=1}^{3750} x_j}{3750}$$

Δx : maximum of $| x_j - \overline{x} |$

x_j : Output voltage of valid pixel number j



4. Average dark signal: ADS

Average output signal voltage of all the valid pixels at light shielding. This is calculated by the following formula, and it is defined by each six of them.

$$\text{ADS (mV)} = \frac{\sum_{j=1}^{3750} d_j}{3750}$$

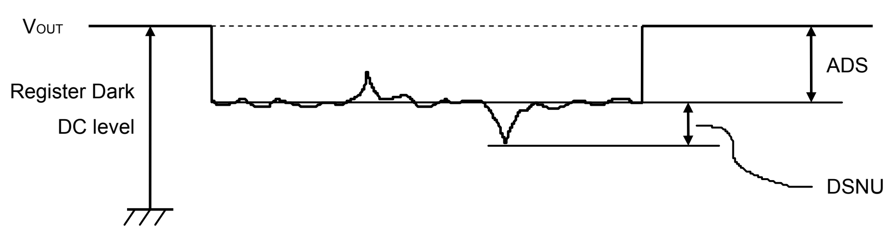
d_j : Dark signal of valid pixel number j

5. Dark signal non-uniformity: DSNU

Absolute maximum of the difference between ADS and voltage of the highest or lowest output pixel of all the valid pixels at light shielding. This is calculated by the following formula, and it is defined by each six of them.

DSNU (mV) : maximum of $| dj - \text{ADS} |_{j = 1 \text{ to } 3750}$

dj : Dark signal of valid pixel number j



6. Output impedance: Z_O

Impedance of the output pins viewed from outside

7. Response: R

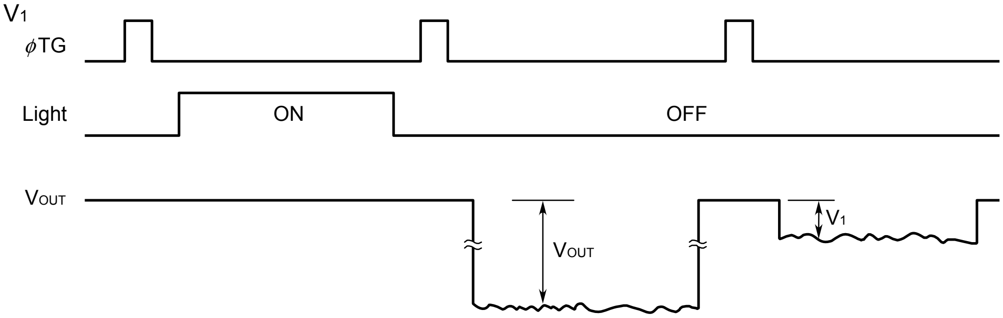
Output voltage divided by exposure (lx•s).

Note that the response varies with a light source (spectral characteristic).

8. Image lag: IL

IL is the average signal output just after light off.

IL (mV) = V_1



9. Register imbalance: RI

RI is the rate of the difference between the averages of the output voltage of Odd and Even pixels, against the average output voltage of all the valid pixels.

$$RI\ (\%) = \frac{\frac{2}{n}\left|\sum_{j=1}^{\frac{n}{2}} (V_{2j-1} - V_{2j})\right|}{\frac{1}{n}\sum_{j=1}^{n} V_j} \times 100$$

n : Number of valid pixels

V_j : Output voltage of each pixel

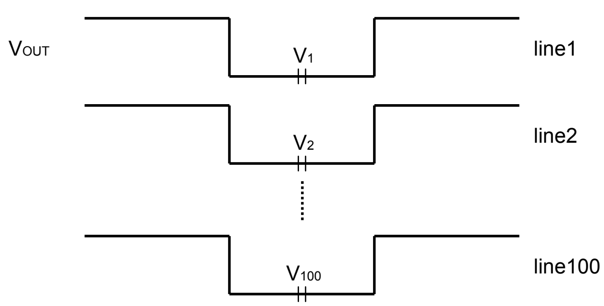
10. Random noise (light shielding): σdark

Shot noise: σshot

σdark and σshot are defined as the standard deviation of a valid pixel output signal with 100 times (100 lines) data sampling. These are measured by the DC level sampling of only the signal level, not by CDS (Correlated Double Sampling)

$$\sigma\ (mV) = \sqrt{\frac{\sum_{i=1}^{100} (V_i - \overline{V})^2}{100}} \quad , \quad \overline{V} = \frac{1}{100}\sum_{i=1}^{100} V_i$$

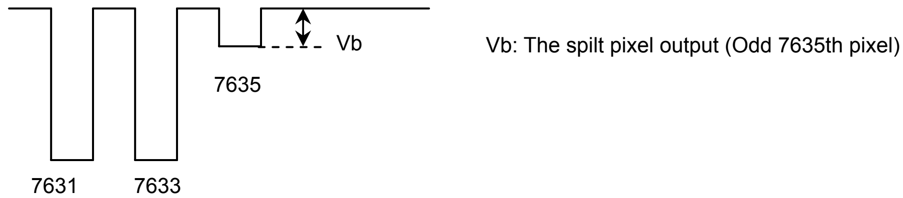
Vi : A valid pixel output signal among all of the valid pixels for each color.



11. Total transfer efficiency: TTE

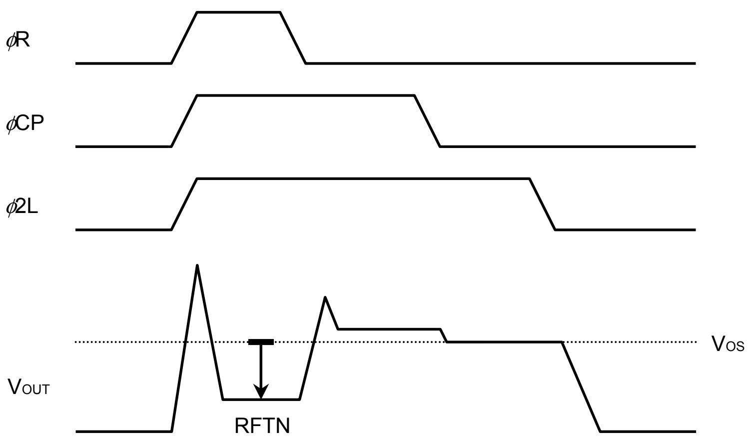
TTE is the total transfer rate of CCD analog shift register. The rate is calculated by the following formula, and it is defined by each odd output.

TTE (%) = (1 - Vb / Average output of all the valid pixels) × 100

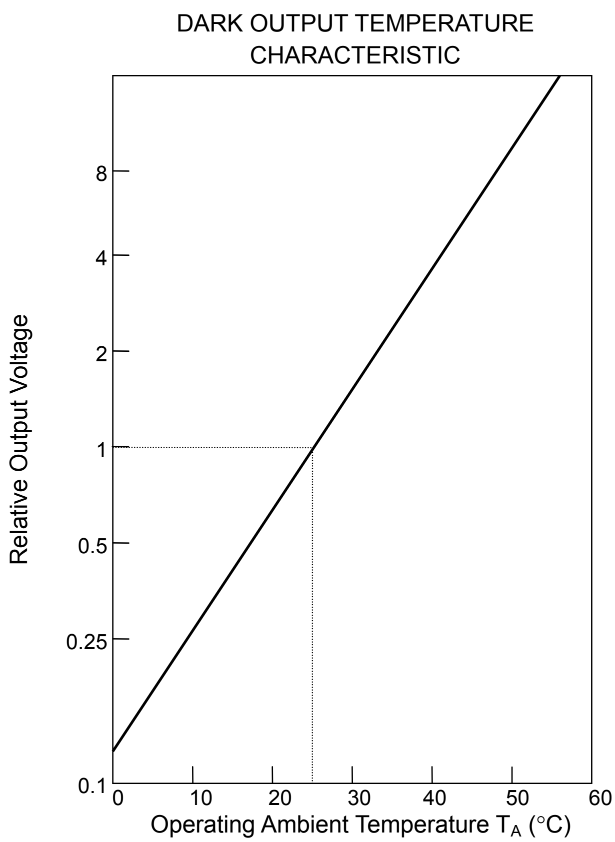


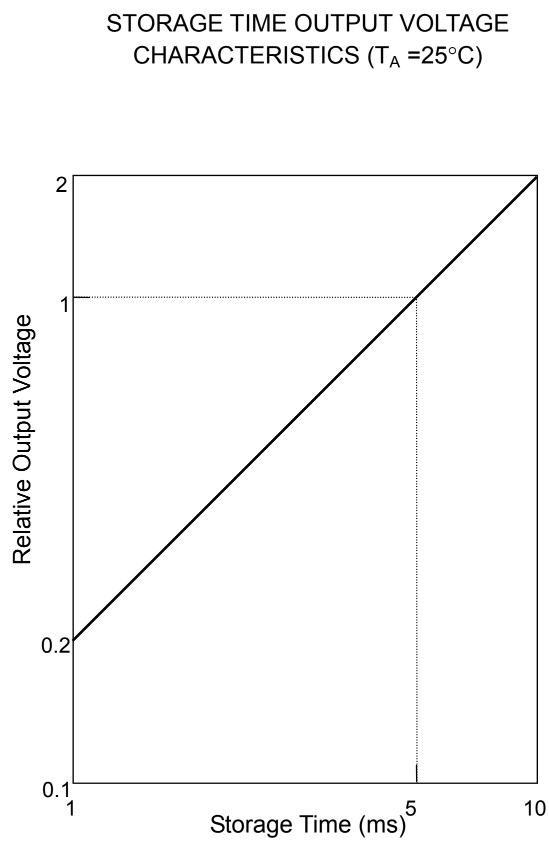
12. Reset feed-through noise: RFTN

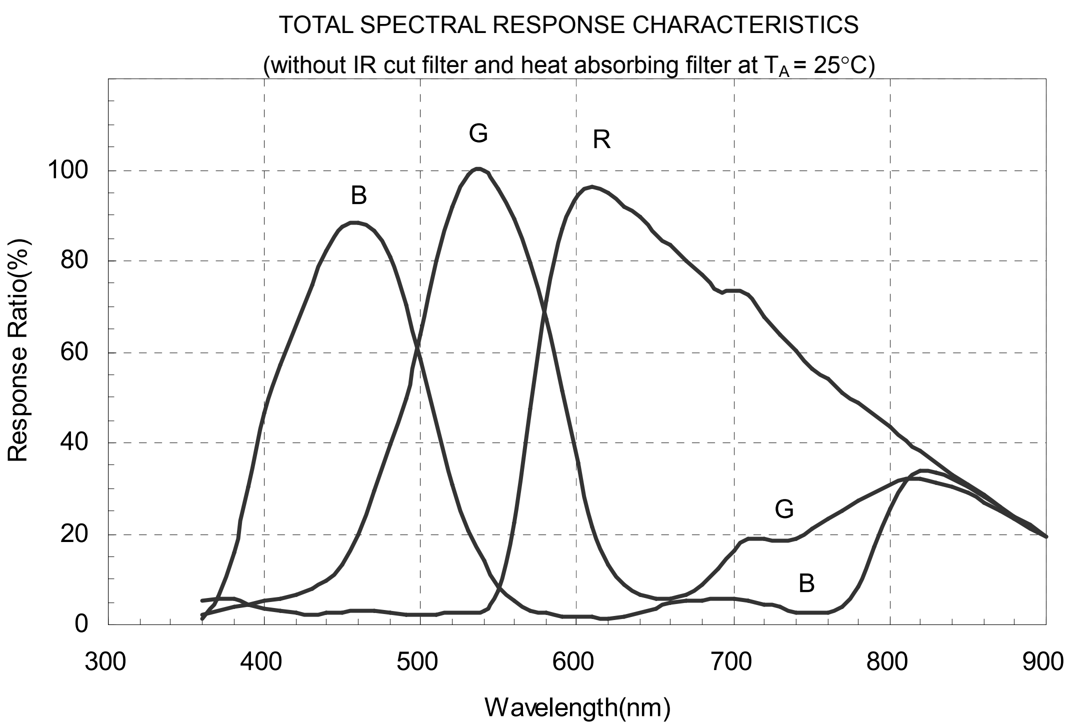
RFTN is switching noise of φR. RFTN is defined as follows.



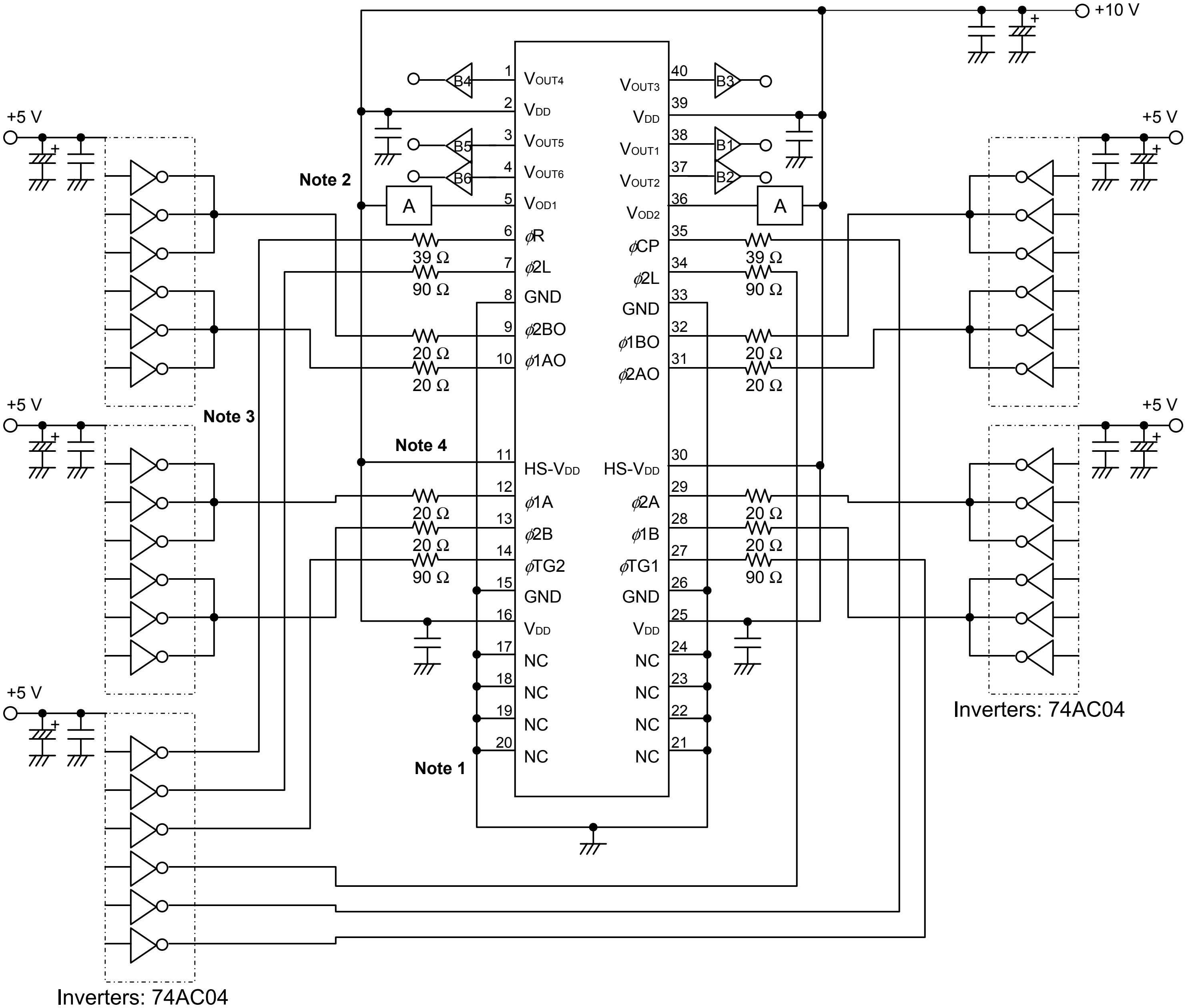
STANDARD CHARACTERISTIC CURVES (Nominal)







APPLICATION CIRCUIT EXAMPLE



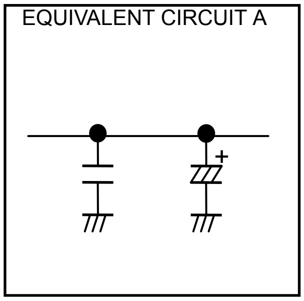
Notes 1. Connect the NC pins to GND.

2. Arrange a circuit A near each power supply terminals (V_{OD1}, V_{OD2}) to prevent the interference between V_{OD1} and V_{OD2}.

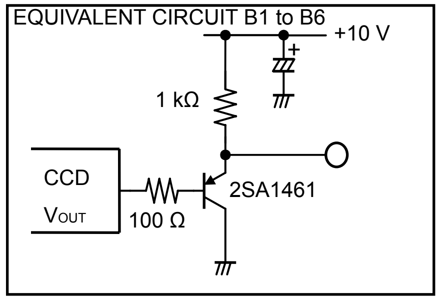
3. Connect 3 inverters for each terminal of φ1∗∗ and φ2∗∗.

4. HS-V_{DD} is connected only to the heat sink, it is not connected to V_{OD1} and V_{OD2}, and V_{DD} inside the device. Set HS-V_{DD} to V_{DD} in common on a board.

EQUIVALENT CIRCUIT A

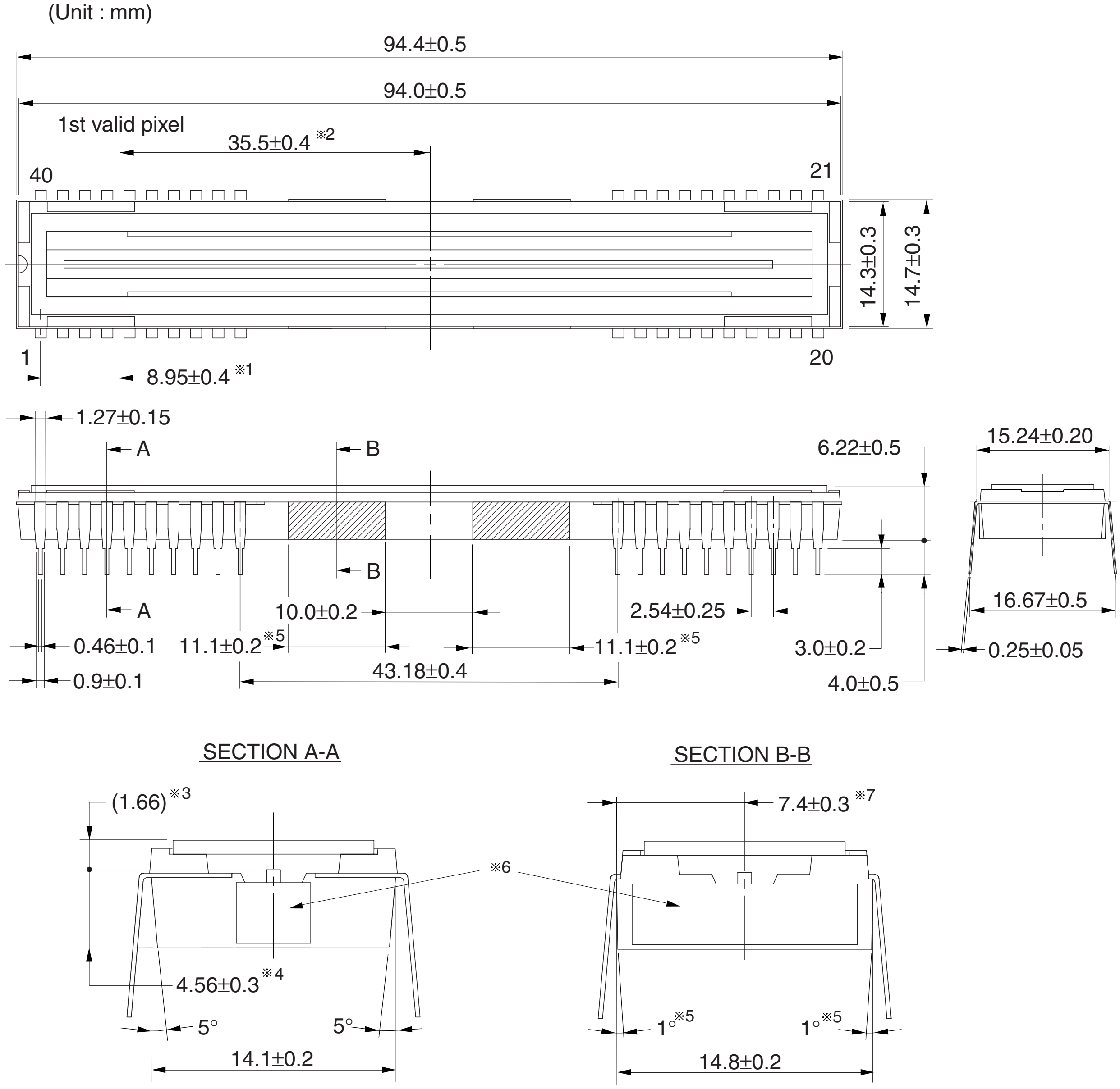


EQUIVALENT CIRCUIT B1 to B6



PACKAGE DRAWING

μPD8827BCZ-A
CCD LINEAR IMAGE SENSOR 40-PIN PLASTIC DIP (WITH HEAT SINK) (15.24mm (600))



Name	Dimensions	Refractive index
Glass cap	91.0×11.6×0.7	1.5

※1 1st valid pixel ←→ The center of the pin1
※2 1st valid pixel ←→ The center of the package
※3 The surface of the CCD chip ←→ The top of the cap
※4 The bottom of the package ←→ The surface of the CCD chip
※5 The draft angle of the shaded portions (4 places) are 1 dgree.
※6 There is no heat sink exposure from the package.
※7 The center of the CCD chip ←→ Package side(shaded portion)

40C-1CCD-PKG2

RECOMMENDED SOLDERING CONDITIONS

When soldering this product, it is highly recommended to observe the conditions as shown below.

If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

Type of Through-hole Device

μPD8827BCZ-A: CCD linear image sensor 40-pin plastic DIP with heat sink (15.24 mm (600))

Process	Conditions
Partial heating method	Pin temperature: 380°C or below, Heat time: 3 seconds or less (per pin).

Cautions 1. During assembly care should be taken to prevent solder or flux from contacting the glass cap. The optical characteristics could be degraded by such contact.

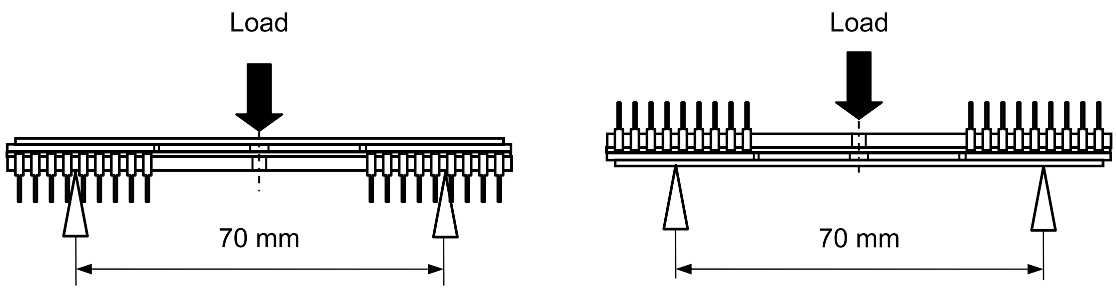
2. Soldering by the solder flow method may have deleterious effects on prevention of glass cap soiling and heat resistance. So the method cannot be guaranteed.

NOTES OF HANDLING THE PACKAGES

The application of an excessive load to the package may cause the package to warp or break, or cause chips to come off internally. Particular care should be taken when mounting the package on the circuit board. You should not reform the lead frame. We recommend to use a IC-inserter when you assemble to PCB.

For this product, the reference value for the three-point bending strength Note is 280[N]. Avoid imposing a load, however, on the inside portion as viewed from the face on which the window (glass) is bonded to the package body.

Note Three-point bending strength test
Distance between supports: 70 mm, Support R: R2 mm, Loading rate: 0.5 mm/min.



NOTES OF HANDLING

1. MOUNTING OF THE PACKAGE

The application of an excessive load to the package may cause the package to warp or break, or cause chips to come off internally. Particular care should be taken when mounting the package on the circuit board. Don't have any object come in contact with glass cap. You should not reform the lead frame. We recommend to use a IC-inserter when you assemble to PCB.

Also, be care that any of the following can cause the package to crack or dust to be generated.

1. Applying heat to the external leads for an extended period of time with soldering iron.
2. Rapid cooling or heating
3. Applying repetitive bending stress to the external leads.

2. GLASS CAP

Don't either touch glass cap surface by hand or have any object come in contact with glass cap surface. Care should be taken to avoid mechanical or thermal shock because the glass cap is easily to damage. For dirt stuck through electricity ionized air is recommended.

3. OPERATE AND STORAGE ENVIRONMENTS

Operate in clean environments. CCD image sensors are precise optical equipment that should not be subject to mechanical shocks. Exposure to high temperatures or humidity will affect the characteristics. So avoid storage or usage in such conditions.

Keep in a case to protect from dust and dirt. Dew condensation may occur on CCD image sensors when the devices are transported from a low-temperature environment to a high-temperature environment. Avoid such rapid temperature changes.

For more detail, refer to our document "Review of Quality and Reliability Handbook" (C12769E)

4. ELECTOROSTATIC BREAKDOWN

CCD image sensor is protected against static electricity, but destruction due to static electricity is something detected. Before handling, be sure to take the following protective measures.

1. Ground the tools such as soldering iron, radio cutting pliers of or pincer.
2. Install a conductive mat or on the floor or working table to prevent the generation of static electricity.
3. Either handle bare handed or use non chargeable gloves, clothes or material.
4. Ionized air is recommended for discharge when handling CCD image sensor.
5. For the shipment of mounted substrates, use box treated for prevention of static charges.
6. Anyone who is handling CCD image sensors, mounting them on PCB or testing or inspecting PCBs on which semiconductor devices have been mounted must wear anti-static bands such as wrist straps and ankle straps which are grounded via a series resistance connection of about 1MΩ.

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

[MEMO]