NIKO-SEM

P-Channel Enhancement Mode Field Effect Transistor

PJ527BA

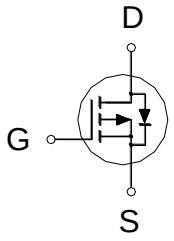
J-Lead

Halogen-Free & Lead-Free

RoHS Compliant

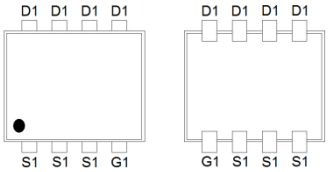
PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
-30V	14mΩ	-8A



Features

- Pb−Free, Halogen Free and RoHS compliant.
- Low $R_{DS(on)}$ to Minimize Conduction Losses.
- Ohmic Region Good $R_{DS(on)}$ Ratio.
- Optimized Gate Charge to Minimize Switching Losses.



G : GATE
D : DRAIN
S : SOURCE

Applications

- Protection Circuits Applications.
- Logic/Load Switch Circuits Applications.

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±25	V
Continuous Drain Current	T_A = 25 °C	I_D	-8	A
	T_A = 70 °C		-6.4	
Pulsed Drain Current[1]		I_{DM}	-50	
Avalanche Current		I_{AS}	-25.7	
Avalanche Energy	L = 0.1mH	E_{AS}	33	mJ
Power Dissipation	T_A = 25 °C	P_D	1.6	W
	T_A = 70 °C		1	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient	$R_{\theta JA}$		76	°C / W

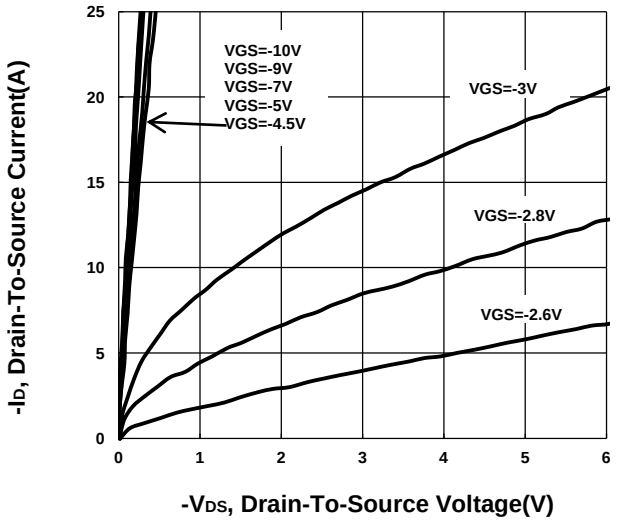
[1]Pulse width limited by maximum junction temperature.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

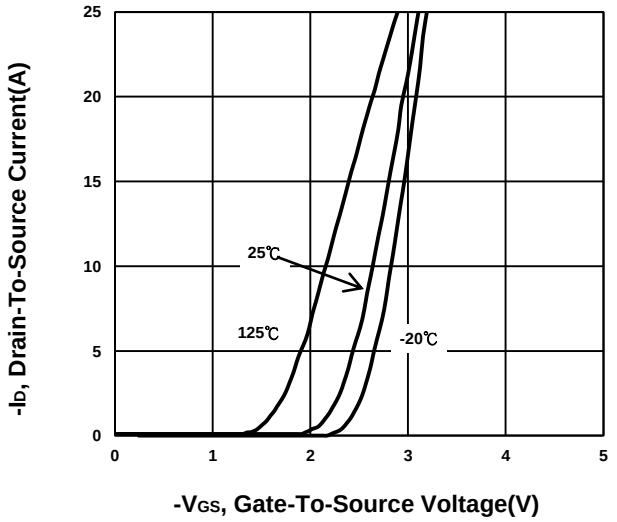
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-1.1	-1.7	-2.1	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±25V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -24V, V_{GS} = 0V			-1	μA
		V_{DS} = -20V, V_{GS} = 0V, T_J = 70 °C			-10	
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = -4.5V, I_D = -8A		17	22	mΩ
		V_{GS} = -10V, I_D = -8A		11.3	14	
Forward Transconductance[1]	g_{fs}	V_{DS} = -5V, I_D = -8A		33		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = -15V, f = 1MHz		1634		pF
Output Capacitance	C_{oss}			250		
Reverse Transfer Capacitance	C_{rss}			189		
Gate Resistance	R_g	V_{GS} = 0V, V_{DS} = 0V, f = 1MHz		4.2		Ω
Total Gate Charge[2]	Q_g	V_{DS} = -15V , V_{GS} = -10V, I_D = -8A		32		nC
Gate-Source Charge[2]	Q_{gs}			4.1		
Gate-Drain Charge[2]	Q_{gd}			7.5		
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DS} = -15V , I_D ≅ -8A, V_{GS} = -10V, R_G = 6 Ω		16		nS
Rise Time[2]	t_r			54		
Turn-Off Delay Time[2]	$t_{d(off)}$			64		
Fall Time[2]	t_f			90		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				-1.3	A
Forward Voltage[1]	V_{SD}	I_F = -8A, V_{GS} = 0V			-1.2	V
Reverse Recovery Time	t_{rr}	I_F = -8A, dI_F/dt = 100A / μS		19		nS
Reverse Recovery Charge	Q_{rr}			8		nC

[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature.

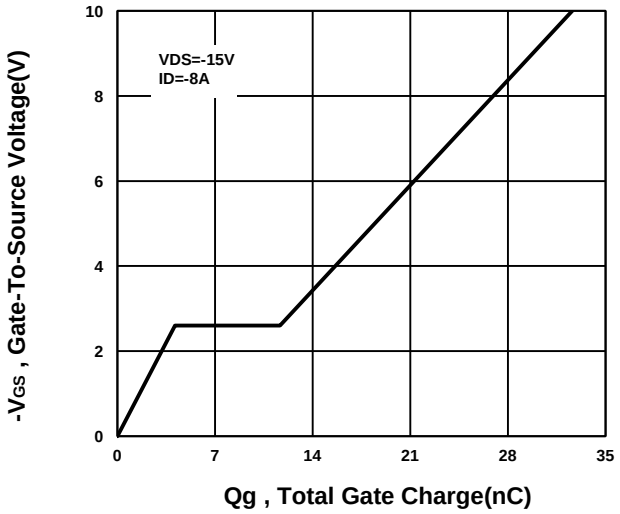
Output Characteristics



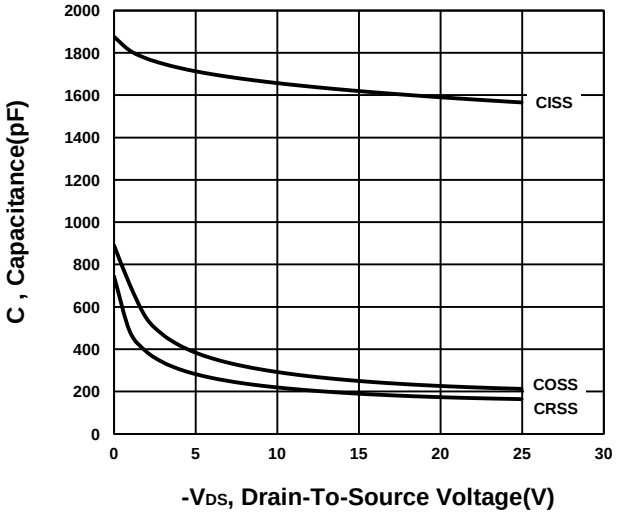
Transfer Characteristics



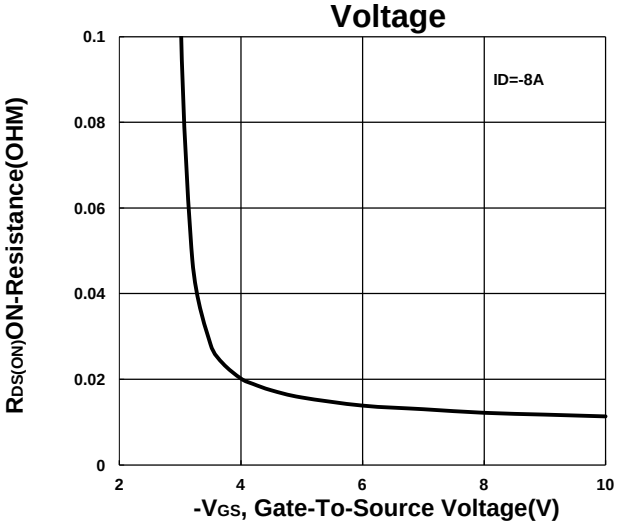
Gate charge Characteristics



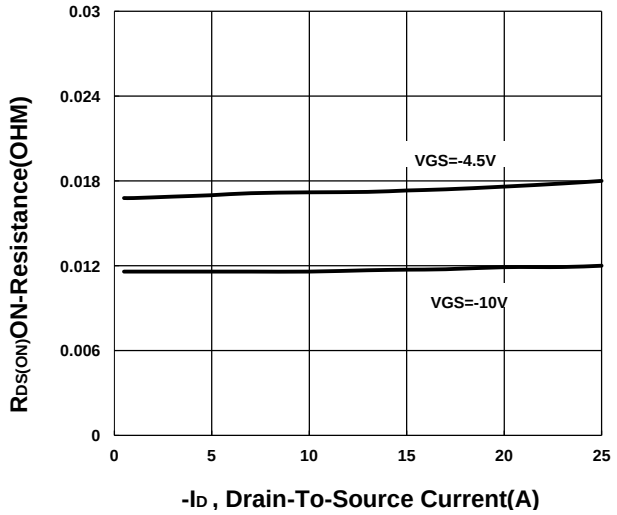
Capacitance Characteristic



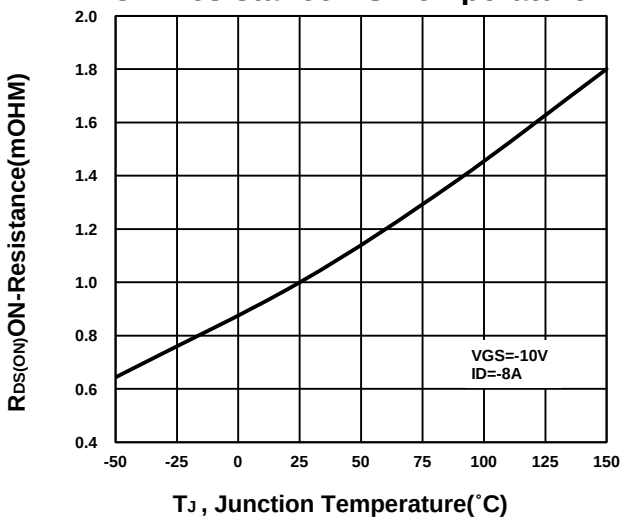
On-Resistance VS Gate-To-Source Voltage



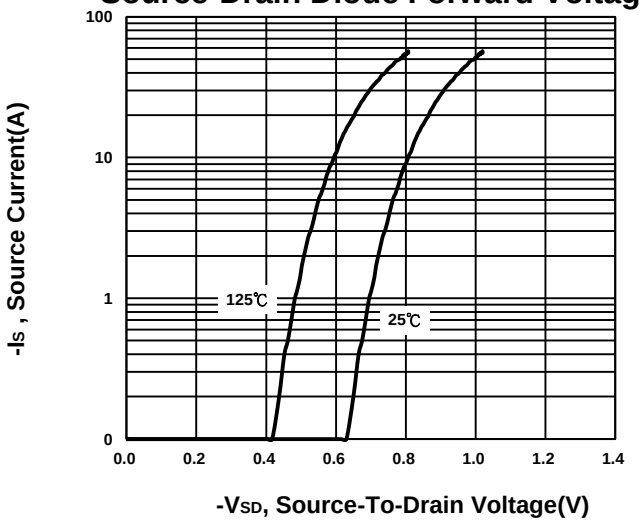
On-Resistance VS Drain Current



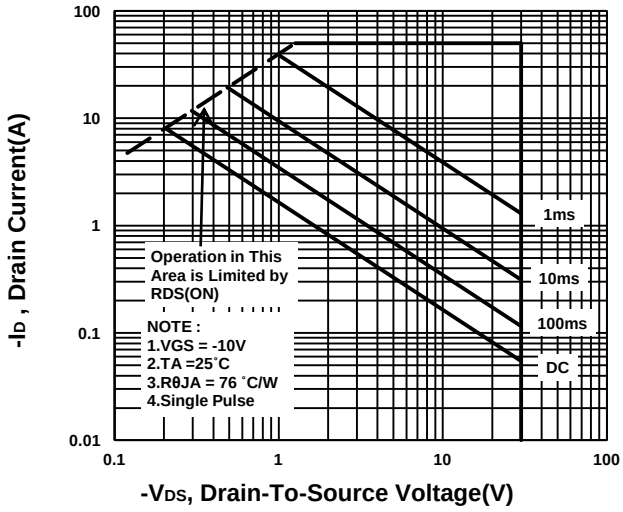
On-Resistance VS Temperature



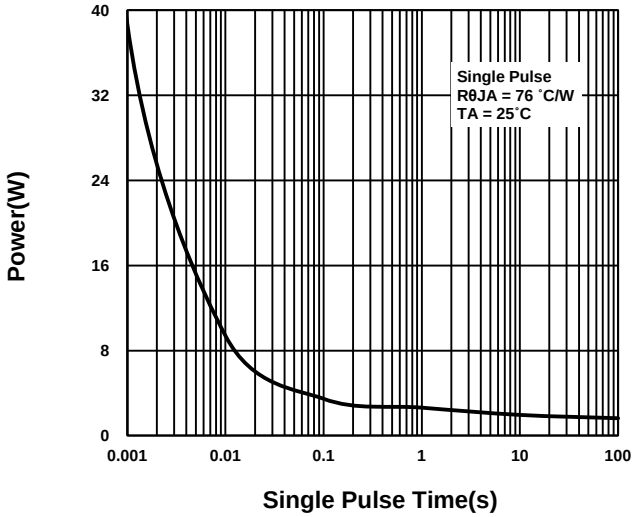
Source-Drain Diode Forward Voltage



Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve