

SONET/SDH Payload Extractor/Aligner

FEATURES

- Monolithic, SONET/SDH Payload Extractor/Aligner for use in STS-1 (STM-0/AU3), STS-3 (STM-1/AU3) or STS-3c (STM-1/AU4) interface applications, operating at serial interface speeds up to 155.52 Mbit/s.
- Provides integrated clock recovery and clock synthesis to allow a direct interface to optical modules.
- Provides termination for SONET Section and Line, SDH Regenerator Section and Multiplexer Section transport overhead, and Path overhead of one or three STS-1 (STM-0/AU3) paths or a single STS-3c (STM-1/AU4) path.
- Maps one or three STS-1 (STM-0/AU3) payloads or a single STS-3c (STM-1/AU4) payload to system timing reference, accommodating plesiochronous timing offsets between the references through pointer processing.

- Maps three DS3 bit streams into a STS-3 (STM-1/AU3) frame.
- Maps three serial data streams (e.g., Frame Relay, PPP, or Ethernet Payload) into a single serial data stream into a STS-1 (STM-0/AU3) or STS-3c (STM-1/AU4) payload.
- Supports line loopback from the line side receive stream to the transmit stream and diagnostic loopback from a Telecom ADD bus interface to a Telecom DROP bus interface.
- Provides a standard 5-signal P1149.1 JTAG test port for boundary scan board test purposes.
- Provides a generic 8-bit microprocessor bus interface for configuration, control, and status monitoring.
- Low power, +5 V, CMOS technology. Device has PECL- and TTL-compatible inputs and TTL outputs.

- Available in a 256-pin, Super Ball Grid Array (SBGA) package.
- Supports industrial temperature range (-40°C to 85°C) operation.

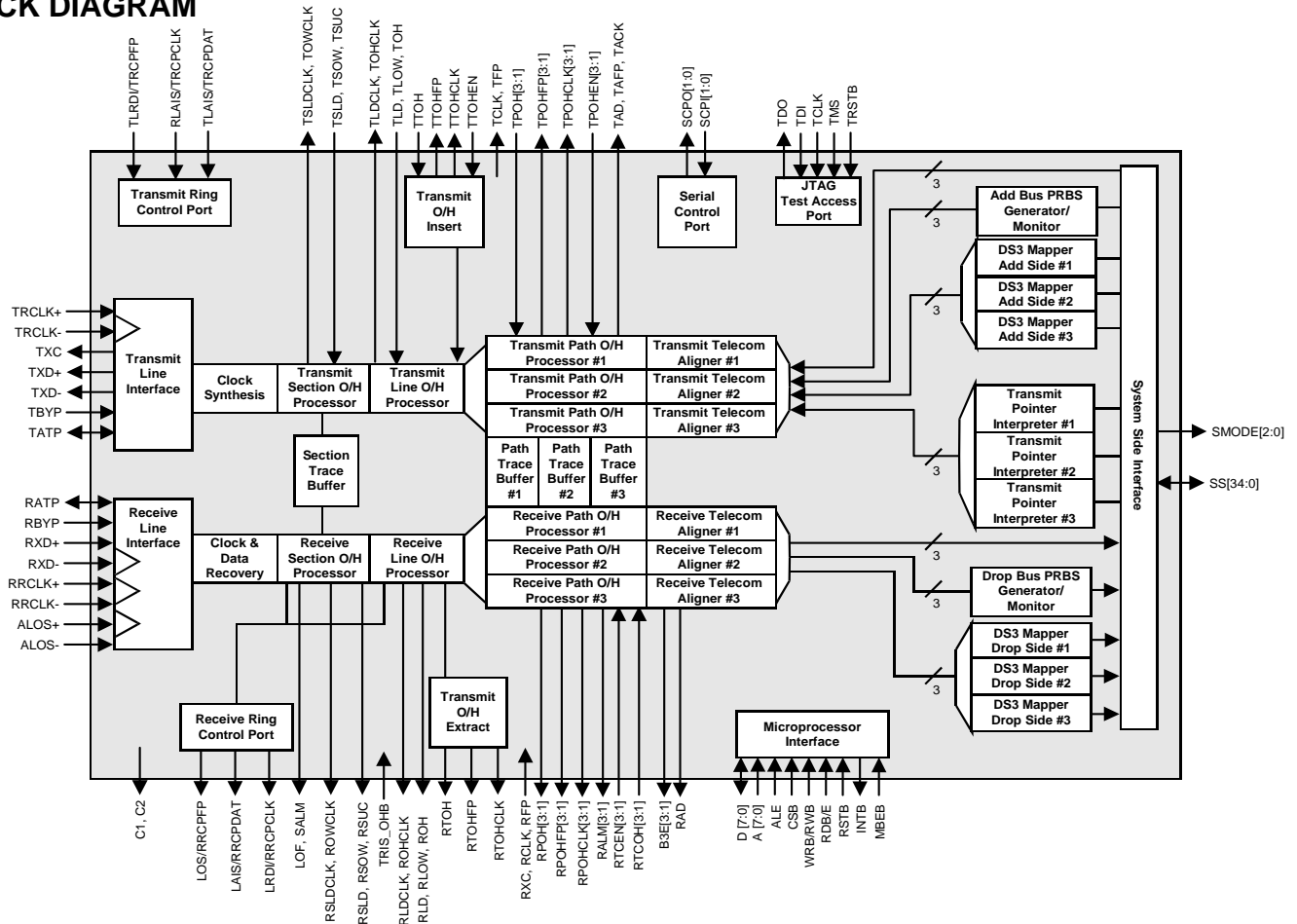
BACKPLANE/DEVICE MODES

- Telecom Byte.
- Telecom Nibble.
- Telecom Serial.
- Datacom Byte.
- Datacom Nibble.
- Datacom Serial.
- Datacom T3.

APPLICATIONS

- SONET/SDH Add/Drop Multiplexers
- SONET/SDH Terminal Multiplexers
- SONET/SDH Digital Cross-Connects
- Channelized Routers and Switches
- Packet Over SONET Router and Switches

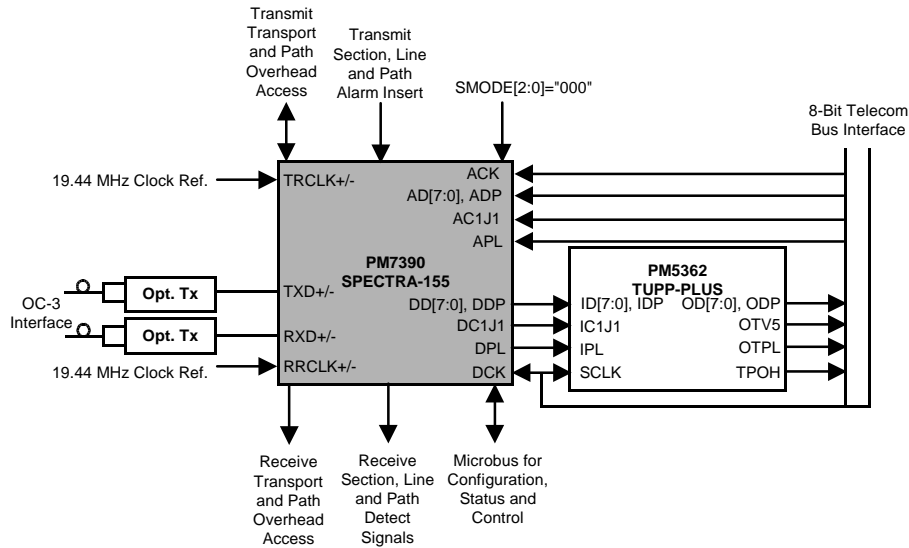
BLOCK DIAGRAM



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TYPICAL APPLICATIONS

STS-3/STM-1 AGGREGATE INTERFACE WITH TRIBUTARY POINTER PROCESSING AND PERFORMANCE MONITORING



CHANNELIZED OC-3 INTERFACE FOR HIGH SPEED ROUTERS

