DESCRIPTION

PT6961 is an LED Controller driven on a 1/7 to 1/8 duty factor. 11 segment output lines, 6 grid output lines, 1 segment/grid output lines, one display memory, control circuit, key scan circuit are all incorporated into a single chip to build a highly reliable peripheral device for a single chip microcomputer. Serial data is fed to PT6961 via a four-line serial interface. Housed in a 32-pin SOP, PT6961 pin assignments and application circuit are optimized for easy PCB Layout and cost saving advantages.

APPLICATIONS

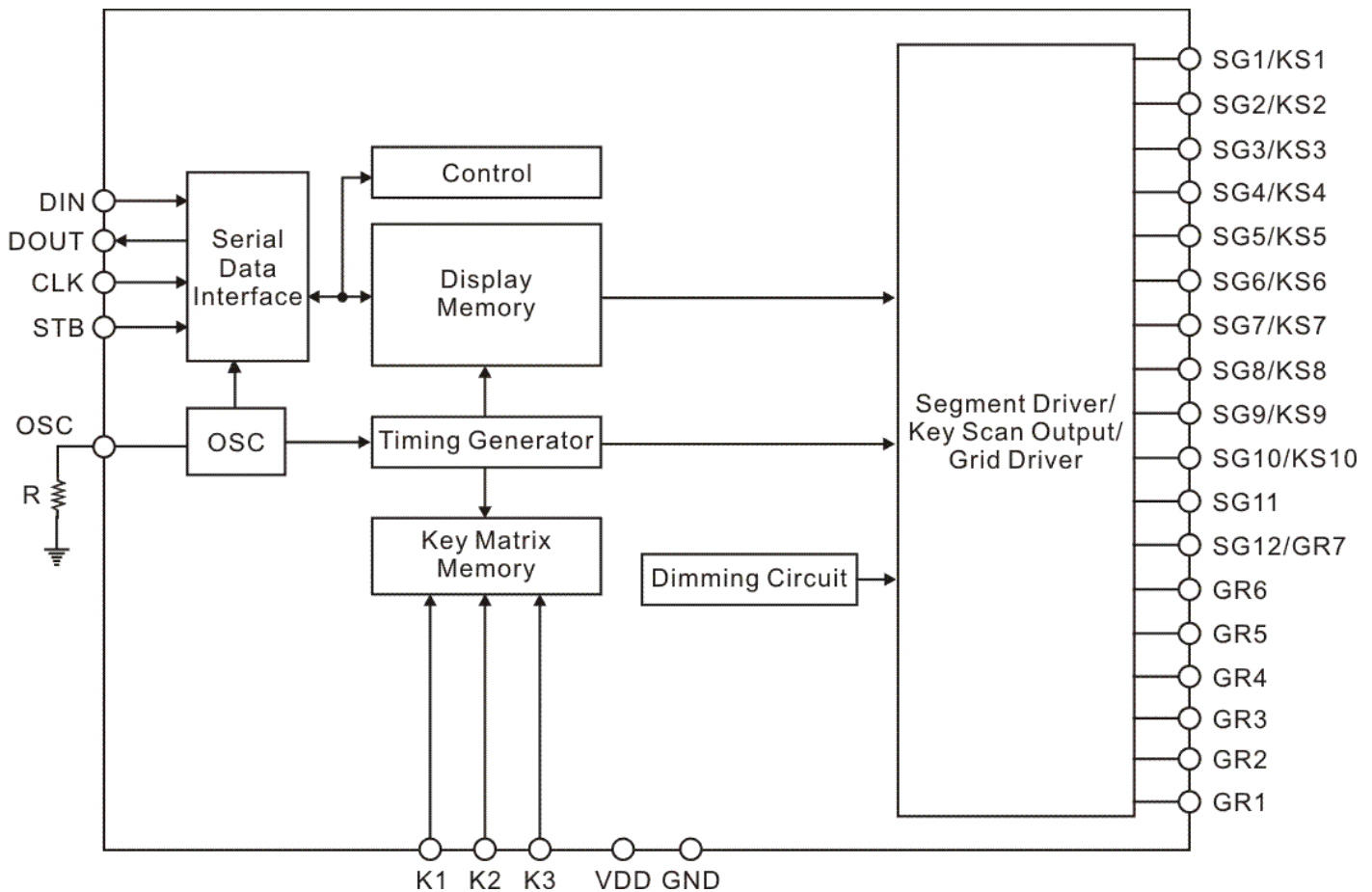- Micro-computer Peripheral Device
- VCR set
- Combo set

FEATURES

- CMOS technology
- Low power consumption
- Multiple display modes (12 segments, 6 grids to 11 segments, 7 grids)
- Key scanning (10 x 3 Matrix)
- 8-Step dimming circuitry
- Serial interface for Clock, Data Input, Data Output, Strobe Pins
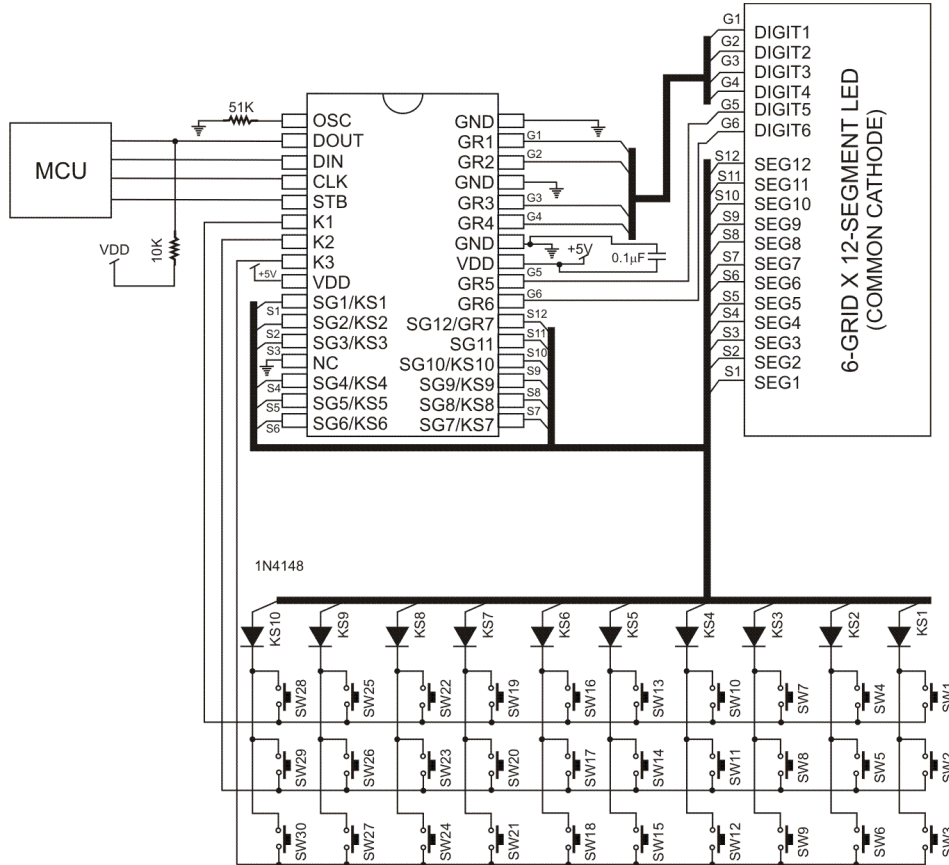- Available in 32-pin, SOP

BLOCK DIAGRAM
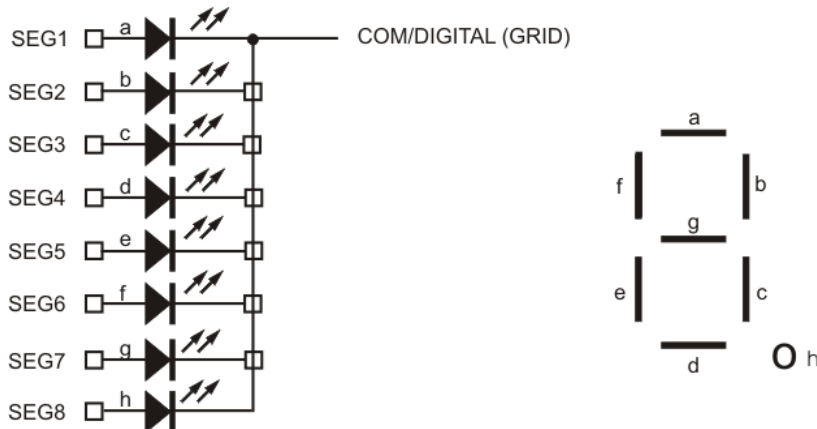
普 誠 科 技
Princeton Technology Corp.

APPLICATION CIRCUIT

Notes:
1. The capacitor (0.1µF) connected between the GND and the VDD pins must be located as close as possible to the PT6961 chip.
2. It is strongly suggested that the NC pin (pins 13) be connected to the GND.
3. The PT6961 power supply is separate from the application system power supply.
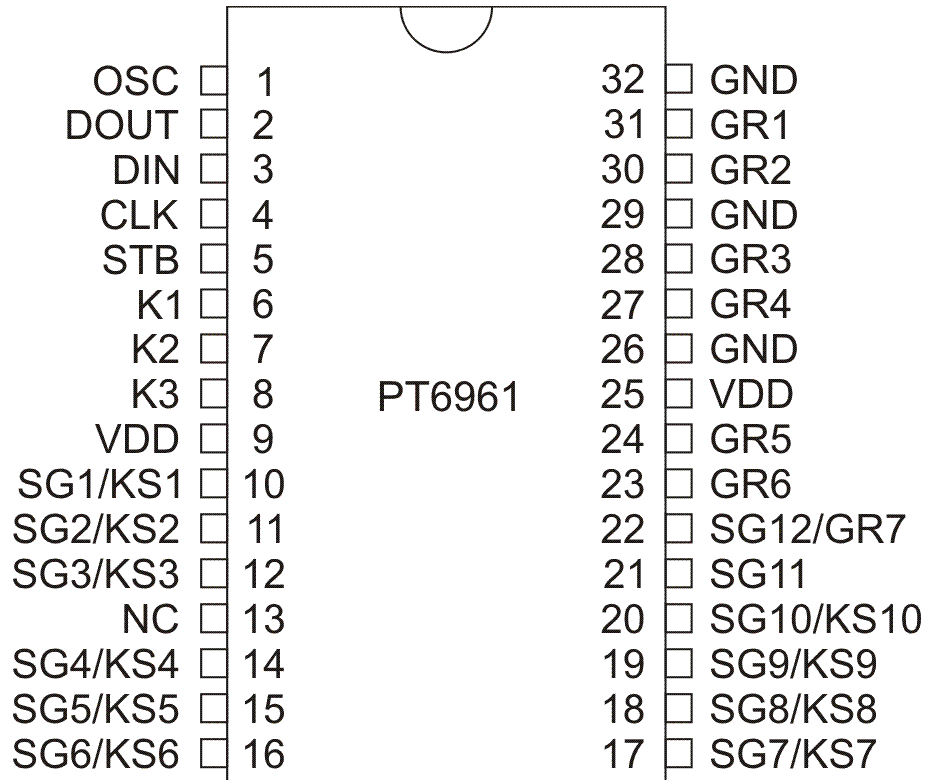
COMMON CATHODE TYPE LED PANEL

ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT6961	32pins, SOP, 300mil	PT6961

PIN DESCRIPTION

```
            OSC  □  1              32  □  GND
           DOUT  □  2              31  □  GR1
            DIN  □  3              30  □  GR2
            CLK  □  4              29  □  GND
            STB  □  5              28  □  GR3
             K1  □  6              27  □  GR4
             K2  □  7              26  □  GND
             K3  □  8    PT6961    25  □  VDD
            VDD  □  9              24  □  GR5
        SG1/KS1  □  10             23  □  GR6
        SG2/KS2  □  11             22  □  SG12/GR7
        SG3/KS3  □  12             21  □  SG11
             NC  □  13             20  □  SG10/KS10
        SG4/KS4  □  14             19  □  SG9/KS9
        SG5/KS5  □  15             18  □  SG8/KS8
        SG6/KS6  □  16             17  □  SG7/KS7
```

PIN DESCRIPTION

| Pin Name	I/O	Description	Pin No.
OSC	I	Oscillator Input Pin A resistor is connected to this pin to determine the oscillation frequency	1
DOUT	O	Data Output Pin (N-Channel, Open-Drain) This pin outputs serial data at the falling edge of the shift clock.	2
DIN	I	Data Input Pin This pin inputs serial data at the rising edge of the shift clock (starting from the lower bit)	3
CLK	I	Clock Input Pin This pin reads serial data at the rising edge and outputs data at the falling edge.	4
STB	I	Serial Interface Strobe Pin The data input after the STB has fallen is processed as a command. When this pin is "HIGH", CLK is ignored.	5
K1 ~ K3	I	Key Data Input Pins The data sent to these pins are latched at the end of the display cycle. (Internal Pull-Low Resistor)	6, 7, 8
VDD	-	Power Supply	9, 25
SG1/KS1 ~ SG10/KS10	O	Segment Output Pins (p-channel, open drain) Also acts as the Key Source	10 ~ 12 14 ~ 20
NC	-	No Connection	13
SG11	O	Segment Output pins (P-Channel, open drain)	21
SG12/GR7	O	Segment / Grid Output Pins	22
GR6 ~ GR1	O	Grid Output Pins	23, 24, 27, 28, 30, 31
GND	-	Ground Pin	26, 29, 32

INPUT/OUTPUT CONFIGURATIONS

The schematic diagrams of the input and output circuits of the logic section are shown below.
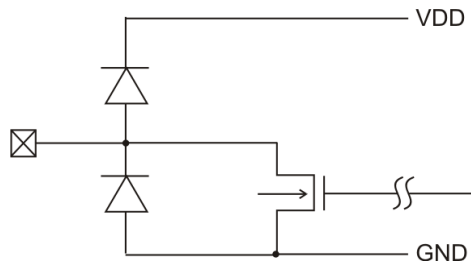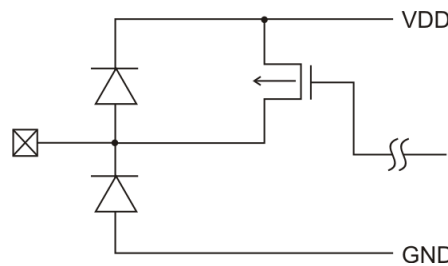
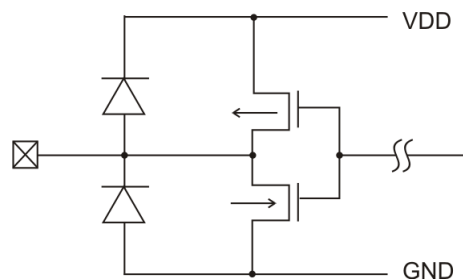## INPUT PINS: CLK, STB & DIN
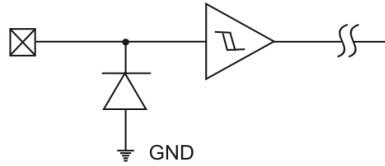
OUTPUT PINS: K1 TO K3
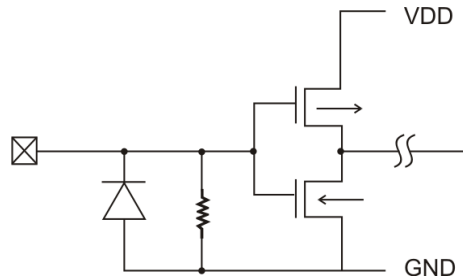
OUTPUT PINS: DOUT, GR1 TO GR4

OUTPUT PINS: SG1 TO SG11

OUTPUT PINS: GR5, GR6 AND SG12/GR7

FUNCTION DESCRIPTION

COMMANDS

A command is the first byte (b0 to b7) inputted to PT6961 via the DIN Pin after STB Pin has changed from HIGH to LOW State. If for some reason the STB Pin is set to HIGH while data or commands are being transmitted, the serial communication is initialized, and the data/commands being transmitted are considered invalid.

COMMANDS 1: DISPLAY MODE SETTING COMMANDS

PT6961 provides 2 display mode settings as shown in the diagram below: As stated earlier a command is the first one byte (b0 to b7) transmitted to PT6961 via the DIN Pin when STB is LOW. However, for these commands, the bit 3 & bit 8 (b2 to b7) are given a value of 0.

The Display Mode Setting Commands determine the number of segments and grids to be used (12 to 11 segments, 6 to 7 grids). A display command ON must be executed in order to resume display. If the same mode setting is selected, no command execution is take place, therefore, nothing happens.
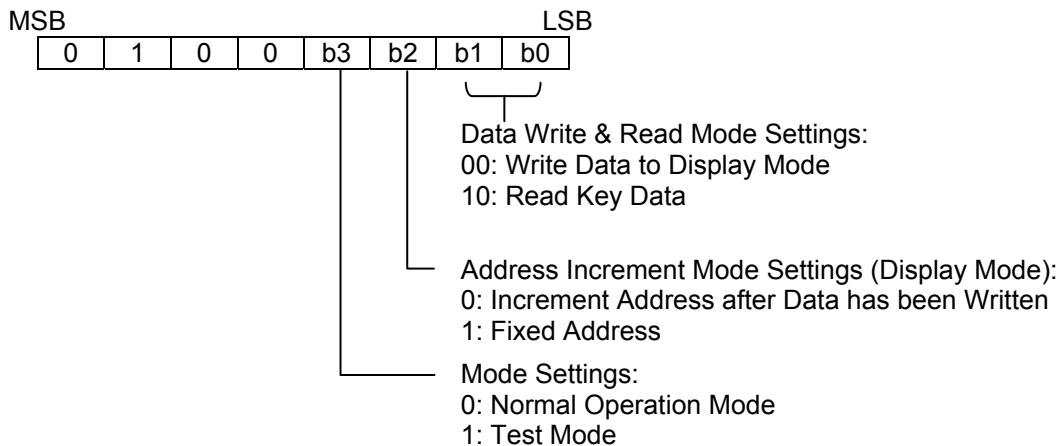
When Power is turned ON, the 7-grid, 11-segment modes is selected.

MSB							LSB
0	0	0	0	0	0	b1	b0

Display Mode Settings:
10: 6 digits, 12 segments
11: 7 digits, 11 segments
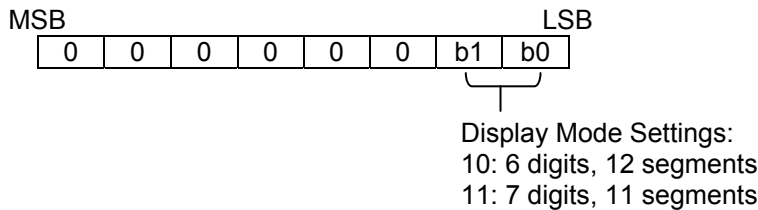
COMMANDS 2: DATA SETTING COMMANDS

The Data Setting Commands executes the Data Write or Data Read Modes for PT6961. The data
Setting Command, the bits 5 and 6 (b4, b5) are given the value of 0, bit 7 (b6) is given the value of 1 while bit 8 (b7) is given the value of 0. Please refer to the diagram below.

When power is turned ON, bit 4 to bit 1 (b3 to b0) are given the value of 0.

MSB							LSB
0	1	0	0	b3	b2	b1	b0

Data Write & Read Mode Settings:
00: Write Data to Display Mode
10: Read Key Data

Address Increment Mode Settings (Display Mode):
0: Increment Address after Data has been Written
1: Fixed Address

Mode Settings:
0: Normal Operation Mode
1: Test Mode

PT6961 KEY MATRIX & KEY INPUT DATA STORAGE RAM

PT6961 Key Matrix consists of 10 x 3 array as shown below:
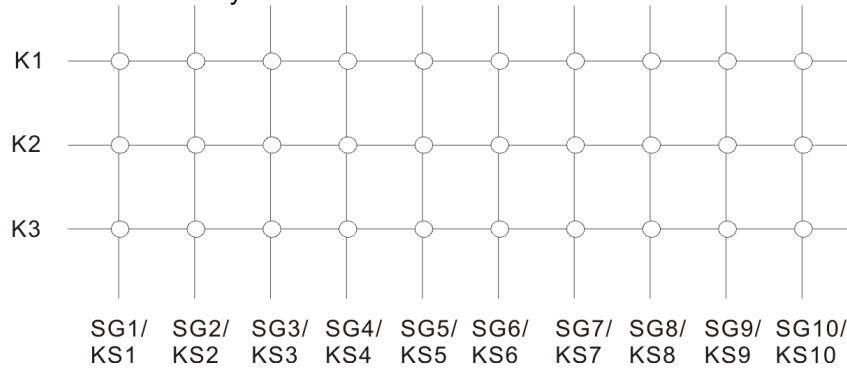
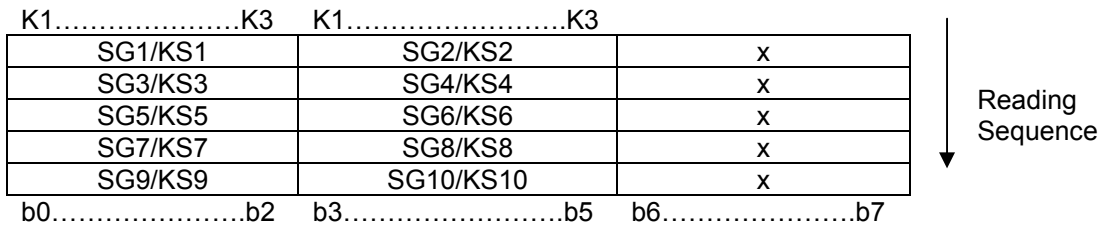Each data entered by each key is stored as follows and read by a READ Command, starting from the last significant bit. When the most significant bit of the data (b7) has been read, the least significant bit of the next data (b0) is read.

K1.....................K3	K1........................K3	
SG1/KS1	SG2/KS2	x
SG3/KS3	SG4/KS4	x
SG5/KS5	SG6/KS6	x
SG7/KS7	SG8/KS8	x
SG9/KS9	SG10/KS10	x
b0.....................b2	b3........................b5	b6.....................b7

Reading Sequence

Note: b6 and b7 do not care.

COMMANDS 3: ADDRESS SETTING COMMANDS

Address Setting Commands are used to set the address of the display memory. The address is considered valid if it has a value of 00H to 0DH. If the address is set to 0EH or higher, the data is ignored until a valid address is set. When power is turned ON, the address is set at 00H.

Please refer to the diagram below.

MSB | 1 | 1 | 0 | 0 | b3 | b2 | b1 | b0 | LSB

Address: 00H to 0DH
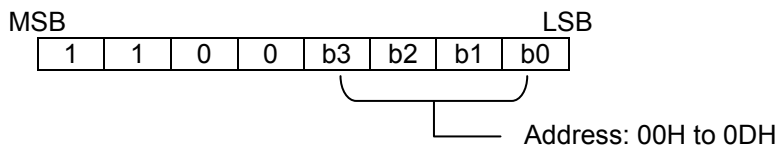
DISPLAY MODE AND RAM ADDRESS

Data transmitted from an external device to PT6961 via the serial interface are stored in the Display RAM and are assigned addresses. The RAM addresses of PT6961 are given below in 8 bits unit.

SG1 ... SG4	SG5 ... SG8	SG9 ... SG12	SG13 ... SG14	
00HL	00HU	01HL	01HU	DIG1
02HL	02HU	03HL	03HU	DIG2
04HL	04HU	05HL	05HU	DIG3
06HL	06HU	07HL	07HU	DIG4
08HL	08HU	09HL	09HU	DIG5
0AHL	0AHU	0BHL	0BHU	DIG6
0CHL	0CHU	0DHL	0DHU	DIG7

b0 ... b3	b4 ... b7
xxHL	xxHU
Lower 4 bits	Higher 4 bits
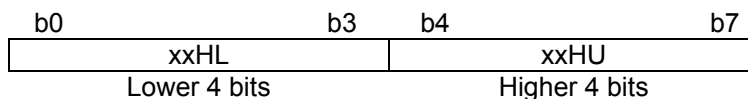
COMMAND 4: DISPLAY CONTROL COMMANDS

The Display Control Commands are used to turn ON or OFF a display. It also used to set the pulse width. Please refer to the diagram below. When the power is turned ON, a 1/16 pulse width is selected and the displayed is turned OFF (the key scanning is started).

MSB   LSB

| 1 | 0 | 0 | 0 | b3 | b2 | b1 | b0 |

Dimming Quantity Settings:
000: Pulse width = 1/16
001: Pulse width = 2/16
010: Pulse width = 4/16
011: Pulse width = 10/16
100: Pulse width – 11/16
101: Pulse width = 12/16
110: Pulse width = 13/16
111: Pulse width = 14/16

Display Settings:
0: Display Off (Key Scan Continues)
1: Display On
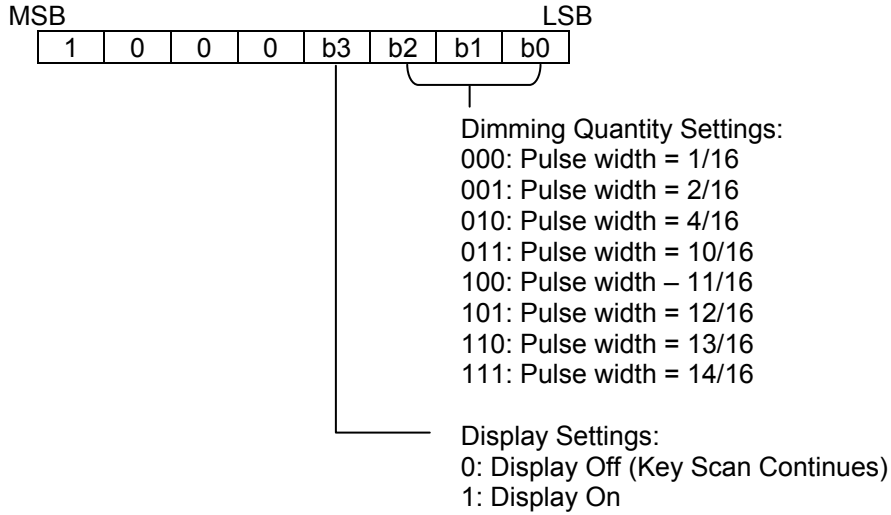
SCANNING AND DISPLAY TIMING

1 Frame = $T_{DISPLAY}$ x (n +1)
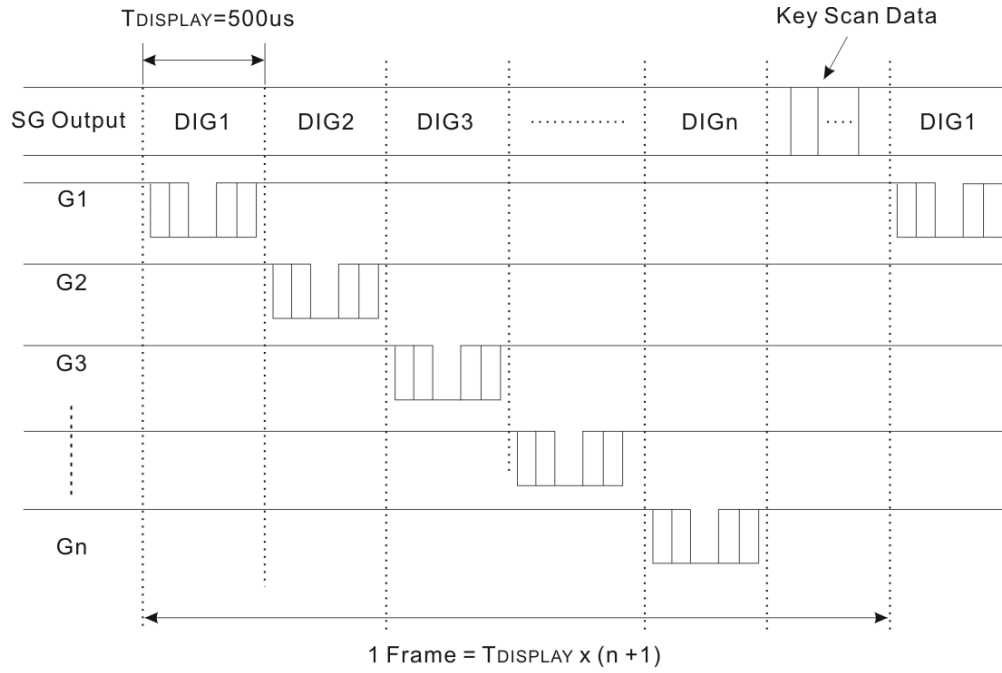
SERIAL COMMUNICATION FORMAT

The following diagram shows the PT6961 serial communication format. The DOUT Pin is an N-channel, open-drain output pin; therefore, it is highly recommended that an external pull-up resistor (1 KΩ to 10 KΩ) must be connected to DOUT.

RECEPTION (DATA/COMMAND WRITE)
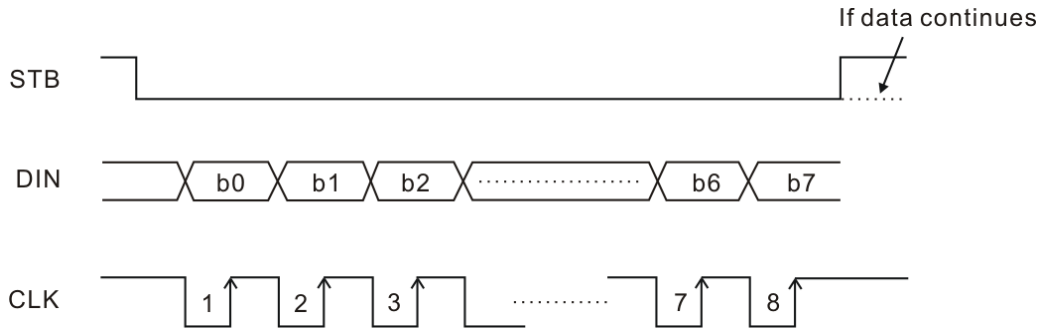
TRANSMISSION (DATA READ)
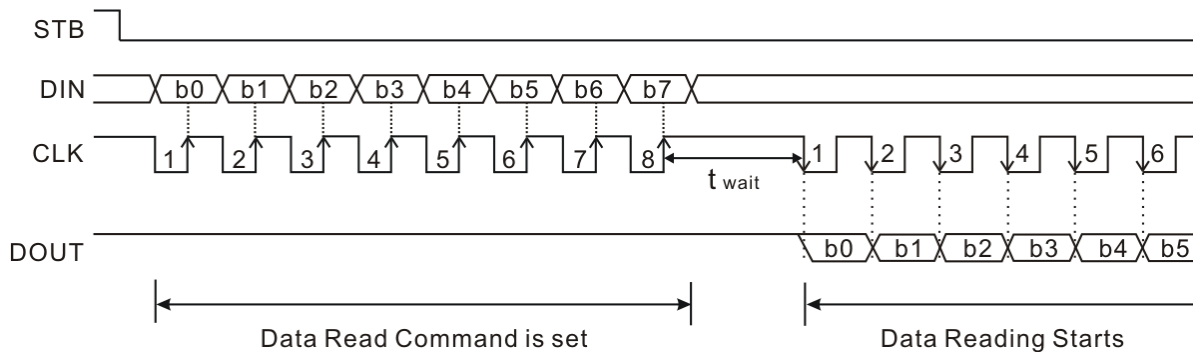
where: twait (waiting time) ≥ 1μs

It must be noted that when the data is read, the waiting time (twait) between the rising of the eighth clock that has set the command and the falling of the first clock that has read the data is greater or equal to 1μs.

SWITCHING CHARACTERISTIC WAVEFORM

PT6961 Switching Characteristics Waveform is given below.
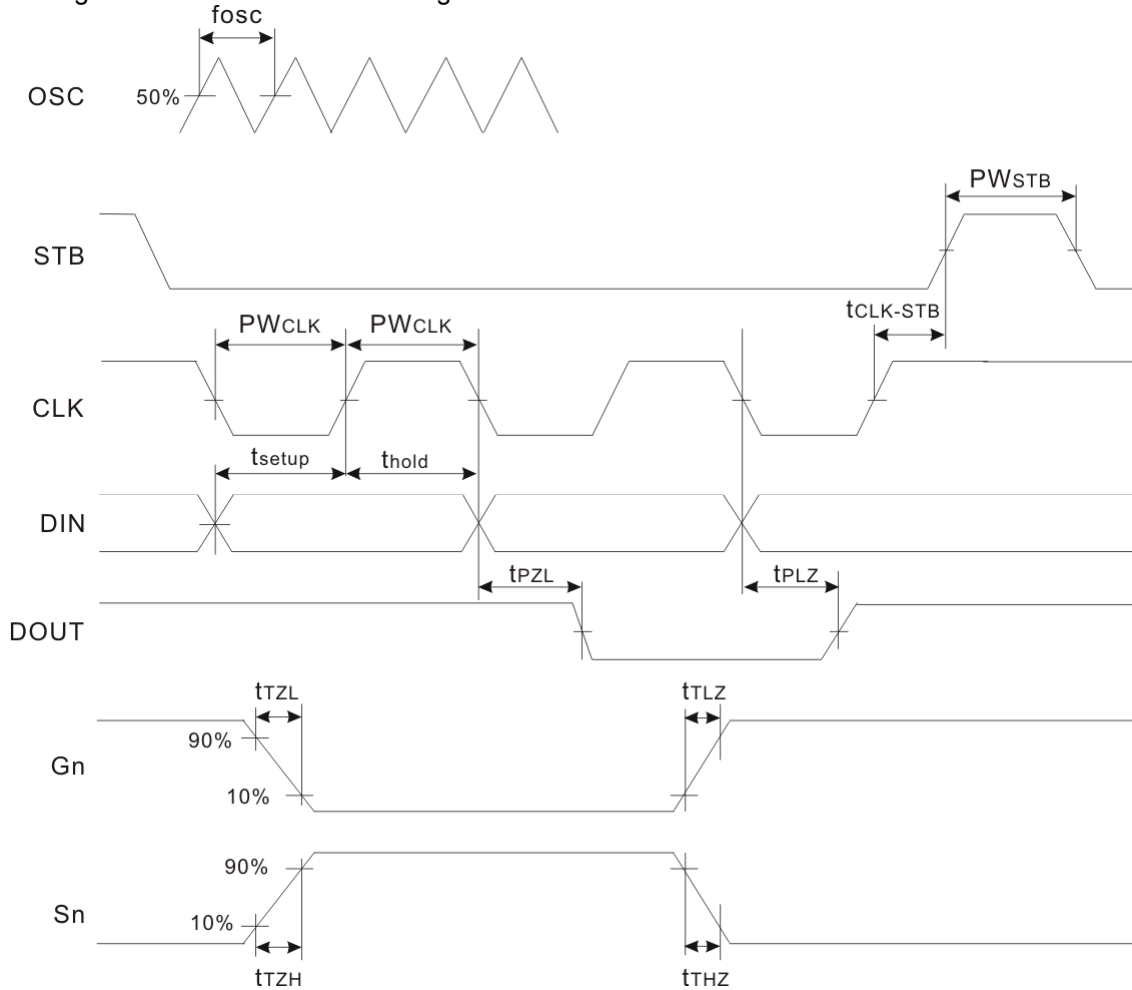
where:

PW_{CLK} (Clock Pulse Width) ≥ 400ns

t_{setup} (Data Setup Time) ≥100ns

$t_{CLK-STB}$ (Clock – Strobe Time) ≥ 1μs

t_{TZH} (Rise Time) ≤ 1 μs

fosc = Oscillation Frequency

t_{TZL} ≤ 1μs

PW_{STB} (Strobe Pulse Width) ≥ 1μs

t_{hold} (Data Hold Time) ≥ 100ns

t_{THZ} (Fall Time) ≤ 10μs

t_{PZL} (Propagation Delay Time) ≤ 100ns

t_{PLZ} (Propagation Delay Time) ≤ 300ns

t_{TLZ} ≤ 10 μs

Note:

Test Condition Under

t_{THZ} (Pull low resistor) = 10KΩ, Loading capacitor = 300pF

t_{TLZ} (Pull high resistor) = 10KΩ, Loading capacitor = 300pF

APPLICATIONS

Display memory is updated by incrementing addresses. Please refer to the following diagram.
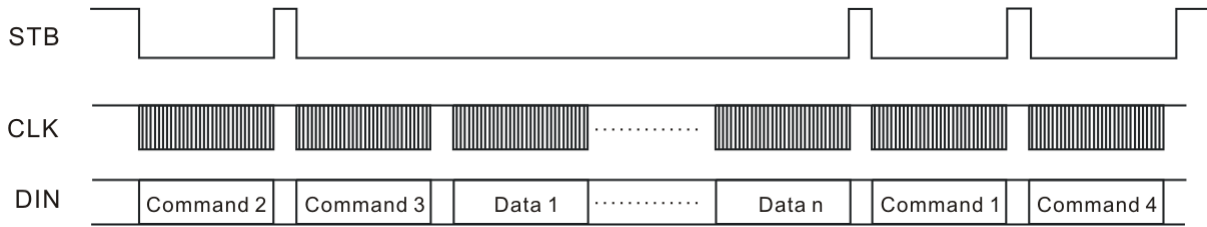
where:
Command 1: Display mode setting command
Command 2: Data setting command
Command 3: Address setting command
Data 1 to n: Transfer display data (14 bytes max.)
Command 4: Display control command

The following diagram shows the waveforms when updating specific addresses.
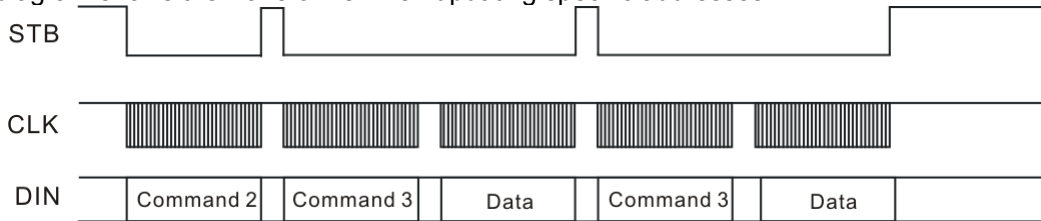
where:
Command 2: Data setting command
Command 3: Address setting command
Data: Display data

RECOMMENDED SOFTWARE FLOWCHART

```
                    START
                      |
                Delay 200 ms
                      |
                    SET
                COMMAND 2
                (Write Data)  ─────────┐
                      |                 |
                    SET                 |
                COMMAND 3               |
              Clear Display RAM         |
                (See Note 5)            |
                      |                 |
                    SET                 |
                COMMAND 1          INITIAL
                      |            SETTING
                SET COMMAND 4
              (80H ~ 87H: Display OFF)
                      |
                    SET
                COMMAND 1
                      |
                    SET
                COMMAND 4
            (88H ~ 8FH : Display ON) ───┘
                      |
                   MAIN          ◄──────┐
                  PROGRAM               |
                      |                 |
                    SET                 |
                COMMAND 2               |
              (READ KEY & WRITE         |
               DATA INCLUDED)      MAIN  |
                      |            LOOP  |
                    SET                 |
                COMMAND 3               |
                      |                 |
                    SET                 |
                COMMAND 1               |
                      |                 |
                    SET                 |
                COMMAND 4  ─────────────┘
                      |
                    END
```
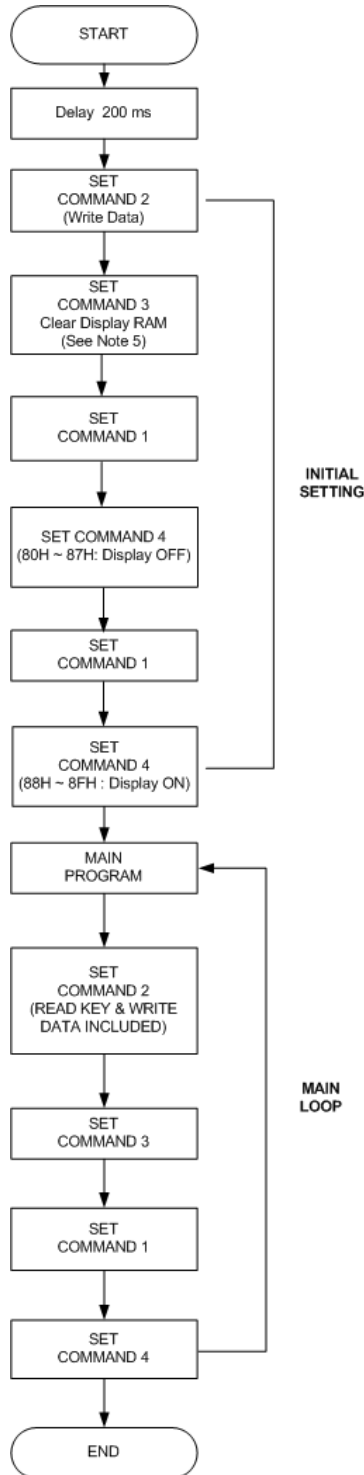
Notes:
1. Command 1: Display Mode Commands
2. Command 2: Data Setting Commands
3. Command 3: Address Setting Commands
4. Command 4: Display Control Commands
5. When IC power is applied for the first time, the contents of the Display RAM are not defined; thus, it is strongly suggested that the contents of the Display RAM be cleared during the initial setting.

SOP 32 (300MIL) THERMAL PERFORMANCE IN STILL AIR

JUNCTION TEMPERATURE: 100℃
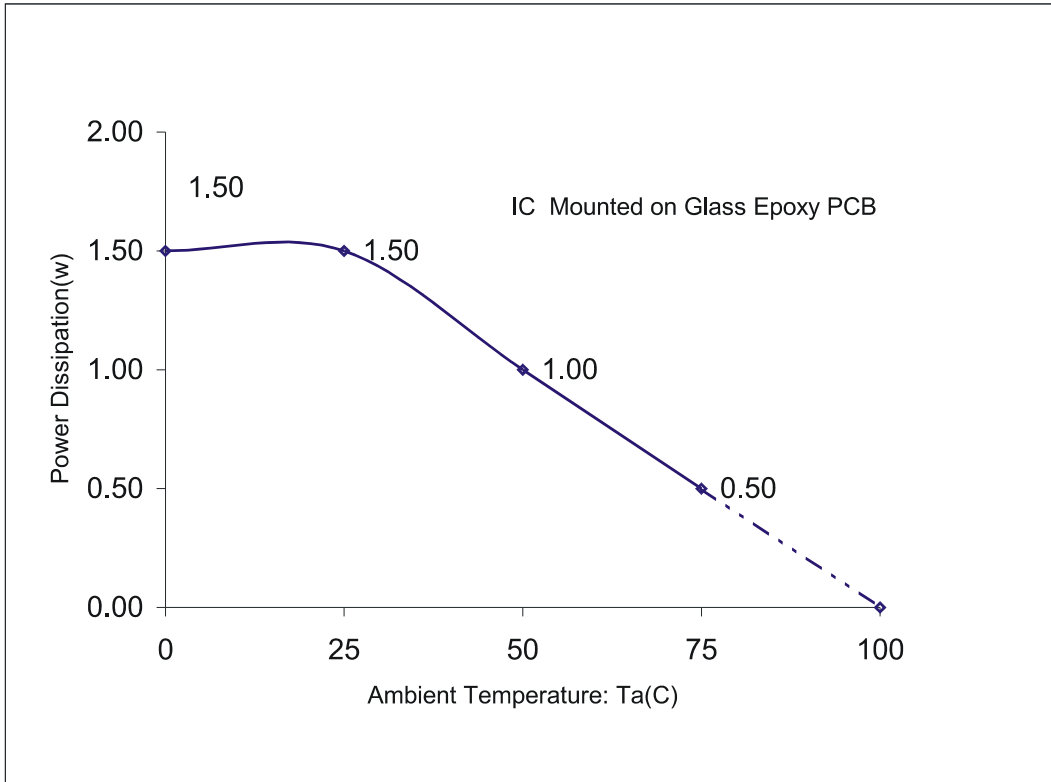
ABSOLUTE MAXIMUM RATINGS

(Unless otherwise specified, Ta=25℃, GND=0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	VDD	-0.5 to +7	V
Logic input voltage	VI	-0.5 to VDD+0.5	V
Driver output current	IOLGR	+250	mA
	IOHSG	-50	mA
Maximum driver output current/total	ITOTAL	400	mA
Operating temperature	Topr	-40 ~ +85	℃
Storage temperature	Tstg	-65 ~ +150	℃

RECOMMENDED OPERATING RANGE

(Unless otherwise specified, Topr=25℃, GND=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Logic supply voltage	VDD	VDD	3	5	5.5	V
Dynamic current (see Note)	IDDdyn	VDD	-	-	5	mA
High-level input voltage	VIH	VDD=5V	0.8 VDD	-	VDD	V
		VDD=3V	0.8 VDD	-	VDD	
Low-level input voltage	VIL	VDD=5V	0	-	0.3 VDD	V
		VDD=3V	0	-	0.3	

Note: Test Condition: Set Display Control Commands = 80H (Display Turn OFF State & under no load)

ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, VDD =5V, GND=0V, Ta=25°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
High-level output current	IOHSG(1)	VO= VDD -2V SG1 to SG11, SG12/GR7	-20	-25	-40	mA
	IOHSG(2)	VO= VDD -3V SG1 to SG11, SG12/GR7	-25	-30	-50	mA
Low-level output current	IOLGR	VO=0.3V GR1 to GR6, SG12/GR7	100	140	-	mA
Low-level output current	IOLDOUT	VO=0.4V	4	-	-	mA
Segment high-level output current tolerance	ITOLSG	VO= VDD -3V SG1 to SG11, SG12/GR7	-	-	±5	%
High-level input voltage	VIH	-	0.8VDD	-	5	V
Low-level input voltage	VIL	-	0	-	0.3VDD	V
Oscillation frequency	fosc	R=51KΩ	350	500	650	KHz
K1 to K3 pull down resistor	RKN	K1 to K3, VDD =5V	40	-	100	KΩ

(Unless otherwise stated, VDD =3V, GND=0V, Ta=25°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
High-level output current	IOHSG	VO=VDD-2V SG1 to SG11, SG12/GR7	-9	-12	-20	mA
Low-level output current	IOLGR	VO=0.3V GR1 to GR6, SG12/GR7	80	100	-	mA
Low-level output current	IOLDOUT	VO=0.4V	3	-	-	mA
Segment high-level output current tolerance	ITOLSG	VO= VDD -2V SG1 to SG11, SG12/GR7	-	-	±5	%
High-level input voltage	VIH	-	0.8VDD	-	VDD	V
Low-level input voltage	VIL	-	0	-	0.3	V
Oscillation frequency	fosc	R=33KΩ	350	500	650	KHz
K1 to K3 pull down resistor	RKN	K1 to K3, VDD=3V	90	-	180	KΩ

PACKAGE INFORMATION

32 PINS, SOP, 300 MIL

PIN 1 INDENT
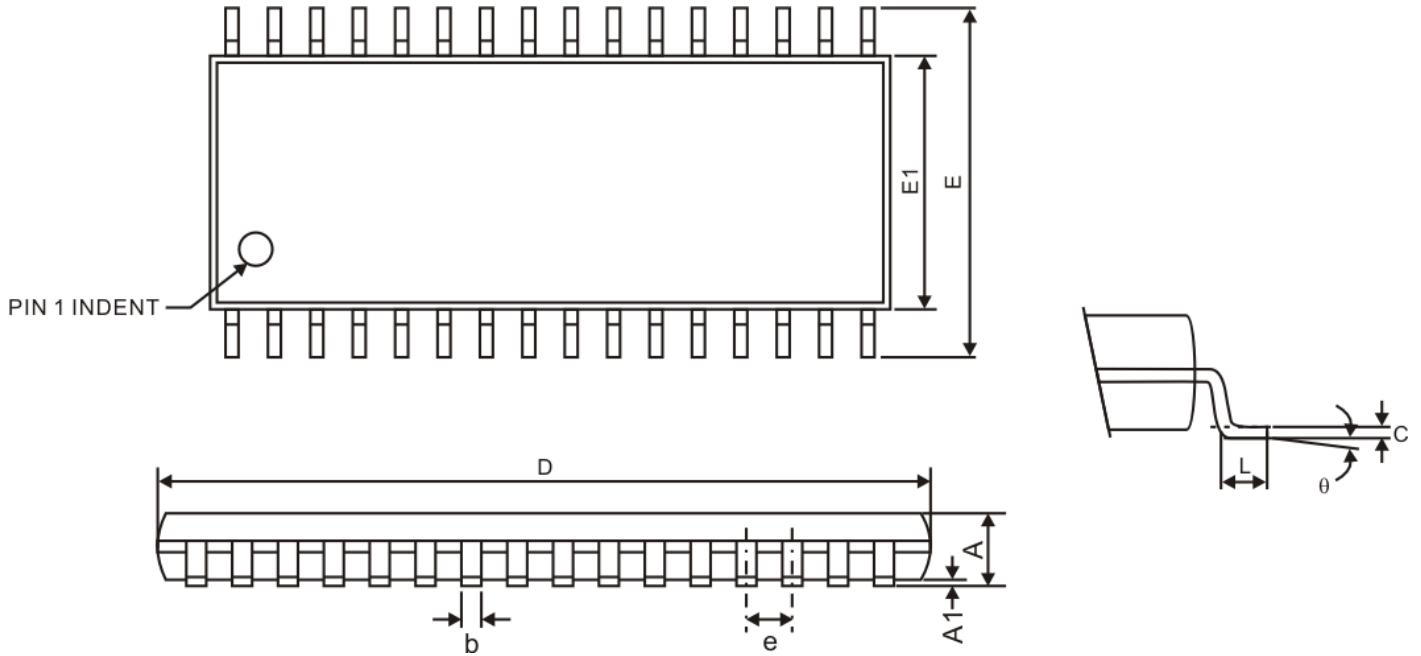
Symbol	Min.	Typ.	Max.
A	-	-	2.65
A1	0.10	-	-
b	0.31	-	0.51
c	0.20	-	0.33
e		1.27 BSC.	
D	20.32	-	20.73
E	7.40	-	7.60
E1	10.00	-	10.65
L	0.38	-	1.27
θ	0		8

Notes:
1. Refer to JEDEC MO-119 AC
2. Unit: mm

IMPORTANT NOTICE

Princeton Technology Corporation (PTC) reserves the right to make corrections, modifications, enhancements, improvements, and other changes to its products and to discontinue any product without notice at any time.

PTC cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a PTC product. No circuit patent licenses are implied.

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