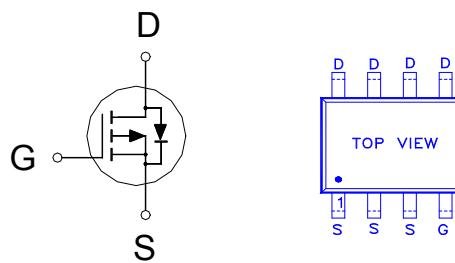


NIKO-SEM
**P-Channel Logic Level Enhancement Mode
Field Effect Transistor**
**PV555BA
SOP-8
Halogen-free & Lead-Free**
PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
-30V	28mΩ	-6A


G : GATE
D : DRAIN
S : SOURCE
ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current $T_A = 25^\circ\text{C}$	I_D	-6	A
$T_A = 70^\circ\text{C}$	I_D	-4.7	
Pulsed Drain Current ¹	I_{DM}	-24	
Avalanche Current	I_{AS}	-19.3	
Avalanche Energy	E_{AS}	18.6	mJ
Power Dissipation $T_A = 25^\circ\text{C}$	P_D	1.7	W
$T_A = 70^\circ\text{C}$	P_D	1.1	
Junction & Storage Temperature Range	T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient ²	$R_{\theta JA}$		72	°C / W

¹Pulse width limited by maximum junction temperature.²The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ\text{C}$.**ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ\text{C}$, Unless Otherwise Noted)**

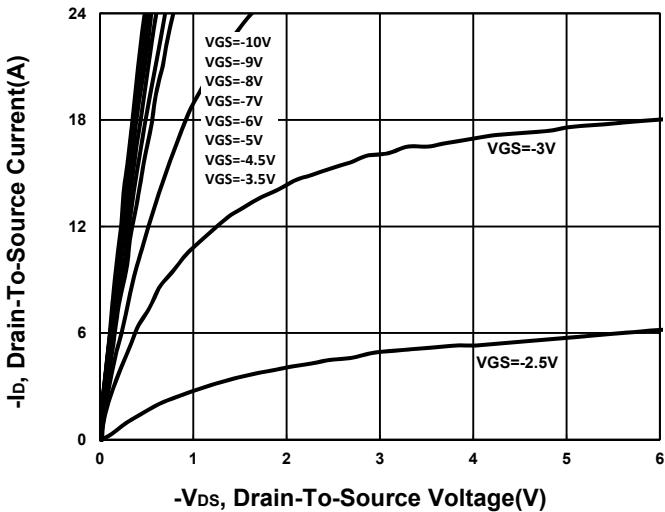
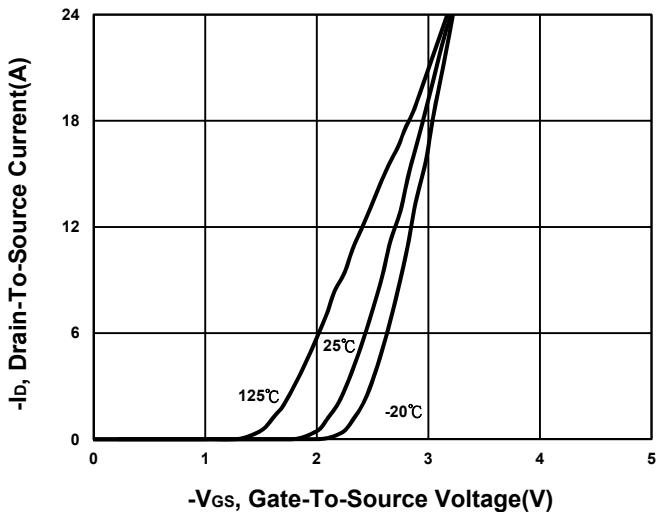
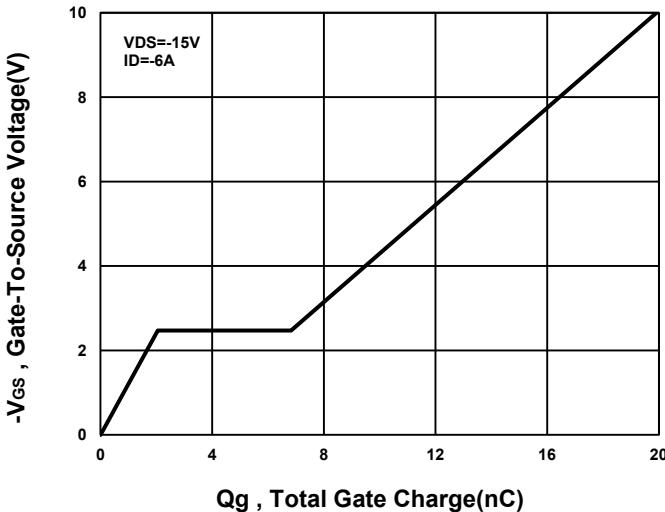
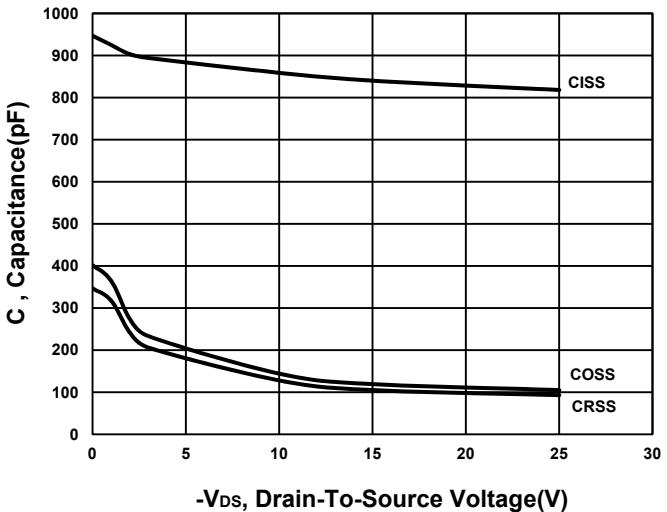
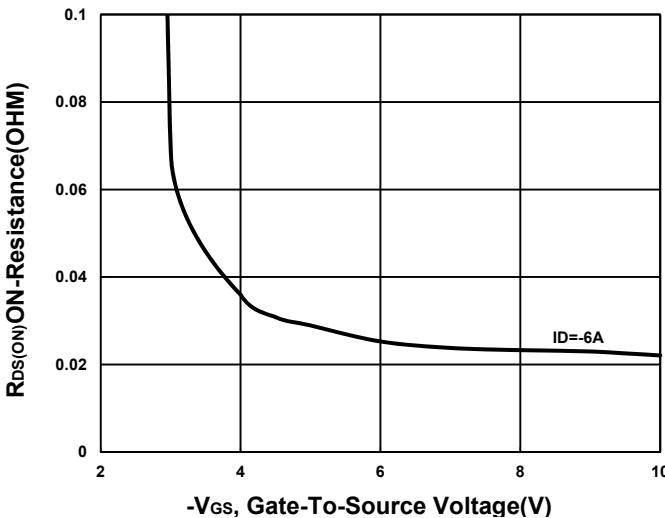
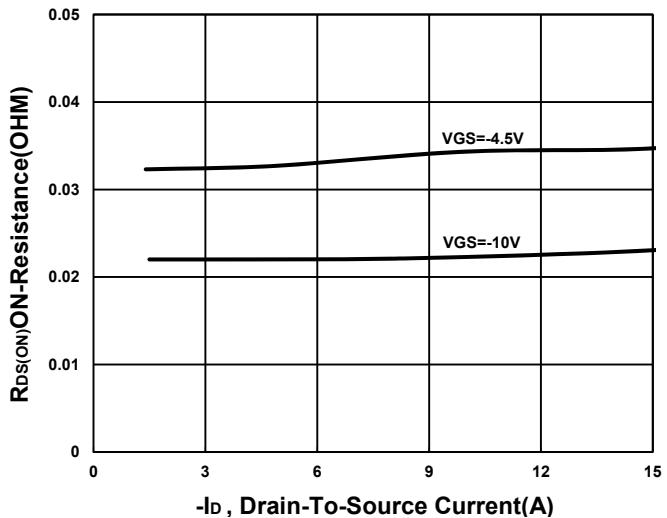
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu\text{A}$	-30			V
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$	-0.8	-1.5	-2.5	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -24V, V_{GS} = 0V$			-1	μA
		$V_{DS} = -20V, V_{GS} = 0V, T_j = 55^\circ\text{C}$			-10	

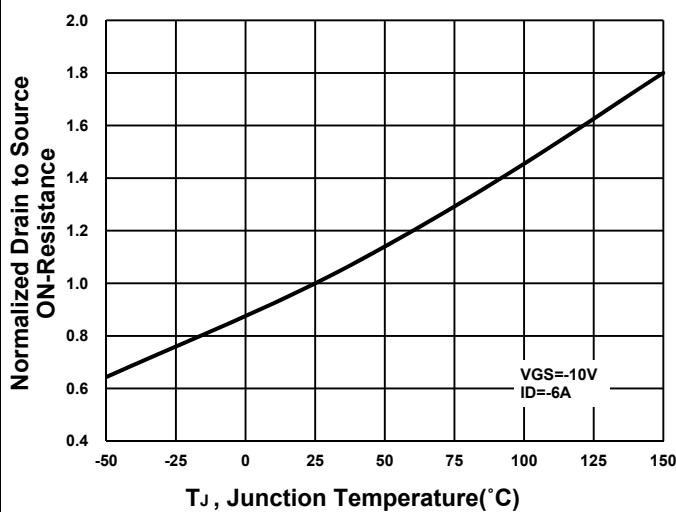
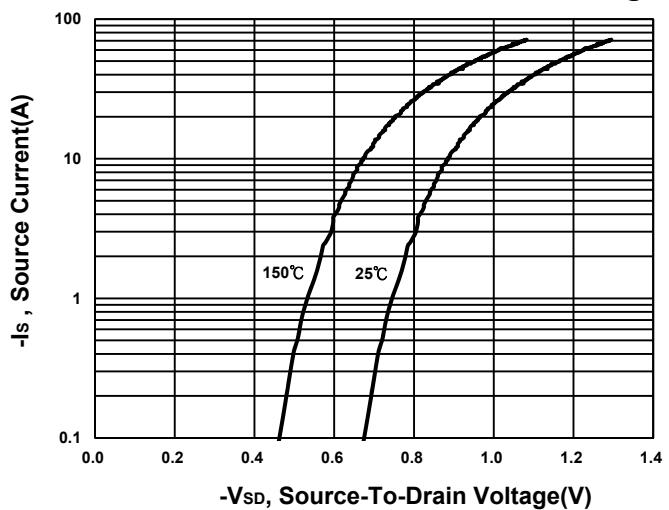
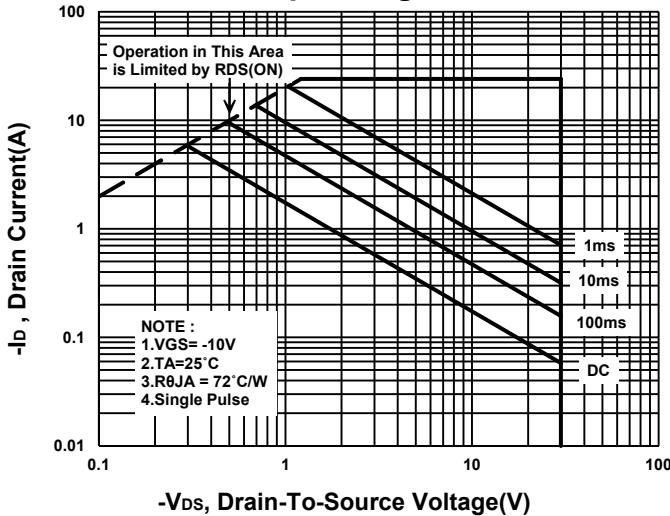
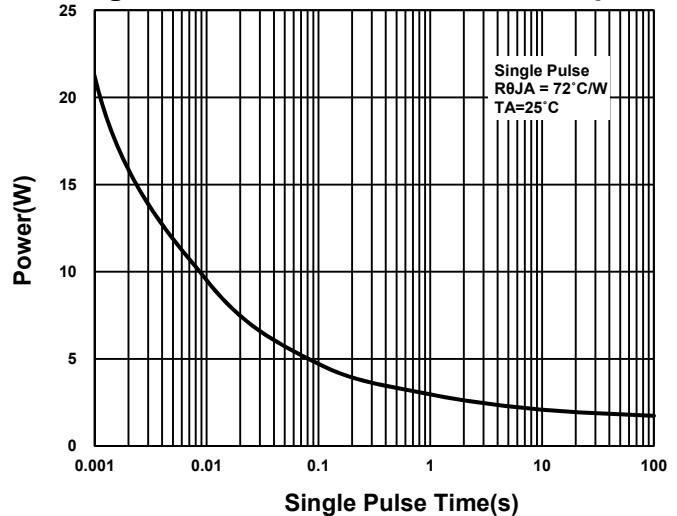
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**PV555BA
SOP-8
Halogen-free & Lead-Free**

Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = -4.5V, I_D = -6A$	32	45	$m\Omega$
		$V_{GS} = -10V, I_D = -6A$	22	28	
Forward Transconductance ¹	g_{fs}	$V_{DS} = -5V, I_D = -6A$	22		S

DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = -15V, f = 1MHz$	846			pF
Output Capacitance	C_{oss}		120			
Reverse Transfer Capacitance	C_{rss}		106			
Gate Resistance	R_g	$V_{GS} = 0V, V_{DS} = 0V, f = 1MHz$	11			Ω
Total Gate Charge ²	Q_g	$V_{DS} = -15V, V_{GS} = -10V, I_D = -6A$	20			nC
Gate-Source Charge ²	Q_{gs}		2.4			
Gate-Drain Charge ²	Q_{gd}		4.8			
Turn-On Delay Time ²	$t_{d(on)}$	$V_{DD} = -15V$ $I_D \geq -6A, V_{GS} = -10V, R_{GEN} = 6\Omega$	10.4			ns
Rise Time ²	t_r		7.8			
Turn-Off Delay Time ²	$t_{d(off)}$		22			
Fall Time ²	t_f		7			
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_J = 25^\circ C$)						
Continuous Current	I_S				-1.7	A
Forward Voltage ¹	V_{SD}	$I_F = -6A, V_{GS} = 0V$			-1	V
Reverse Recovery Time	t_{rr}	$I_F = -6A, dI/dt=100A/\mu s$			12.2	ns
Reverse Recovery Charge	Q_{rr}				3.5	nC

¹Pulse test : Pulse Width $\leq 300 \mu sec$, Duty Cycle $\leq 2\%$.²Independent of operating temperature.

NIKO-SEM**P-Channel Logic Level Enhancement Mode
Field Effect Transistor****PV555BA
SOP-8
Halogen-free & Lead-Free****Output Characteristics****Transfer Characteristics****Gate charge Characteristics****Capacitance Characteristic****On-Resistance VS Gate-To-Source****On-Resistance VS Drain Current**

NIKO-SEM
**P-Channel Logic Level Enhancement Mode
Field Effect Transistor**
**PV555BA
SOP-8
Halogen-free & Lead-Free**
On-Resistance VS Temperature**Source-Drain Diode Forward Voltage****Safe Operating Area****Single Pulse Maximum Power Dissipation****Transient Thermal Response Curve**