

# R2A15908SP

5 Input Selector 2ch Electronic Volume with Tone & Surround

REJ03F0270-0100 Rev.1.00 Jan 25, 2008

# Description

The R2A15908SP is an optimum audio signal processor IC for TV. It has a 5ch input selector with mono switch, surround, tone control (2band), input gain control and 2ch master volume. It can control all of these functions with  $I_2C$  bus.

# Features

- Volume 0 to -87dB, -∞ / 1dB step Each channel is independent control.
- 5 input selector + MUTE with mono switch
- Input gain control 0dB to +20dB / 2dB step
- Tone control Bass : -14dB to +14dB / 2dB step Treble : - 14dB to +14dB / 2dB step
- Surround Low / High
- Mode selector Bypass / Tone / Tone & Surround
- I<sub>2</sub>C-bus control
- Package SOP with 28 pin

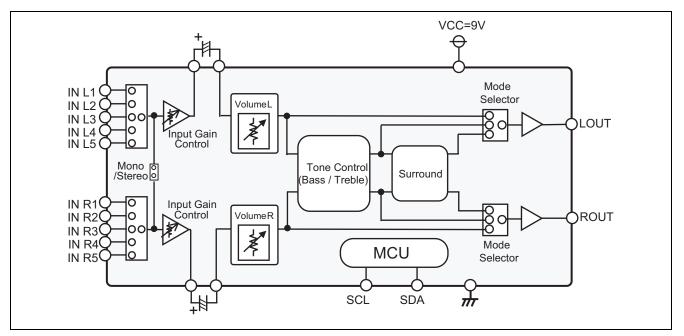
# Application

• Mini stereo, TV, etc.

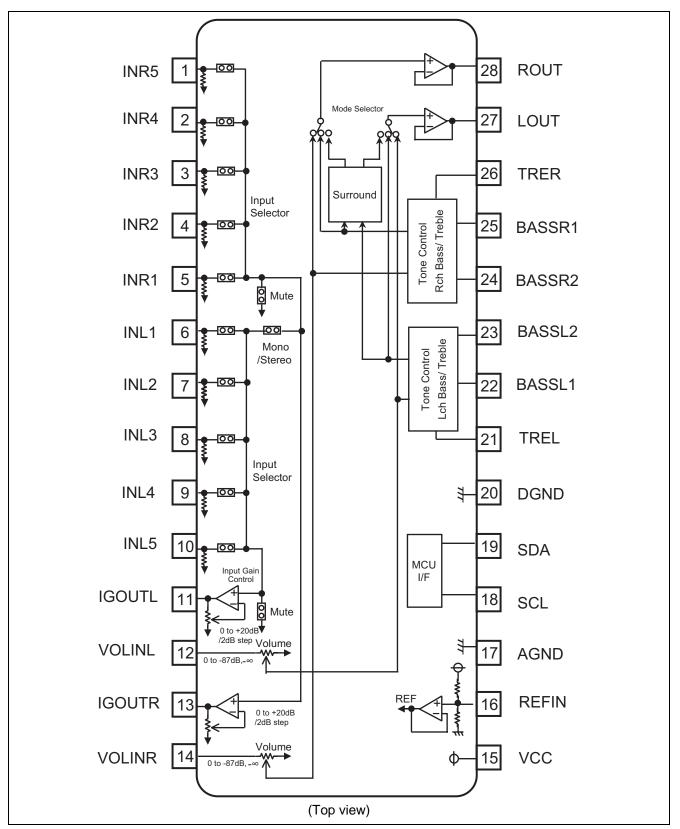
# **Recommended Operating Condition**

• Supply voltage .....  $V_{CC} = 9.0V$  (typ)

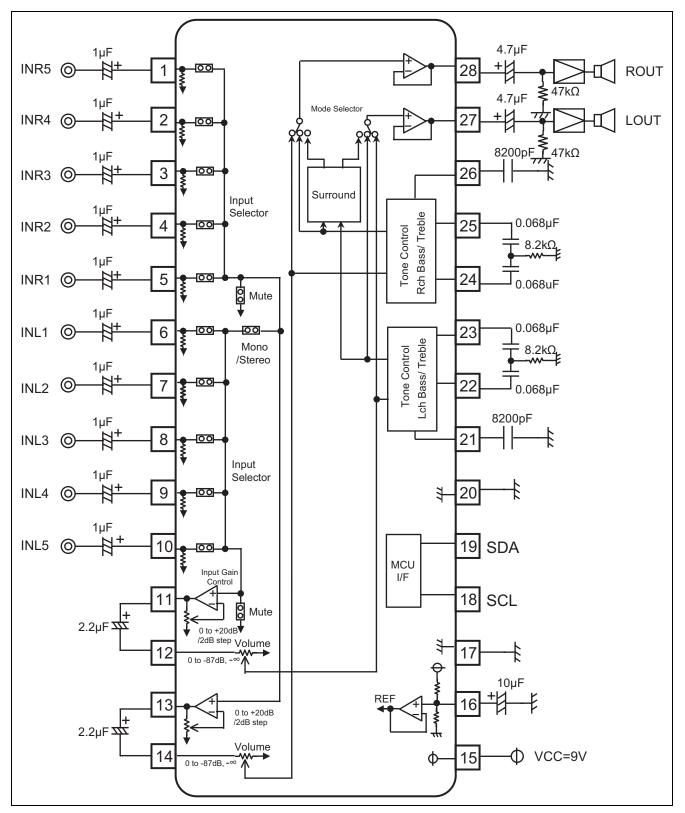
# **System Configuration**



# **Block Diagram and Pin Configuration**



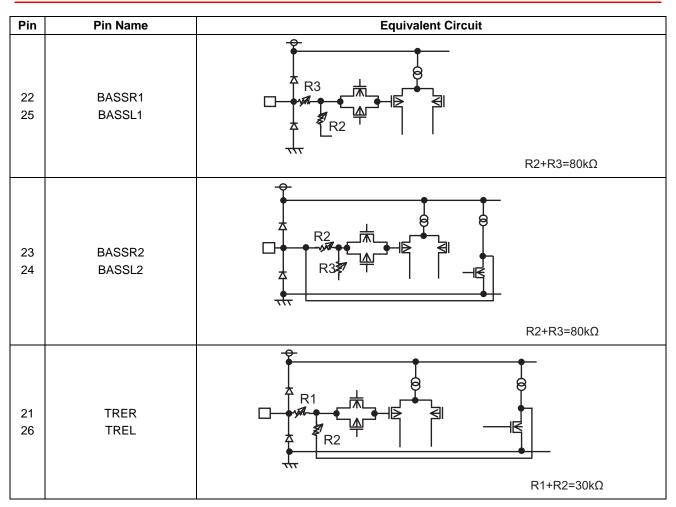
# **Application Example**



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# Equivalent Circuit of Pin Interface Block

Pin	Pin Name	Equivalent Circuit
1	INR5	
2	INR4	<del></del>
3	INR3	<b>∮</b>
4	INR2	
5	INR1	
6	INL1	
7	INL2	
8	INL3	4 ≸ 50k
9	INL4	+++ ref
9 10	INL4 INL5	
10	INLO	<u>^</u>
11 13 27 28	IGOUTL IGOUTR LOUT ROUT	
12 14	VOLINL VOLINR	$R_1$ $R_2$ $R_2$ $R_1$ $R_2$ $R_1$ $R_2$ $R_1$ $R_2$ $R_1$ $R_2$ $R_1$ $R_2$ $R_1$ $R_2$ $R_1$ $R_1$ $R_2$ $R_1$ $R_1$ $R_2$ $R_1$ $R_1$ $R_2$ $R_1$ $R_2$ $R_1$ $R_2$ $R_1$ $R_2$ $R_1$ $R_2$ $R_1$ $R_2$ $R_1$ $R_2$ $R_1$ $R_2$ $R_1$ $R_2$ $R_1$ $R_2$ $R_1$ $R_2$ $R_1$ $R_2$ $R_1$ $R_2$ $R_1$ $R_2$ $R_1$ $R_2$ $R_1$ $R_2$ $R_1$ $R_2$ $R_1$ $R_2$ $R_1$ $R_2$ $R_1$ $R_2$ $R_1$ $R_2$ $R_1$ $R_2$ $R_1$ $R_2$ $R_1$ $R_2$ $R_1$ $R_2$ $R_1$ $R_2$ $R_1$ $R_1$ $R_2$ $R_1$ $R_1$ $R_2$ $R_1$ $R_1$ $R_2$ $R_1$ $R_1$ $R_2$ $R_1$ $R_1$ $R_2$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_1$ $R_2$ $R_2$ $R_1$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_2$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$ $R_3$
18	SCL	
19	SDA	
16	REFIN	
15	VCC	
17	AGND	
20	DGND	



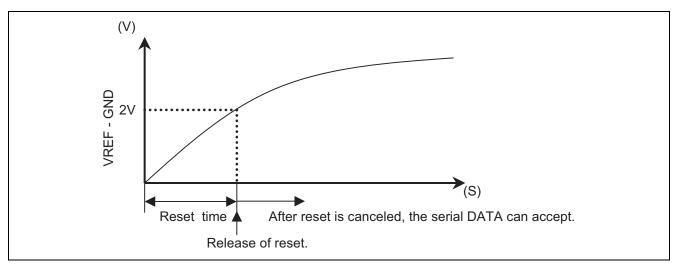
# Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Condition
Power supply	V <sub>cc</sub>	10	V	
Power dissipation	Pd		W	Ta ≤ 25°C
Thermal derating	K		mW / °C	Ta > 25°C (Circuit board installation)
Operating temperature	Topr	-20 to +75	°C	
Storage temperature	Tstg	-40 to +125	°C	

# **Power on Reset**

This IC built-in the power on reset function.

The voltage of VREF-GND less than 2V, the serial DATA can not accept.



# I<sub>2</sub>C Bus Format

	MSB LSB		MSB	LSB		MSB	LSB		
S	Slave Address	А	Sub Address		А	Data		А	Р
1 bit	8 bit	1 bit	8 bit		1 bit	8 bit		1 bit	1 bit

S: Starting Term

A: Acknowledge Bit

P: Stop Term

If more than one Data Byte is transmitted, then the significant SUB ADDRESS bits are auto incremented.  $00H\rightarrow 01H\rightarrow 02H\rightarrow 03H\rightarrow 04H\rightarrow 00H$ 

### 1. Slave Address

MSB							LSB
1	0	0	0	0	0	1	R/W <sub>B</sub>

 $R/W_B{=}0$  : Write mode for register setting  $R/W_B{=}1$  : Not available

### 2. Sub Address Table

Sub	BIT									
Address	D7	D7 D6 D5 D4 D3 D2 D1								
00H		<1>Lch Master volume								
01H			<1>F	Rch Master vo	lume			0		
02H	<	2>Input select	or		<3>Inp	out gain		0		
03H	<4>Stere	eo / Mono	<5>Mode	e selector	0	0	0	0		
04H	<6>Tone control Bass <6>Tone control Treble									

# 3. Data Table

# <1> Master Volume (Sub Address: 00H, 01H)

ATT	Lch	Sub	00H	D7	D6	D5	D4	D3	D2	D1
ATT	Rch	Address	01H	D7	D6	D5	D4	D3	D2	D1
0	dB			0	0	0	0	0	0	0
-1	dB			0	0	0	0	0	0	1
-2	2dB			0	0	0	0	0	1	0
-3	BdB			0	0	0	0	0	1	1
-4	ldB			0	0	0	0	1	0	0
-5	δdB			0	0	0	0	1	0	1
-6	бdВ			0	0	0	0	1	1	0
-7	′dB			0	0	0	0	1	1	1
-8	BdB			0	0	0	1	0	0	0
-9	)dB			0	0	0	1	0	0	1
-1	0dB			0	0	0	1	0	1	0
-1	1dB			0	0	0	1	0	1	1
-1:	2dB			0	0	0	1	1	0	0
-1	3dB			0	0	0	1	1	0	1
-1-	4dB	]		0	0	0	1	1	1	0
-1	5dB	]		0	0	0	1	1	1	1
-1	6dB	]		0	0	1	0	0	0	0
-1	7dB			0	0	1	0	0	0	1
-1	8dB			0	0	1	0	0	1	0
-1	9dB			0	0	1	0	0	1	1
-2	0dB			0	0	1	0	1	0	0
-2	1dB			0	0	1	0	1	0	1
-2	2dB			0	0	1	0	1	1	0
-2	3dB	l ab		0	0	1	0	1	1	1
-2-	4dB	– Lch Rch	Volume	0	0	1	1	0	0	0
-2	5dB	K CH		0	0	1	1	0	0	1
-2	6dB			0	0	1	1	0	1	0
-2	7dB			0	0	1	1	0	1	1
-2	8dB			0	0	1	1	1	0	0
-2	9dB			0	0	1	1	1	0	1
-3	0dB			0	0	1	1	1	1	0
-3	1dB			0	0	1	1	1	1	1
-3	2dB			0	1	0	0	0	0	0
-3	3dB			0	1	0	0	0	0	1
-3-	4dB	]		0	1	0	0	0	1	0
-3	5dB	]		0	1	0	0	0	1	1
-3	6dB	]		0	1	0	0	1	0	0
-3	7dB	]		0	1	0	0	1	0	1
-3	8dB	]		0	1	0	0	1	1	0
-3	9dB	]		0	1	0	0	1	1	1
-4	0dB	1		0	1	0	1	0	0	0
-4	1dB	1		0	1	0	1	0	0	1
-42	2dB	1		0	1	0	1	0	1	0
-4	3dB	1		0	1	0	1	0	1	1
-4-	4dB	1		0	1	0	1	1	0	0
-4	5dB	1		0	1	0	1	1	0	1
	6dB	1		0	1	0	1	1	1	0
	7dB	1		0	1	0	1	1	1	1
	8dB	1		0	1	1	0	0	0	0

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ATT	Lch	Sub	00H	D7	D6	D5	D4	D3	D2	D1
ATT	Rch	Address	01H	D7	D6	D5	D4	D3	D2	D1
-4	9dB			0	1	1	0	0	0	1
-5	0dB			0	1	1	0	0	1	0
-5	1dB			0	1	1	0	0	1	1
-5	2dB			0	1	1	0	1	0	0
-5	3dB			0	1	1	0	1	0	1
-5	4dB			0	1	1	0	1	1	0
-5	5dB			0	1	1	0	1	1	1
-5	6dB			0	1	1	1	0	0	0
-5	7dB			0	1	1	1	0	0	1
-5	8dB			0	1	1	1	0	1	0
-5	9dB			0	1	1	1	0	1	1
-6	0dB	1		0	1	1	1	1	0	0
-6	1dB	1		0	1	1	1	1	0	1
-6	2dB	1		0	1	1	1	1	1	0
-6	3dB			0	1	1	1	1	1	1
-6	4dB			1	0	0	0	0	0	0
-6	5dB		Lch	1	0	0	0	0	0	1
-6	6dB			1	0	0	0	0	1	0
-6	7dB			1	0	0	0	0	1	1
-6	8dB	L ch		1	0	0	0	1	0	0
-6	9dB	R ch	Volume	1	0	0	0	1	0	1
-7	0dB			1	0	0	0	1	1	0
-7	1dB			1	0	0	0	1	1	1
-7	2dB			1	0	0	1	0	0	0
-7	3dB			1	0	0	1	0	0	1
-7	4dB			1	0	0	1	0	1	0
-7	5dB			1	0	0	1	0	1	1
-7	6dB			1	0	0	1	1	0	0
-7	7dB			1	0	0	1	1	0	1
-7	8dB			1	0	0	1	1	1	0
-7	9dB			1	0	0	1	1	1	1
-8	0dB			1	0	1	0	0	0	0
-8	1dB	1		1	0	1	0	0	0	1
-8	2dB	1		1	0	1	0	0	1	0
-8	3dB	1		1	0	1	0	0	1	1
-8	4dB	1		1	0	1	0	1	0	0
-8	5dB	1		1	0	1	0	1	0	1
	6dB	1		1	0	1	0	1	1	0
	7dB	1		1	0	1	0	1	1	1
-	-∞	1		1	1	1	1	1	1	1

\* It's initial setting when power is turned on.

Setting	Input Selector						
Setting	D7	D6	D5				
IN1	0	0	0				
IN2	0	0	1				
IN3	0	1	0				
IN4	0	1	1				
IN5	1	0	0				
MUTE	1	1	1				

### <3> Input Gain (Sub Address: 02H)

Setting	Input Gain							
Setting	D4	D3	D2	D1				
0dB	0	0	0	0				
+2dB	0	0	0	1				
+4dB	0	0	1	0				
+6dB	0	0	1	1				
+8dB	0	1	0	0				
+10dB	0	1	0	1				
+12dB	0	1	1	0				
+14dB	0	1	1	1				
+16dB	1	0	0	0				
+18db	1	0	0	1				
+20dB	1	0	1	0				

# <4> Stereo / Mono Selector (Sub Address: 03H)

Setting	Mode Selector				
Setting	D7	D6			
Stereo	0	0			
Lch Mono	0	1			
Rch Mono	1	0			

### <5> Mode Selector (Sub Address: 03H)

Sotting	Mode Selector				
Setting	D5	D4			
Bypass	0	0			
Tone	0	1			
Tone & Surround Hi	1	0			
Tone & Surround Low	1	1			

\* It's initial setting when power is turned on.

# <6> Tone control (Sub Address: 04H)

Gain	Bass	D7	D6	D5	D4
Gain	Treble	D3	D2	D1	D0
OdB           2dB           4dB           6dB           8dB           10dB           12dB           14dB		A	0	0	0
			0	0	1
			0	1	0
			0	1	1
			1	0	0
			1	0	1
			1	1	0
			1	1	1

If A = 0 means Tone control gain CUT(-), then A = 1 means Tone control gain BOOST(+).

\* It's initial setting when power is turned on.

# **Electrical Characteristics**

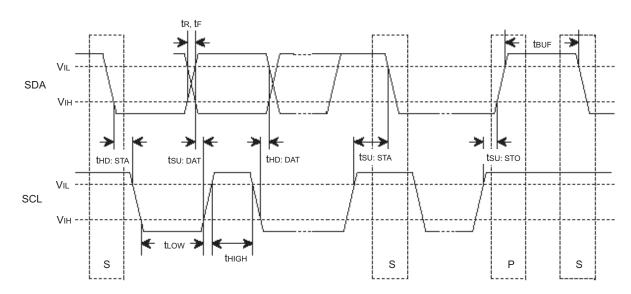
 $(V_{CC} = 9V, Ta = 25^{\circ}C, Vi = 100mVrms, f = 1kHz, Tone control = 0dB, Rg = 600\Omega, RL = 47k\Omega)$ 

#### **General Characteristics**

Parameter	Symbol	Limits		Unit	Condition			
Parameter	Symbol	Min	Typ Max		Unit	Condition		
Operational power supply	V <sub>CC</sub>	4.75	9.0	9.7	V			
Supply current	I <sub>CC</sub>		15	25	mA	No signal		
Reference voltage	Vref	4.0	4.5	5.0	V	No signal		
Input impedance	RIN	35	50	65	kΩ			
Maximum output voltage	VOM	_	2.5	—	Vrms	VOL = 0dB, THD = 1%		
Volume maximum	VOLmax	-2	0	+2	dB	VOL = 0dB		
Volume minimum	VOLmin	_	-100	-90	dB	VOL = Mute, Vin = 1Vrms, IHF-A		
Channel balance	CBAL	-1.5	0	1.5	dB	VOL = 0dB		
Total harmonic distortion	THD	_	0.01	0.5	%	400Hz to 30kHz BPF, Vo = 0.5Vrms		
Input selector cross talk	СТ	_	-100	-70	dB	400Hz to 30kHz BPF Vin = 1Vrms		
Channel separation	CS	_	-100	-70	dB	400Hz to 30kHz BPF Vin = 1Vrms		
Output noise 1	Vno1	_	30	50	μVrms	VOL = 0dB, Input gain = 0dB Tone = 0dB, Surround = Low, IHF-A		
Output noise 2	Vno2		5	15	μVrms	VOL = Mute, Input gain = 0dB Bypass, IHF-A		

### **Tone Control**

Parameter	Symbol	Limits			Unit	Condition	
Falameter	Symbol	Min	Тур	Max	Onit	Condition	
Tone control voltage gain (Boost/ Bass)	G(Bass)B	+11.5	+14	+16.5	dB	f = 100Hz, Bass = +14dB	
Tone control voltage gain (Cut/ Bass)	G(Bass)C	-16.5	-14	-11.5	dB	f = 100Hz, Bass = -14dB	
Tone control voltage gain (Flat/ Bass)	G(Bass)F	-2	0	+2	dB	f = 100Hz, Bass = 0dB	
Tone control voltage gain (Boost/ Treble)	G(Treble)B	+11.5	+14	+16.5	dB	f = 10kHz, Tre = +14dB	
Tone control voltage gain (Cut/ Treble)	G(Treble)C	-16.5	-14	-11.5	dB	f = 10kHz, Tre = $-14dB$	
Tone control voltage gain (Flat/ Treble)	G(Treble)F	-2	0	+2	dB	f = 100Hz, Tre = 0dB	



# **Bus Line Timing Specification**

Parameters	Symbol	Min	Max	Units
Min input low voltage	VIL	0	1.5	V
Max input high voltage	VIH	3.0	5.0	V
SCL clock frequency	f <sub>SCL</sub>	_	100	kHz
Time the bus must be free before a new transmission can start	t <sub>BUF</sub>	4.7	—	μS
Hold time start condition. After this period the first clock pulse is generated	t <sub>HDSTA</sub>	4.0	—	μS
The Low period of the clock	t <sub>Low</sub>	4.7	—	μS
The High period of the clock	t <sub>High</sub>	4.0	—	μS
Set-up time for start condition (Only relevant for a repeated start condition)	t <sub>SU: STA</sub>	4.7	—	μS
Hold time DATA	t <sub>HD: DAT</sub>	0	—	μS
Set-up time DATA	t <sub>SU: DAT</sub>	250	—	ns
Rise time of both SDA & SCL lines	t <sub>R</sub>	_	1000	ns
Fall time of both SDA & SCL lines	t <sub>F</sub>		300	ns
Set-up time for stop condition	t <sub>SU: STO</sub>	4.0	_	μS

# **Function Description**

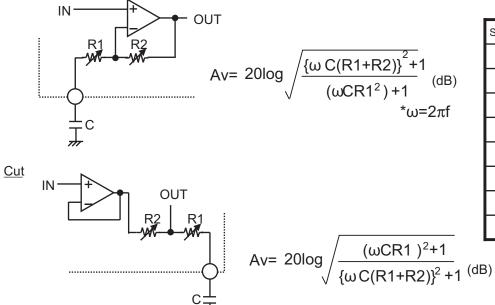
# 1. Tone Control

#### <1> Bass Circuit

		1			8.2kΩ =0.068µF
Boos		fo = $\frac{1}{2\pi \sqrt{R1(R2+R3)C1C2}}$ (Hz)	Setting [dB]	R2[Ω]	R3[Ω]
		• • • •	± 0	0	80000
		$Q \cong \frac{1}{C1+C2} \sqrt{\frac{C1C2R2}{R1}}  (R3=0)$	± 2	19820	60180
		(R2+R3	± 4	35570	44430
	·	$Gv = 20log\left(\frac{\frac{R2+R3}{R1}+2}{\frac{R3}{R1}+2}\right) (dB)$ (C1=C2)	± 6	48040	31920
	$ \begin{array}{c} \hline \\ \hline $	$\left[ \frac{R_3}{R_1} + 2 \right]$	± 8	58020	21980
		C 9 (C1=C2)	± 10	65910	14090
<u>Cut</u>	~	fo = (Hz)	± 12	72190	7810
		fo = $\frac{1}{2\pi\sqrt{R1(R2+R3)C1C2}}$ (Hz)	± 14	77170	2830
		$Q \cong \frac{1}{C1+C2} \sqrt{\frac{C1C2R2}{R1}}  (R3=0)$			
		$Gv = 20log\left(\frac{\frac{R3}{R1}+2}{\frac{R2+R3}{R1}+2}\right) (dB)$ (C1=C2)			

# <2> Treble Circuit

Boost



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		-
Setting [dB]	R1 [Ω]	R2 [Ω]
± 0	30000	0
± 2	23810	6190
± 4	18890	11110
± 6	14970	15030
± 8	11850	18150
± 10	9350	20650
± 12	7340	22660
± 14	5730	24270

\*ω=2πf

C=8200pF

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  Pines
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