

RMWB04001

4 GHz Buffer Amplifier MMIC

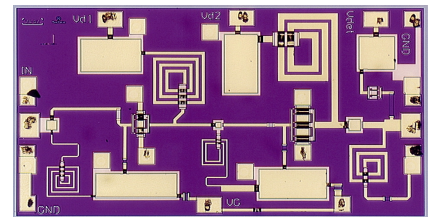
ADVANCED INFORMATION

Description

The RMWB04001 is a 2-stage GaAs MMIC amplifier designed as a 3.5 to 4 GHz Buffer Amplifier for use in the LO chain of millimeter wave point to point radios, point to multi-point communications, LMDS, and similar applications. In conjunction with other Raytheon amplifiers, multipliers and mixers it forms part of a complete 23 and 26 GHz transmit/receive chipset. The RMWB04001 utilizes Raytheon's 0.25µm power PHEMT process and can be used in a variety of applications requiring a high gain medium power amplifier.

Features

- ◆ 4 mil substrate
- ◆ Small-signal gain 27 dB (typ.)
- ◆ Saturated power out 20 dBm (typ.)
- ◆ Voltage detector included to monitor Pout
- ◆ Chip size 2.4 mm x 1.3 mm



Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|---|------------------|-------------|-------|
| Positive DC voltage (+4V Typical) | Vd | +6 | Volts |
| Negative DC voltage | Vg | -2 | Volts |
| Simultaneous (Vd - Vg) | Vdg | 8 | Volts |
| Positive DC Current | I _D | 168 | mA |
| RF Input Power (from 50 Ω source) | P _{IN} | +7 | dBm |
| Operating Baseplate Temperature | T _C | -30 to +85 | °C |
| Storage Temperature Range | T _{stg} | -55 to +125 | °C |
| Thermal Resistance (Channel to backside) | R _{jc} | 140 | °C/W |

Electrical Characteristics

(At 25°C), 50 Ω system, Vd=+4 V, Quiescent Current Idq=36 mA

| Parameter | Min | Typ | Max | Unit |
|---------------------------------------|-----|------|-----|------|
| Frequency Range | 3.5 | | 4.0 | GHz |
| Gate Supply Voltage (Vg) ¹ | | -0.7 | | V |
| Gain (Small Signal at Pin= -12 dBm) | 24 | 27 | | dB |
| Gain Variation Vs. Frequency | | 0.5 | | dB |
| Power Output Saturated: (Pin=-2 dBm) | 18 | 20 | | dBm |
| Input Return Loss (Pin=-12 dBm) | | -14 | | dB |
| Output Return Loss (Pin=-12 dBm) | | -12 | | dB |
| DC detector voltage at Pout=20 dBm | | 0.5 | | V |

Application Information

CAUTION: THIS IS AN ESD SENSITIVE DEVICE.

Chip carrier material should be selected to have GaAs compatible thermal coefficient of expansion and high thermal conductivity such as copper molybdenum or copper tungsten. The chip carrier should be machined, finished flat, plated with gold over nickel and should be capable of withstanding 325°C for 15 minutes.

Die attachment should utilize Gold/Tin (80/20) eutectic alloy solder and should avoid hydrogen environment for PHEMT devices. Note that the backside of the chip is gold plated and is used as RF and DC ground.

These GaAs devices should be handled with care and stored in dry nitrogen environment to prevent contamination of bonding surfaces. These are ESD sensitive devices and should be handled with appropriate precaution including the use of wrist grounding straps. All die attach and wire/ribbon bond equipment must be well grounded to prevent static discharges through the device.

Recommended wire bonding uses 3 mils wide and 0.5 mil thick gold ribbon with lengths as short as practical allowing for appropriate stress relief. The RF input and output bonds should be typically 0.012" long corresponding to a typically 2 mil between the chip and the substrate material.

Note: 1. Typical range of gate voltage is -1 to -0.4 V to set Idq of 36 mA.

Characteristic performance data and specifications are subject to change without notice.

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Recommended Procedure
for Biasing and Operation

CAUTION: THIS IS AN ESD SENSITIVE DEVICE.

CAUTION: LOSS OF GATE VOLTAGE (VG) WHILE DRAIN VOLTAGE (VD) IS PRESENT MAY DAMAGE THE AMPLIFIER CHIP.

The following sequence of steps must be followed to properly test the amplifier:

Step 1: Turn off RF input power.

Step 2: Connect the DC supply grounds to the grounds of the chip carrier.

Slowly apply negative gate bias supply voltage of -1.5 V to Vg.

Step 3: Slowly apply positive drain bias supply voltage of +4 V to Vd.

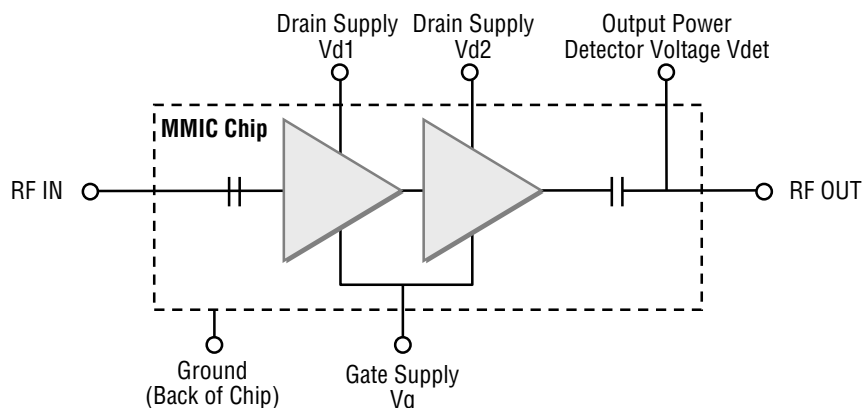
Step 4: Adjust gate bias voltage to set the quiescent current of $I_{dq}=36$ mA.

Step 5: After the bias condition is established, RF input signal may now be applied at the appropriate frequency band.

Step 6: Follow turn-off sequence of:

- (i) Turn off RF input power
- (ii) Turn down and off drain voltage (Vd)
- (iii) Turn down and off gate bias voltage (Vg)

Functional Block Diagram

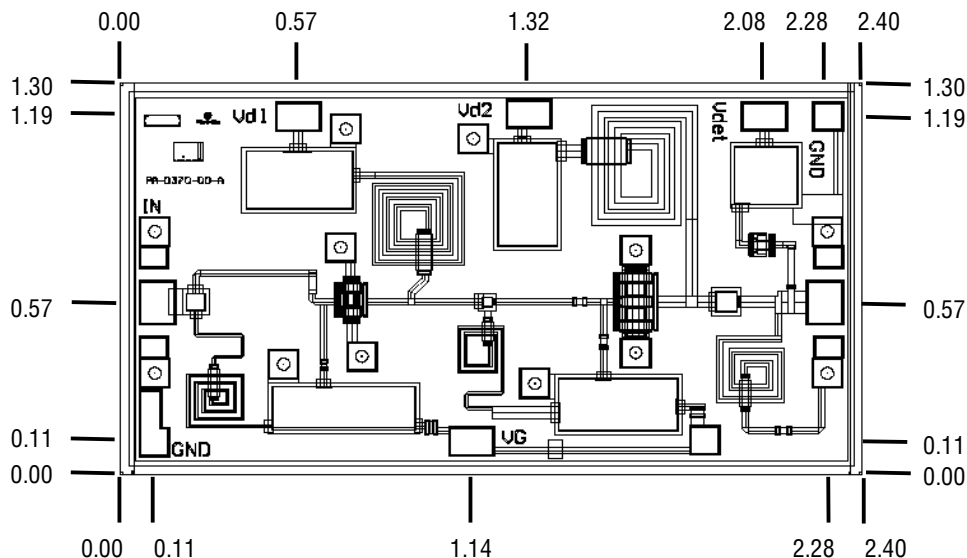


Note: Detector delivers > 0.1V DC into 3kΩ load resistor for >20 dBm output power. If output power level detection is not desired, do not connect to detector bond pad.

Figure 1

Chip Layout and Bond Pad Locations
Chip Size is 2.40 mm x 1.30 mm. X 100 μm.
Back of chip is RF and DC ground

Dimensions in mm



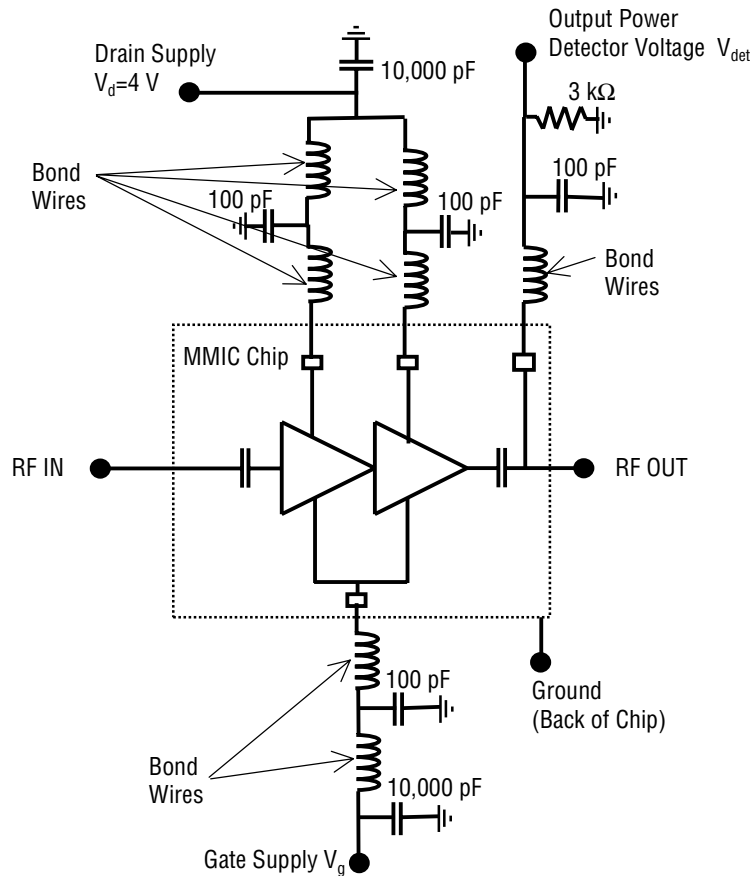
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4 GHz Buffer Amplifier MMIC

Figure 2

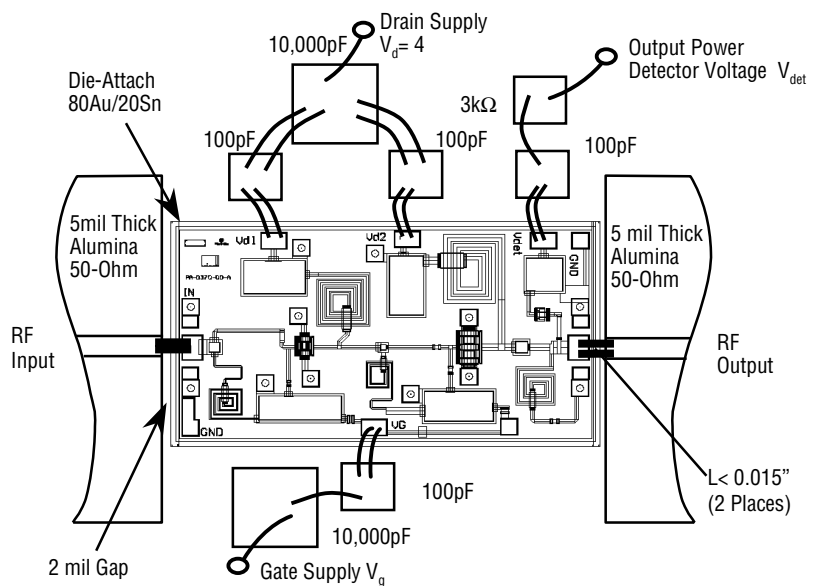
Recommended Application Schematic Circuit Diagram



Note: Detector delivers > 0.1V DC into 3kΩ load resistor for >20dBm output power. If output power level detection is not desired, do not connect to detector bond pad.

Figure 3

Recommended Assembly Diagram



Note: Use 0.003" by 0.0005" Gold Ribbon for bonding. RF input and output bonds should be less than 0.015" long with stress relief.

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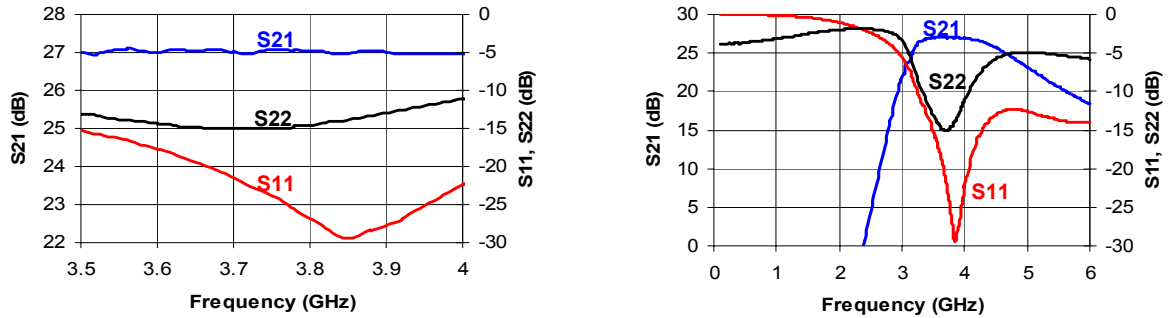
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4 GHz Buffer Amplifier MMIC

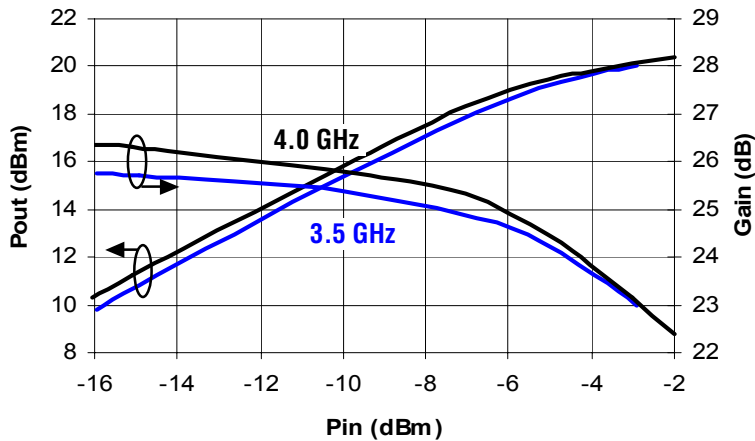
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Performance Data

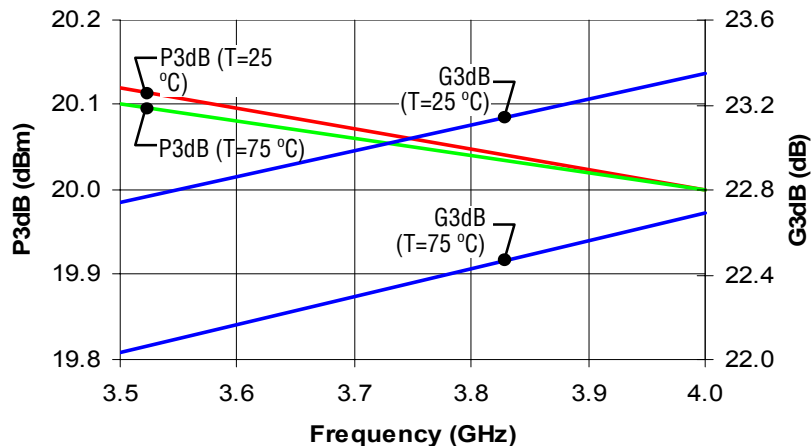
Typical Small Signal Performance
On-Wafer Measurements, $V_d=4\text{ V}$, $I_{dq}=36\text{ mA}$, $T=25\text{ }^\circ\text{C}$



Power Output and Gain Vs. Power In
50 Ω Fixture Measurements, $V_d=4\text{ V}$, $I_{dq}=36\text{ mA}$, $T=25\text{ }^\circ\text{C}$



Power Output and Gain at 3 dB Compression Vs. Frequency and Temperature
50 Ω Fixture Measurements, $V_d=4\text{ V}$, $I_{dq}=36\text{ mA}$



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