Two Phase General Purpose PWM Controller

General Description

The RT8805 is the most compact dual-phase synchronous buck controller in the industry specifically designed for high power density applications. This part is capable of delivering up to 60A output current due to its embedded bootstrapped drivers that support 12V + 12V driving capability.

The phase currents are sensed by innovative time sharing $R_{DS(ON)}$ current sensing technique for current balance and over current balance. Using one common GM amplifier to sense two phase currents eliminates offset and nonlinearity of the GM amplifier and yields good current balance. Other features include adjustable operation frequency from 50kHz to 1MHz, adjustable soft-start, PGOOD, external compensation, enable/shutdown for various application and performance consideration.

The RT8805 comes to a tiny footprint package of VQFN-16L 3x3 package that is capable of dissipating up to 1.47W heat.

Ordering Information

RT8805 □ □

Package Type
QV : VQFN-16L 3x3 (V-Type)

Operating Temperature Range
P : Pb Free with Commercial Standard

Note :

RichTek Pb-free products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.
- 100% matte tin (Sn) plating.

Marking Information

For marking information, contact our sales representative directly or through a RichTek distributor located in your area, otherwise visit our website for detail.

Features

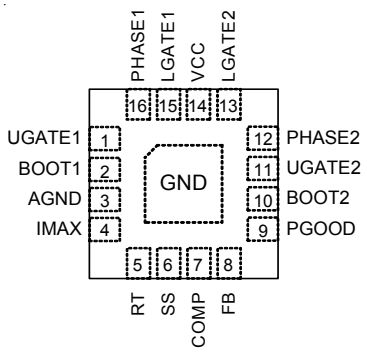
- **12V Power Supply Voltage**
- **2 Phase Power Conversion**
- **Embedded 12V Boot Strapped Driver**
- **Precise Core Voltage Regulation**
- **Low Side MOSFET $R_{DS(ON)}$ Current Sensing for Power Stage Current Balance**
- **External Compensation**
- **Adjustable Soft-Start**
- **Adjustable Frequency and Typical at 300kHz Per Phase**
- **Power Good Indication**
- **Adjustable Over Current Protection**
- **Small 16-Lead VQFN Package**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Applications

- Middle-High End GPU Core Power
- High End Desktop PC Memory Core Power
- Low Output Voltage, High Power Density DC-DC Converters
- Voltage Regulator Modules

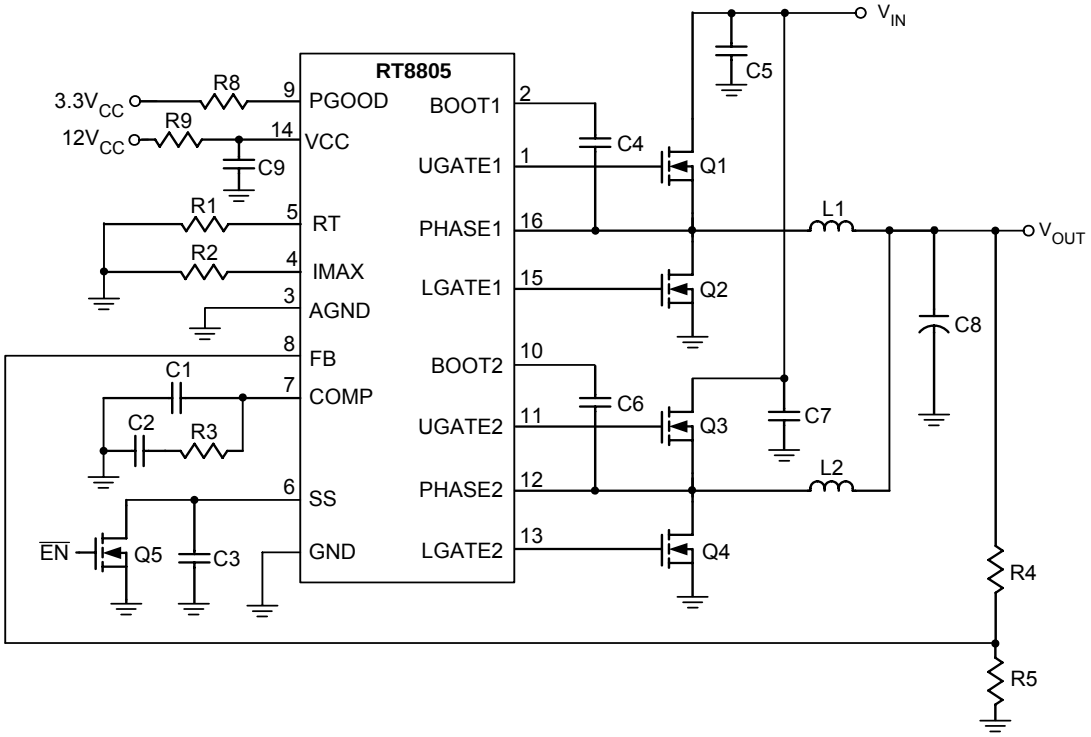
Pin Configurations

(TOP VIEW)

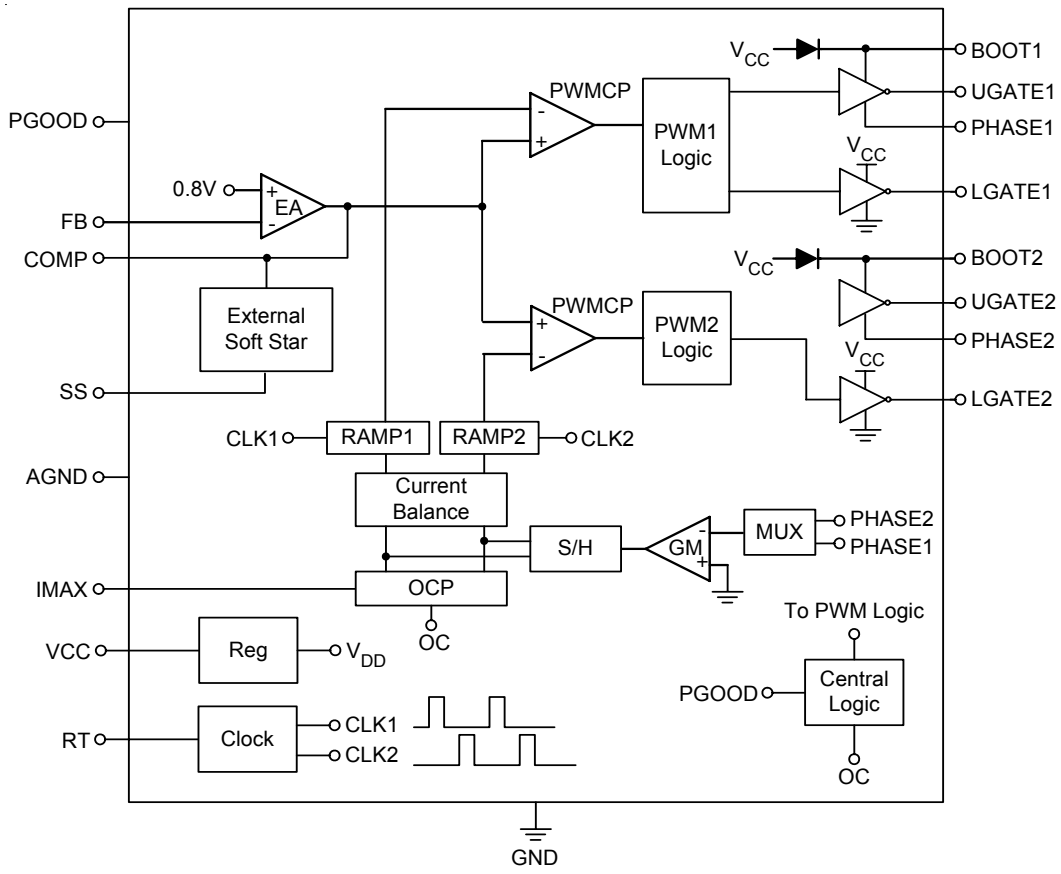


VQFN-16L 3x3

Typical Application Circuit



Function Block Diagram



Functional Pin Description

UGATE1 (Pin 1), UGATE2 (Pin 11)

Upper Gate Drive. These pins drive the gates of the highside MOSFETs.

BOOT1 (Pin 2), BOOT2 (Pin 10)

Bootstrap Power Pin. These pins power the high-side MOSFET drivers. Connect These pins to the junctions of the bootstrap capacitors.

AGND (Pin 3)

Chip Analog Ground.

IMAX (Pin 4)

Maximum Current Setting. This pin sets the current limiting level. Connect this pin with resistor to ground to set the current limit.

RT (Pin 5)

Timing Resistor. Connect a resistor from RT to AGND to set the clock frequency.

SS (Pin 6)

Soft-Start Pin. This pin provides soft-start function for controller. The COMP voltage of the converter follows the ramping voltage on the SS pin.

COMP (Pin 7)

Compensation Pin. This pin is output node of the error amplifier.

FB (Pin 8)

Feedback Pin. This pin is negative input pin of the error amplifier.

PGOOD (Pin 9)

Power Good. PGOOD is an open drain output used to indicate the status of the voltages on SS pin and FB pin. PGOOD will go high impedance when SS > 3.7V and FB > 0.6V.

LGATE1 (Pin 15), LGATE2 (Pin 13)

Lower Gate Drive. These pins drive the gate of the lowside MOSFETs.

PHASE1 (Pin 16), PHASE2 (Pin 12)

These pins are return nodes of the high-side driver. Connect These pins to high-side MOSFET sources together with the low-side MOSFET drains and the inductors.

VCC (Pin 14)

The VCC pin is the external 12V power. Internal 5V power (V_{DD}) is regulated from this pin. This pin also powers the low side MOSFETS drivers.

GND (Exposed Pad)

Exposed pad should be soldered to PCB board and connected to GND.

Absolute Maximum Ratings (Note 1)

- Supply Voltage, V_{CC} ---------- –0.3V to 16V
- PHASE to GND
  DC ---------- –5V to 15V
  < 200ns ---------- –10V to 30V
- BOOT to PHASE ---------- 15V
- BOOT to GND
  DC ---------- –0.3V to V_{CC}+15V
  < 200ns ---------- –0.3V to 42V
- Input, Output or I/O Voltage ---------- GND-0.3V to 7V
- Power Dissipation, P_D @ T_A = 25°C
  VQFN–16L 3x3 ---------- 1.47W
- Package Thermal Resistance (Note 4)
  VQFN–16L 3x3, θ_{JA} ---------- 68°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- ESD Susceptibility (Note 2)
  HBM (Human Body Mode) ---------- 1.5kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 3)

- Supply Voltage ---------- 9V to 14V
- Junction Temperature Range ---------- –20°C to 70°C

Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input						
Power Supply Voltage	V_{CC}		--	12	15	V
Power On Reset	V_{CC}		5.4	5.9	6.5	V
Power On Reset Hysteresis			--	0.3	--	V
Power Supply Current	I_{VCC}	V_{SS} = 0V	--	10	--	mA
Soft Start						
Soft Start Current	I_{SS}		8	10	15	μA
Oscillator						
Free Running Frequency	f_{OSC}	RT = 33kΩ	255	300	345	kHz
Frequency Variation			-15	--	15	%
Frequency Range			50	300	1000	kHz
Maximum Duty Cycle			70	75	80	%

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Reference Voltage						
Feedback Voltage	V_{FB}	V_{FB} = 0.8V	0.784	0.8	0.816	V
Error Amplifier						
DC Gain			60	70	--	dB
Gain-Bandwidth Product	GBW	C_{LOAD} = 5pF	6	10	--	MHz
Trans-conductance	GM	R_{LOAD} = 20kΩ	600	660	--	μA/V
MAX Current (Source & Sink)	I_{COMP}	V_{COMP} = 2.5V	300	360	--	μA
Current Sense GM Amplifier						
OC	V_{PHASE}	R_{IMAX} = 33kΩ	--	-220	--	mV
Gate Driver						
Maximum Upper Drive Source	$I_{UGATE(MAX)}$	BOOT – PHASE = 12V	1	--	--	A
Upper Drive Sink	R_{UGATE}	V_{UGATE} = 1V	--	3.5	7	Ω
Maximum Lower Drive Source	$I_{LGATE(MAX)}$	PV_{CC} = 12V	1	--	--	A
Lower Drive Sink	R_{LGATE}	V_{LGATE} = 1V	--	2	4	Ω
Protection						
Under Voltage Protection			0.55	0.6	0.65	V
Power Sequence						
Power Good Threshold			3.4	3.7	4	V
Power Good Sink Capability (4mA)			--	0.05	0.2	V

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

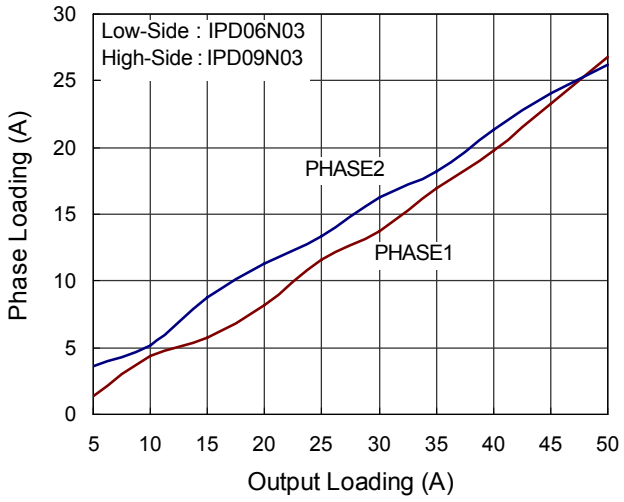
Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. The device is not guaranteed to function outside its operating conditions.

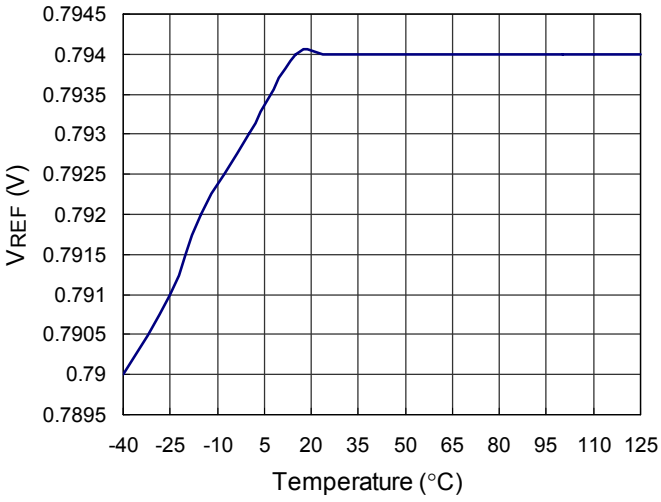
Note 4. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Typical Operating Characteristics

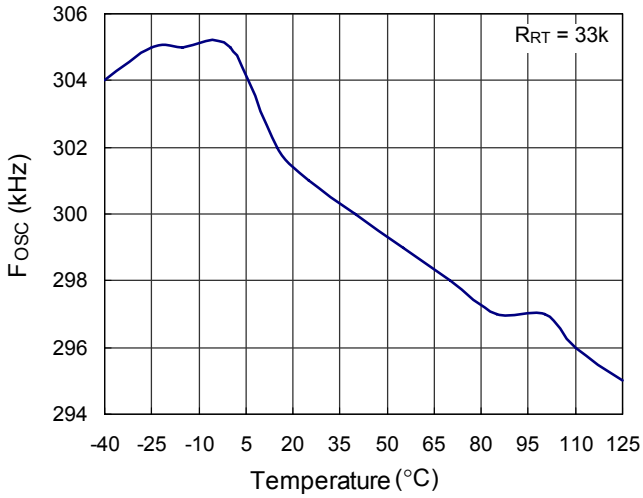
Phase Loading vs. Output Loading



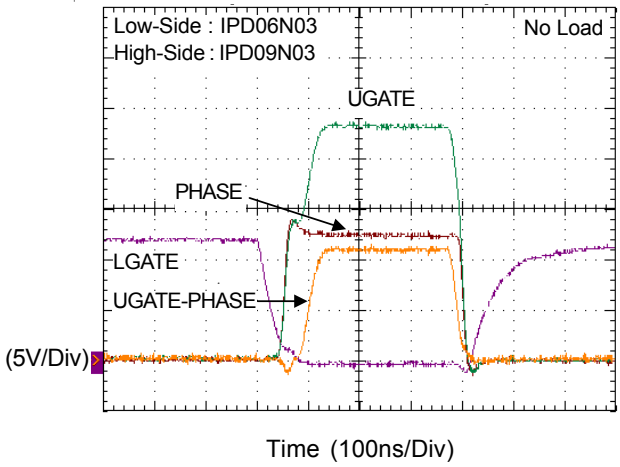
V_{REF} vs. Temperature



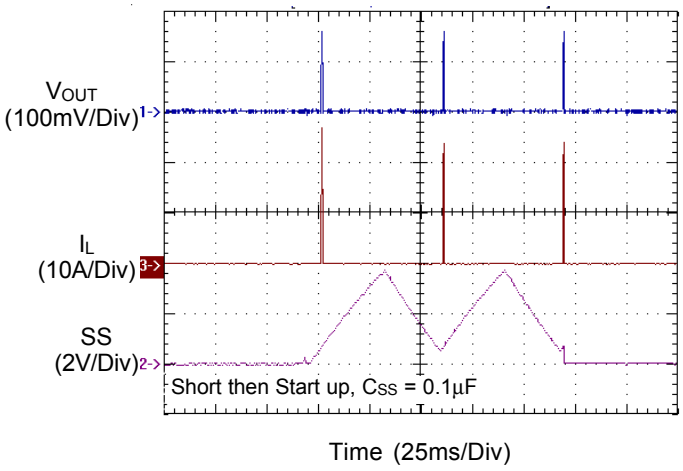
F_{OSC} vs. Temperature



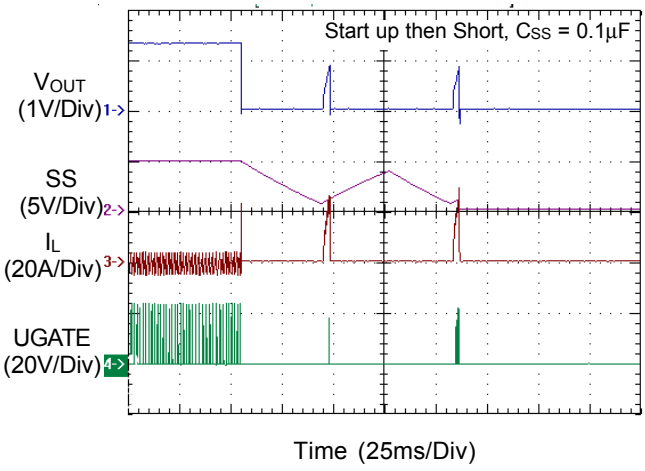
Dead Time



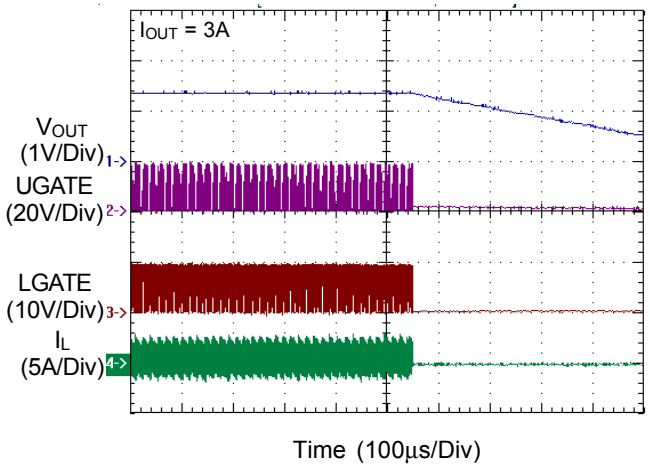
OCP



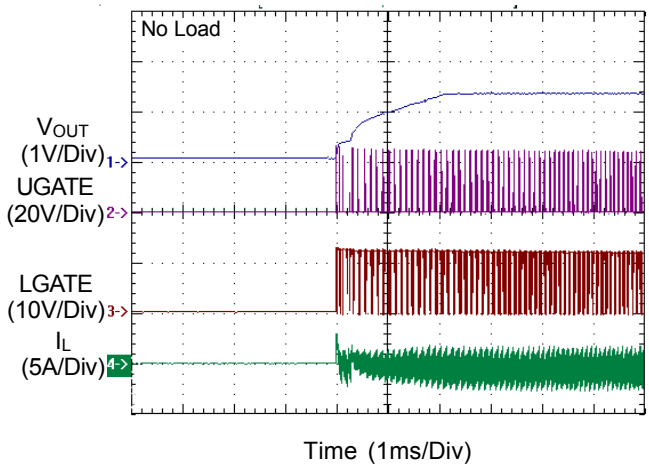
OCP



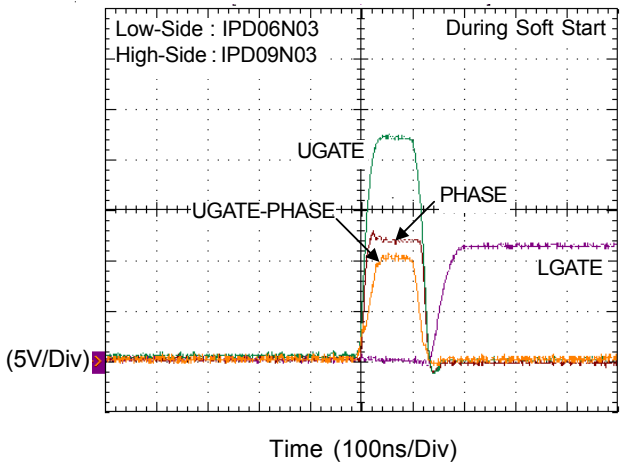
Power Off



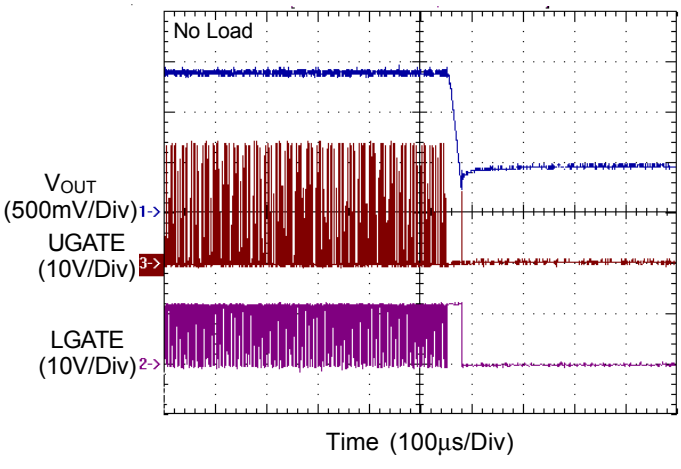
Power On



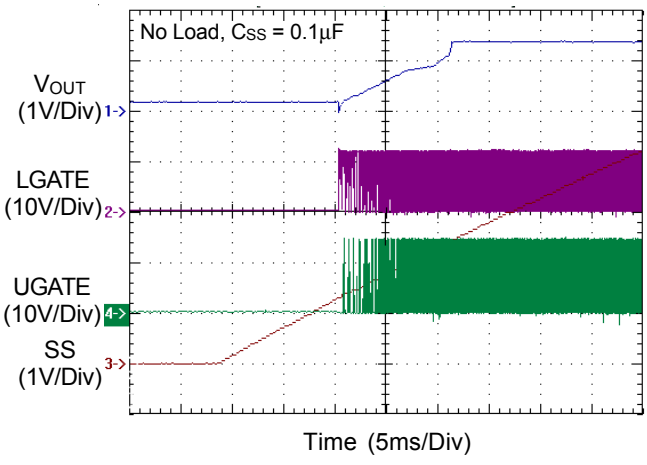
Short Pulse



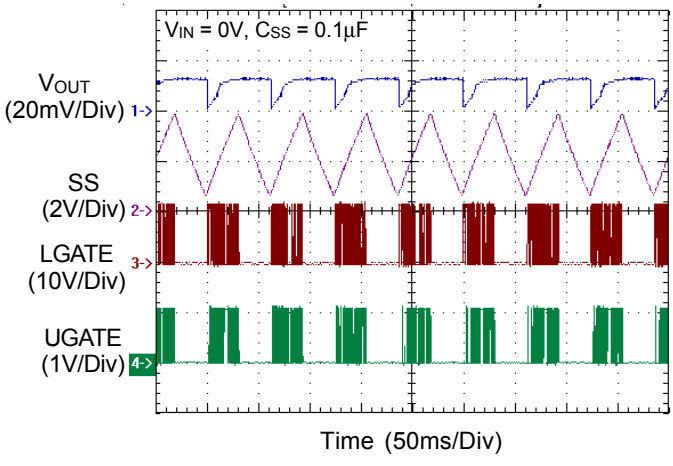
Shutdown by SS Pin



Start Up by SS Pin



UVP



Applications Information

Power On Reset

RT8805 operates with input voltage at VCC pin ranging from 5.9V to 15V. An internal linear regulator regulates the input voltage to 5V for internal control circuit use. The POR (power on reset) circuitry monitors the supply voltage to make sure the supply voltage is high enough for RT8805 normal work. When the regulated power exceeds 4.2V typically, the RT8805 releases the reset state and works according to the setting. Once the regulated voltage is lower than 4.0V, POR circuitry resets the chip. Hysteresis between the rising and falling thresholds assure that once enabled, the RT8805 will not inadvertently turn off unless the bias voltage drops substantially (see *Electrical Specifications*).

Enable, Soft Start and Power Good

Once POR releases, the RT8805 begins its soft start cycle as shown in Figure 1. A 10μA source current charges the capacitor C_{SS} connected to SS to control the soft start behavior of RT8805. During soft start, SS voltage increases linearly and clamps the error amplifier output. Duty cycle and output voltage increase accordingly. The soft start limits inrush current from input capacitors.

The RT8805 regards SS pin voltage higher than 3.7V as the end of soft start cycle. Then RT8805 trip PGOOD to high impedance if no fault occurs indicating power good. The SS pin also act as the timer during OCP and UVP hiccup as described in the later sections.

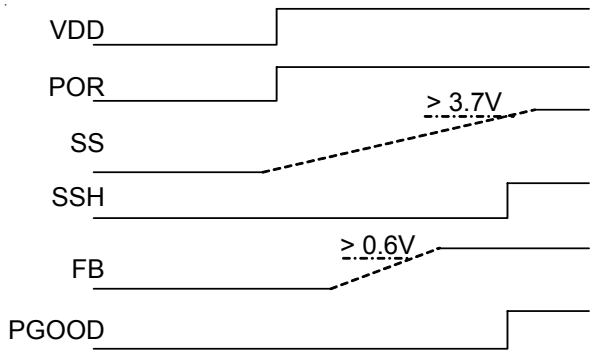


Figure 1. Power Sequence

Frequency setting

The converter switching frequency is programmed by connecting a resistor from the RT pin to GND. Figure 2 illustrates switching frequency vs. R_{RT}.

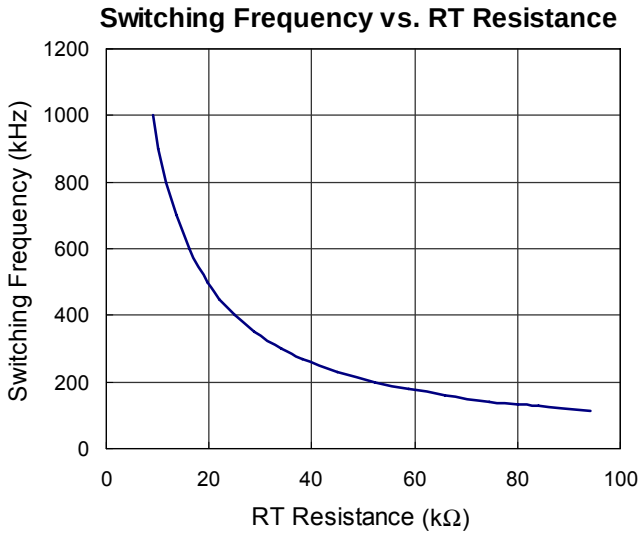


Figure 2. Switching Frequency vs. R_{RT}.

Voltage Control

The voltage control loop consists of error amplifier, multiphase pulse width modulator, drivers and power components. As conventional voltage mode PWM controller, the output voltage is locked at the positive input of error amplifier and the error signal is used as the control signal of pulse width modulator. The PWM signals of different channels are generated by comparison of EA output and split-phase sawtooth wave. Power stage transforms V_{IN} to output by PWM signal on-time ratio.

Current Sensing Setting

RT8805 senses the current of low side MOSFET in each synchronous rectifier when it is conducting for channel current balance and OCP detecting. The multiplexer and sensing GM amplifier converts the voltage on the sense component (can be a sense resistor or the $R_{DS(ON)}$ of the low side MOSFET) to current signal into internal circuit (see Figure 3).

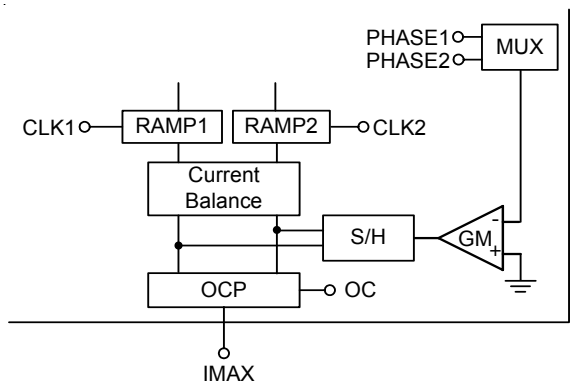


Figure 3. Current Sensing Loop

The sensing circuit gets $I_X = I_{L(S/H)} \times R_{DS(ON)} \times GM$ by local feedback. I_X is sampled and held just before low side MOSFET turns off (See Figure 4). Therefore,

$$I_{X(S/H)} = I_{L(S/H)} \times R_{DS(ON)} \times GM$$

$$I_{L(S/H)} = I_{L(AVG)} - \frac{V_{OUT}}{L} \times \frac{T_{OFF}}{2},$$

$$T_{OFF} = \left[\frac{V_{IN} - V_{OUT}}{V_{IN}}\right] \times 5\mu s,$$

$$F_{SW} = 200kHz$$

$$I_{X(S/H)} = \left[I_{L(AVG)} - \frac{V_{OUT} \times \left(\frac{V_{IN} - V_{OUT}}{V_{IN}}\right) \times 5\mu s}{2L}\right] \times R_{DS(ON)} \times GM$$

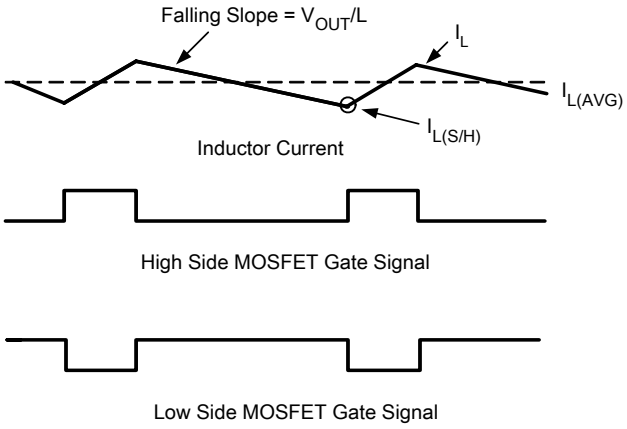


Figure 4. Inductor Current and Gate signals

Current Balance

RT8805 senses the voltage drop of the low-side MOS and translates this to control the ramp signal. We can see that the voltage signal finally injected to channel one is proportional to (I_{L1} - I_{L2}). Channel two is proportional to (I_{L2} - I_{L1}). In steady state and current balance situation, there is no sensed signal injected into the ramp.

If $I_{L1} > I_{L2}$, the ramp bottom of channel 1 will be lifted up and decreased the duty of UGATE1. On the other hand, the ramp bottom of channel 2 will be pulled low to increase the duty of UGATE2. Finally, the loop will be back to the balance state through above mentioned negative feedback scheme. Figure 5 shows this scheme.

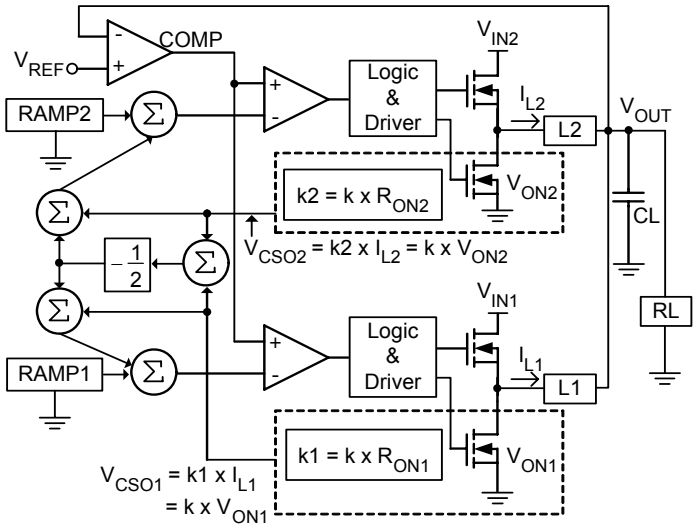


Figure 5. Current Balance

Gate control

a. Before SS signal reach the valley of the ramp voltage, UGATE and LGATE will be off.

b. If SS pin is pulled down 0.4V, UGATE and LGATE will be off.

c. UV protect function caused by FB < 0.6V and SS > 3.7V, and controller will trigger Always Hiccup Mode.

d. When OC function occurs and SS > 3.7V, a constant current of 10μA starts to discharge the capacitor connected to SS pin right away. When OC occurs, UGATE and LGATE will be off. When the voltage at the capacitor connected to SS pin pass about 0.4V, a constant current of 10μA starts to charge the capacitor. The PWM signal is enable to pass to UGATE and

LGATE. OCP function monitors both channels, either one can activate OCP. If the OC protection occurs three times, OCSD (Over Current Shut Down) will be activated and shut down the chip.

e. When fault conditions occur or SS < 0.4V, the current sense function will be disabled.

Power Good

PGOOD goes high when soft-start voltage > 3.7V, and no fault conditions.

Feedback Loop Compensation

The RT8805 is a voltage mode controller ; the control loop is a single voltage feedback path including an error amplifier and PWM comparator. In order to achieve fast transient response and accurate output regulation, an adequate compensator design is necessary. The goal of the compensation network is to provide adequate phase margin (greater than 45 degrees) and the highest 0dB crossing frequency. To manipulate loop frequency response under its gain crosses over 0dB at a slope of -20dB/ decade.

1) Modulator Frequency Equations

RT8805 is a voltage mode buck converter using the high gain error amplifier with transconductance (OTA, Operational Transconductance Amplifier), as Figure 6 shown.

The Transconductance:

$$GM = \frac{\Delta I_{OUT}}{\Delta V_M}$$

ΔV_M = (EA+) - (EA-) ; ΔI_{OUT} = E/A output current.

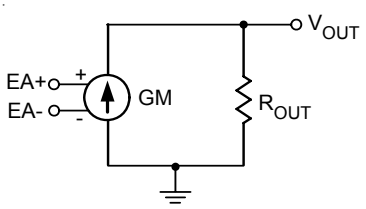


Figure 6. OTA Topology

This transfer function of OTA is dominated by a higher DC gain and the output filter (L_{OUT} and C_{OUT}) with a double pole frequency at F_{LC} and a zero at F_{ESR}. The DC gain of the modulator is the input voltage (V_{IN}) divided by the peak to peak oscillator voltage V_{RAMP}.

The first step is to calculate the complex conjugate poles contributed by the LC output filter.

The output LC filter introduces a double pole, 40dB/decade gain slope above its corner resonant frequency, and a total phase lag of 180 degrees. The resonant frequency of the LC filter expressed as follows:

$$F_{P(LC)} = \frac{1}{2\pi \times \sqrt{L_{OUT} \times C_{OUT}}}$$

The next step of compensation design is to calculate the ESR zero. The ESR zero is contributed by the ESR associated with the output capacitance. Note that this requires that the output capacitor should have enough ESR to satisfy stability requirements. The ESR zero of the output capacitor expressed as follows:

$$F_{Z(ESR)} = \frac{1}{2\pi \times C_{OUT} \times ESR}$$

2) Compensation Frequency Equations

The compensation network consists of the error amplifier and the impedance networks Z_C and Z_F as Figure 7 shown.

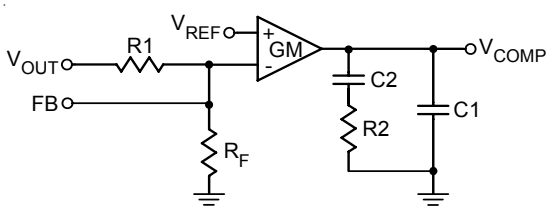


Figure 7. Compensation Loop

$$F_{Z1} = \frac{1}{2\pi \times R2 \times C2}$$

$$F_{P1} = \frac{1}{2\pi \times R1 \times C1}$$

$$F_{P2} = \frac{1}{2\pi \times R2 \times \left(\frac{C1 \times C2}{C1 + C2}\right)}$$

Figure 8 shows the DC-DC converter's gain vs. frequency. The compensation gain uses external impedance networks ZC and ZF to provide a stable, high bandwidth loop. High crossover frequency is desirable for fast transient response, but often jeopardize the system stability. In order to cancel one of the LC filter poles, place F_{Z1} before the LC filter resonant frequency. In the experience, place F_{Z1} at 10% LC filter resonant frequency. Crossover frequency should be higher than the ESR zero but less than 1/5 of the switching frequency. The F_{P2} should be place at half the switching frequency.

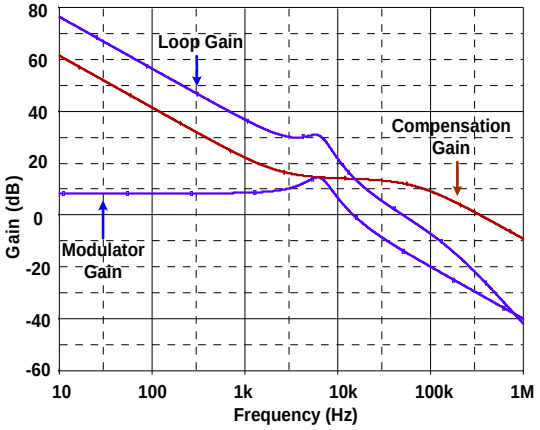


Figure 8. Type 2 Bode Plot

There is another type of compensation called Type 3 compensation that adds a pole-zero pair to the Type 2 network. It's used to compensate output capacitor whose ESR value is much lower (pure MLCC or OSCON Capacitors).

As shown in Figure 9, to insert a network between V_{OUT} and FB in the original Type 2 compensation network can result in Type 3 compensation. Figure 10 shows the difference of their AC response. Type 3 compensation has an additional pole-zero pair that causes a gain boost at the flat gain region. But the gain boosted is limited by the ratio (R1+R4)/R4; if R3 << R4.

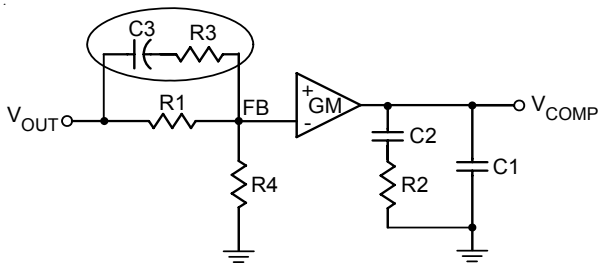


Figure 9. Additional Network of Type 3 Compensation (Add between V_{OUT} and FB)

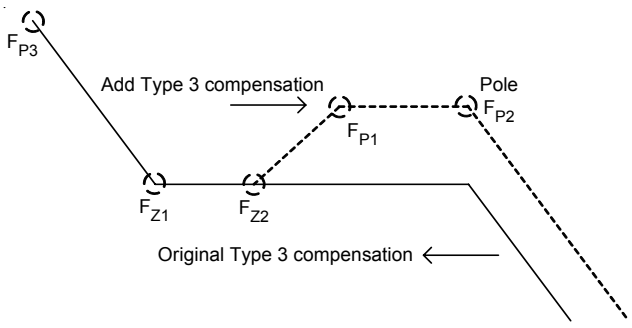


Figure 10. AC Response Curves of Type 2 and 3

Type 3 will induce three poles and two zeros.

Zeros :

$$F_{Z1} = \frac{1}{2\pi \times R2 \times C2}$$

$$F_{Z2} = \frac{1}{2\pi \times (R1+R3) \times C3}$$

Poles :

$$F_{P1} = \frac{1}{2\pi \times R2 \times \left(\frac{C1 \times C2}{C1+C2}\right)}$$

$$F_{P2} = \frac{1}{2\pi \times R3 \times C3}$$

$$F_{P3} = \frac{1}{2\pi \times \left(\frac{R1 \times R3 \times C1}{R1+R3}\right)};$$

which is in the origin.

We recommend F_{Z1} placed in 0.5 x $F_{P(LC)}$; F_{Z2} placed in $F_{P(LC)}$; F_{P1} placed in F_{ESR} and F_{P2} placed in 0.5 x F_{SW}. Figure 11 shows Type 3 Bode Plot.

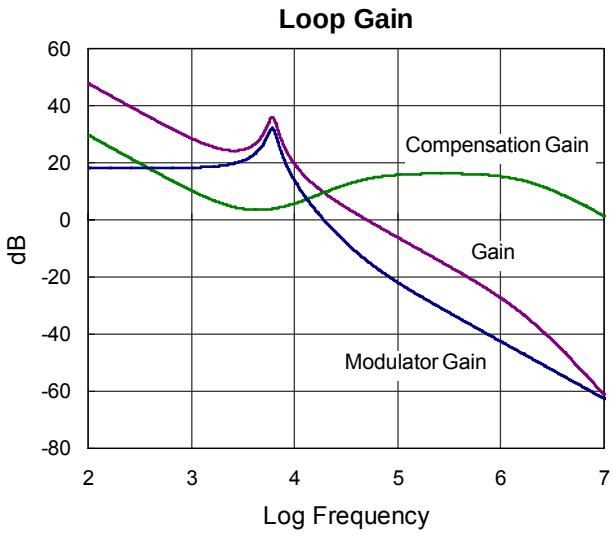


Figure 11. Type 3 Bode Plot

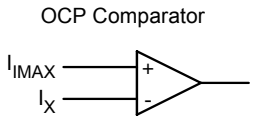
Protection

OCP

The RT8805 uses " Cycle by Cycle" current comparison. The over current level is set by IMAX pin. When OC function occurs and SS > 3.7V, a constant current of 10μA starts to discharge the capacitor connected to SS pin right away. When OC occurs, UGATE and LGATE will be off.

When the voltage at the capacitor connected to SS pin pass about 0.4V, a constant current of 10μA starts to charge the capacitor. The PWM signal is enabled to pass to the UGATE and LGATE. OCP function monitors both channels, either one can activate OCP. If the OC protection occurs three times, the chip will shut down and the state will only be released by POR.

RT8805 uses an external resistor R_{IMAX} to set a programmable over current trip point. OCP comparator compares each inductor current with this reference current. RT8805 uses hiccup mode to eliminate fault detection of OCP or reduce output current when output is shorted to ground. The OCP comparator compares the difference between I_X and I_{IMAX}.



For example:

From *Electrical Specifications* : R_{IMAX} = 33kΩ

→ V_{PHASE} = -220mV

Assume Low side MOSFET $R_{DS(ON)}$ = 3mΩ.

Get the OCP setting current is $\frac{220mV}{3m\Omega}$=73A per PHASE (the valley of inductor's current).

Change the setting current which you want from 73A per PHASE to 50A per PHASE.

Following below steps:

1. Calculate phase voltage. If Low side MOSFET

   $R_{DS(ON)}$ = 3mΩ, V_{PHASE_new} = -150mV.

2. $R_{IMAX\_new} = \frac{-220mV}{V_{PHASE\_new}} \times 33k\Omega$

   $R_{IMAX\_new} = 48.4k\Omega$

UVP

By detecting voltage at FB pin when SS > 3.7V. If FB < 0.6V, the chip will trigger the always Hiccup mode and a constant current source 10μA starts to charge capacitor at SS pin when SS pass 0.4V and discharge Css when SS > 3.7V. As Figure 12 shown.

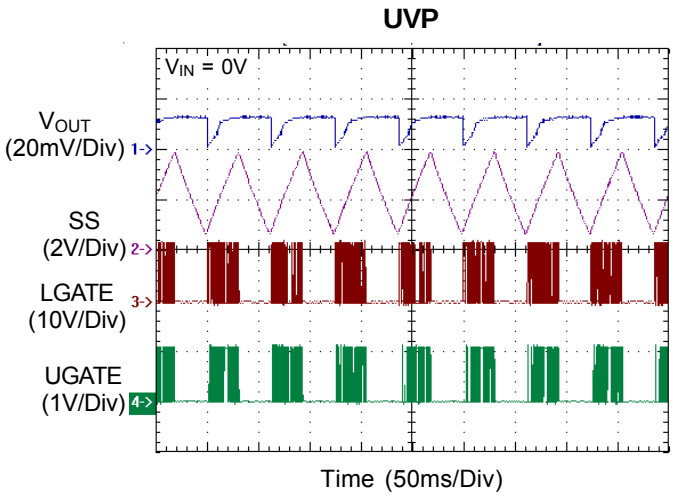


Figure 12. UVP (Always Hiccup Mode)

OTP

Monitor the temperature near the driver part within the chip. Shutdown the chip when OTP (Typical trip point : 170°C).

General Design Guide

This design guide is intended to provide a high-level explanation of the steps necessary to create a multi-phase power converter. It is assumed that the reader is familiar with many of the basic skills and techniques referenced below.

Power Stages

Designing a multi-phase converter is to determine the number of phases. This determination depends heavily on the cost analysis which in turn depends on system constraints that differ from one design to the next. Principally, the designer will be concerned with whether components can be mounted on both sides of the circuit board, whether through-hole components are permitted, the total board space available for power-supply circuitry, and the maximum amount of load current. Generally speaking, the most economical solutions are those in which each phase handles between 20 to 25 A (One Upper and one Lower MOSFET). All surface-mount designs will tend toward the lower end of this current range.

If through-hole MOSFETs and inductors can be used, higher per-phase currents are possible. In cases where

board space is the limiting constraint, current can be pushed as high as 40A per phase, but these designs require heat sinks and forced air to cool the MOSFETs, inductors and heat dissipating surfaces.

MOSFETs

The choice of MOSFETs depends on the current each MOSFET will be required to conduct, the switching frequency, the capability of the MOSFETs to dissipate heat, and the availability and nature of heat sinking and air flow.

Package Power Dissipation

When choosing MOSFETs it is important to consider the amount of power being dissipated in the integrated drivers located in the controller. Since there are a total of two drivers in the controller package, the total power dissipated by both drivers must be less than the maximum allowable power dissipation for the VQFN package. Calculating the power dissipation in the drivers for a desired application is critical to ensure safe operation. Exceeding the maximum allowable power dissipation level will push the IC beyond the maximum recommended operating junction temperature of 125°C. The maximum allowable IC power dissipation for the 3x3 VQFN package is approximately 1.47W at room temperature.

According below equations at two phases operation, it's clear to describe that the junction temperature of the chip is directly proportional to the total C_{ISS} (including C_{UGATE} and C_{LGATE}) of all external MOSFETs.

$$P_D = (C_{UGATE} \times V_{BOOT-PHASE}^2 \times f) + (C_{LGATE} \times V_{CC}^2 \times f) + \chi$$

$$T_J = T_A + (\theta_{JA} \times P_D)$$

(χ is the minor factor and could be ignored)

For example, according to the application we evaluated on board, the C_{UGATE} = 1nF, C_{LGATE} = 5nF (dual MOSFETs in parallel), V_{CC} = 12V, $V_{BOOT-PHASE}$ = 12V, and operation frequency = 300kHz.

$$P_D \approx 1nF \times 12^2 \times 300kHz + 2 \times 5nF \times 12^2 \times 300kHz = 475mW / PHASE$$

$$T_J = 30°C + 68°C/W \times 0.475W \times 2 = 94.6°C$$

That means the junction temperature is most likely to be operated under or over maximum (~125°C) operation rating.

Layout Considerations

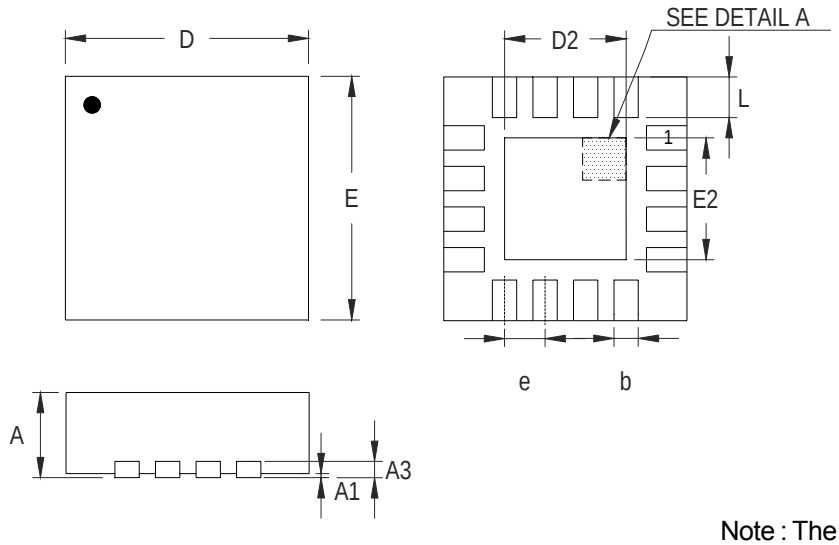
Layout is very important in high frequency switching converter design. If designed improperly, the PCB could radiate excessive noise and contribute to the converter instability.

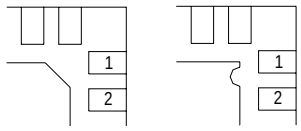
First, place the PWM power stage components. Mount all the power components and connections in the top layer with wide copper areas. The MOSFETs of Buck, inductor, and output capacitor should be as close to each other as possible. This can reduce the radiation of EMI due to the high frequency current loop. If the output capacitors are placed in parallel to reduce the ESR of capacitor, equal sharing ripple current should be considered. Place the input capacitor directly to the drain of high-side MOSFET. In multi-layer PCB, use one layer as power ground and have a separate control signal ground as the reference of the all signal. To avoid the signal ground is effect by noise and have best load regulation, it should be connected to the ground terminal of output. Furthermore, follows below guidelines can get better performance of IC :

1. A multi-layer printed circuit board is recommended.
2. Use a middle layer of the PC board as a ground plane and making all critical component ground connections through vias to this layer.
3. Use another solid layer as a power plane and break this plane into smaller islands of common voltage levels.
4. Keep the metal running from the PHASE terminal to the output inductor short.
5. Use copper filled polygons on the top and bottom circuit layers for the phase node.
6. The small signal wiring traces from the LGATE and UGATE pins to the MOSFET gates should be kept short and wide enough to easily handle the several Amperes of drive current.
7. The critical small signal components include any bypass capacitors, feedback components, and compensation components. Position those components close to their pins with a local GND connection, or via directly to the ground plane.

8. R_T and R_{IMAX} resistors should be near the R_T and R_{IMAX} pin respectively, and their GND return should be short, and kept away from the noisy MOSFET GND.
9. Place the compensation components close to the FB and COMP pins.
10. The feedback resistors for both regulators should also be located as close as possible to the relevant FB pin with vias tied straight to the ground plane as required.
11. Minimize the length of the connections between the input capacitors, C_{IN} and the power switches by placing them nearby.
12. Position both the ceramic and bulk input capacitors as close to the upper MOSFET drain as possible, and make the GND returns (From the source of lower MOSFET to V_{IN}, C_{VIN}, GND) short.
13. Position the output inductor and output capacitors between the upper MOSFET and lower MOSFET and the load.
14. AGND should be on the clearer plane, and kept away from the noisy MOSFET GND.

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	1.300	1.750	0.051	0.069
E	2.950	3.050	0.116	0.120
E2	1.300	1.750	0.051	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

V-Type 16L QFN 3x3 Package

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