CMOS HIGH SPEED GATE ARRAY

■DESCRIPTION

The SLA7000 series consists of a group of 6 CMOS gate arrays with gate counts from 1,632 to 16,250 gates. The series is fabricated utilizing our 1.5 micron high speed CMOS silicon gate technology to achieve propagation delays of 1.0ns for the internal gates. All I/O buffers are TTL and CMOS compatible which makes this series an ideal choice for replacing existing discrete logic as well as for new designs requiring very high speed and/or high gate counts.

■FEATURES

- ●Very high speed silicon gate CMOS technology
- ●TTL and CMOS I/O compatible
- ●High output drivercapability
- ●Gate densities from 1,632 to 16,250 gates
- ●"Hard" MSI macrocells for superior AC performance
- ●Cell libraries, software, and documentation available for IBM® PC compatibles with Future Net or OrCAD and Daisy and Mentor systems

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■SLA7000 SERIES

Parameter \ Series	SLA7160	SLA7220	SLA7340	SLA7490	SLA7620	SLA7800	SLA790S*3
Gates (2-input NAND)	1,632	2,232	3,432	4,900	6,210	8,000	16,250
Technology	SILICON GATE CMOS 2 LAYER METALLIZATION						
I/O level	TTL, CMOS						
Delay time: Internal gate*1	1.0ns						
Delay time: Input buffer*1, *2	tp_{LH}=1.9ns, tp_{HL}=3.4ns						
Delay time: Output buffer*2	tp_{LH}=5.5ns, tp_{HL}=4.7ns, C_L=30pF						
Total ports for I/O	70	82	104	128	150	170	188
Total ports for Power/GND (Max)	8	8	8	8	8	8	8
Output mode	Normal, Open-drain, 3-state, Bi-directional						

*1 Typical fanout of 2, 1mm of interconnect.
*2 Standard I/O cell.
*3 Sea of Gates (approx 8K usable gates.)

■ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.3 to 7.0	V
Input voltage	V_I	−0.3 to V_{DD}+0.3	V
Output voltage	V_O	−0.3 to V_{DD}+0.3	V
Storage temperature	T_{stg}	−65 to 150	°C

■RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}	—	4.75	5.00	5.25	V
Operating temperature	T_{opr}	—	0	—	70	°C

■ELECTRICAL CHARACTERISTICS

(V_{DD}=5V ± 5%, Ta=0 to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply current	I_{DD}	Standby	—	2	—	μA
High level output voltage	V_{OH}	V_{DD}=4.75V I_{OH}=−6mA	2.4	—	—	V
Low level output voltage	V_{OL}	V_{DD}=4.75V I_{OL}=6mA	—	—	0.4	V
High level input voltage	V_{IH}	V_{DD}=5.25V	2.0	—	—	V
Low level input voltage	V_{IL}	V_{DD}=4.75V	—	—	0.8	V
Input leakage current	I_{LI}	—	−1	—	1	μA

■PACKAGE TYPES

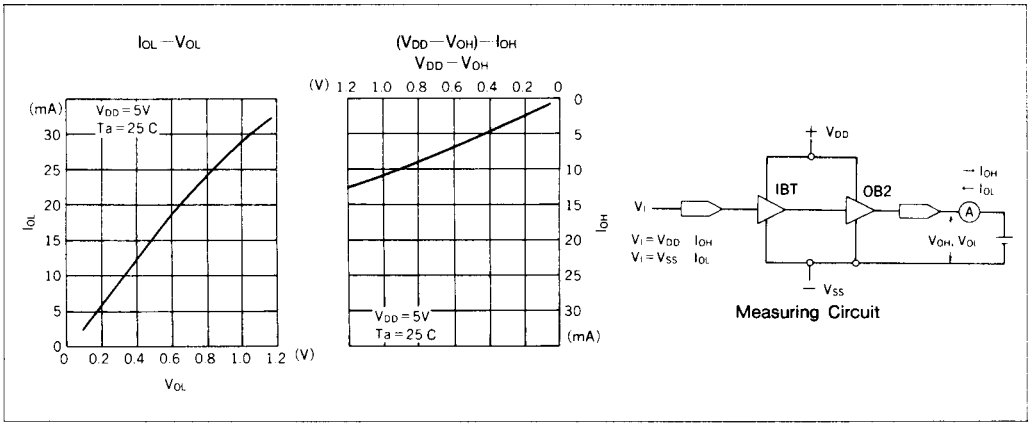
Package Type	No.of Pins	Code	7160	7220	7340	7490	7620	7800	7905
No. of Pads			78	90	112	136	158	178	178
No. of Gross Gates			1632	2232	3432	4900	6210	11040	13500
Plastic DIP	22	C22	A						
	24	C24	A*						
	28	C28	A*	A*					
	40	C40	A*	A*	A*	A*			
	42	C42	A*	A*					
Plastic Shrink DIP	64	S64	A*	A*	A*				
Plastic QFP	44	F44-6	A*	(A)					
	52	F52-6	A*						
	60	F60-6	A	A*	A	A	A		
	60	F60-5	A*	(A)	A*	(A*)	(A)		
	80	F80-5	A*	A*	A*	A*	A*		
	100	F100-5	A*	A*	A*	A*	A*	F	
	120	F120-8			A*	A*	A*	(A)	
	128	F128-8			A*	A*	A*	A*	A*
	128	F128-5							
	144	F144-8				A*	A*	A*	A*
	160	F160-8				A*	A*	A*	A*
	196	F196-9						(A)	(A)
Plastic SOP	24	M24-2	A						
	28	M28-2	A*	(A)					
Plastic PGA	89	G89		(A)	(A)	A	(A)		
	132	G132			(A)	A	(A)	(A)	(A)
	176	G176						A	A
PLCC	44	J44	A*			(A)	(A)		
	68	J68	A*	A*	A*	A*	A*		
	84	J84	(A)	A*	A*	A*	A*	A*	A*
Ceramic PGA	72	P72			A*	A*	A*		
	132	P132		A*	A*	A*	A*	A*	A*

A: Available Now (A): Lead Frame Currently Not Available *: Pin Pad Table Exists F: Currently Not Available

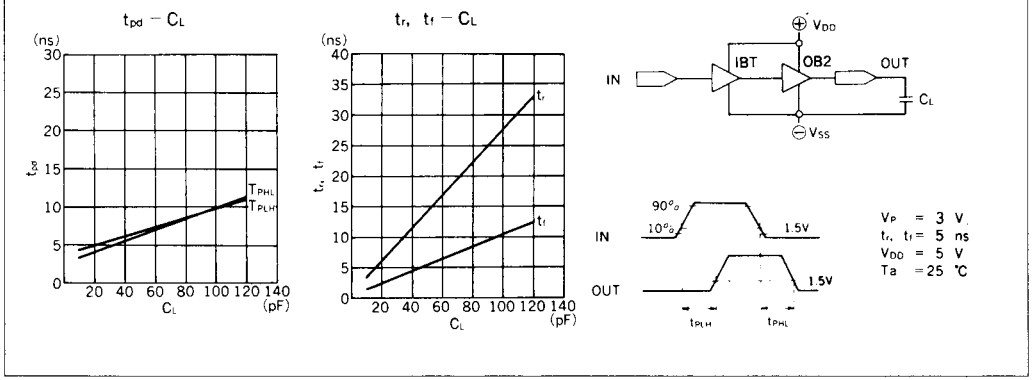
(#): Bondable Pads for Die/Package Configuration

■PERFORMANCE CURVES

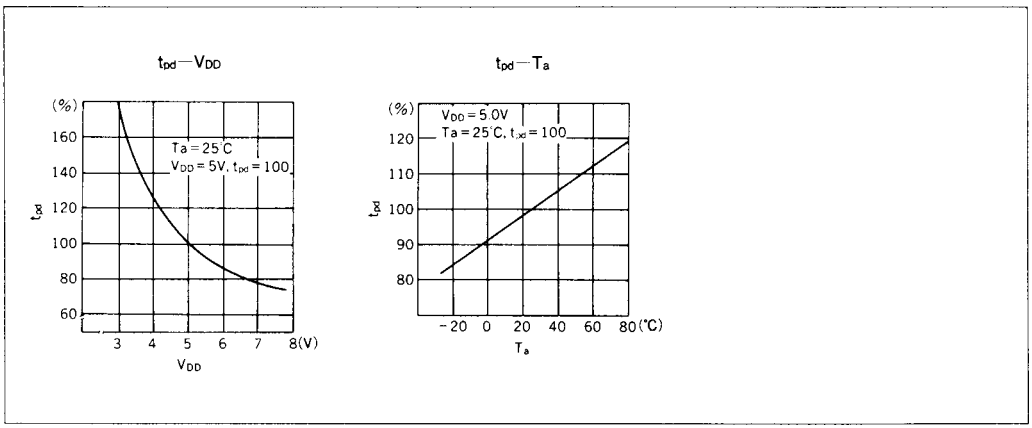
●Output Current



●t_{pd}, t_r, t_f—C_L



●Delay Time



■ GATE ARRAY DESIGN FLOW