Low Capacitance Dual Line ESD Protection Diode Array
SM12/SM15 SOT23-3

General Description

The SM12/SM15 of transient voltage suppressors (TVS) are designed to protect components which are connected to data and transmission lines from voltage surges caused by electrostatic discharge (ESD). TVS diodes are characterized by their high surge capability, low operating and clamping voltages, and fast response time. This makes them ideal for use as board level protection of sensitive semiconductor components. The dual-junction common-anode design allows the user to protect one bidirectional data line or two unidirectional lines. The low profile SOT23-3 package allows flexibility in the design of "crowded" circuit boards. The SM12/SM15 will meet the surge requirements of IEC 61000-4-2 (Formerly IEC801-2), Level 4, "Human Body Model" for air and contact discharge.

Applications

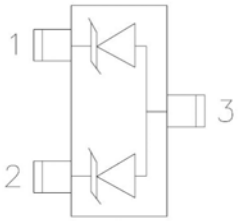
- Cellular Handsets and Accessories
- Portable Electronics
- Industrial Controls
- Set-Top Box
- Servers, Notebook, and Desktop PC

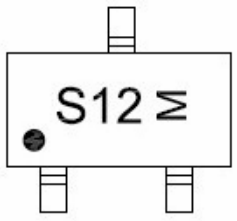
Features

- Transient protection for data & power lines to IEC 61000-4-2 (ESD) ±15kV (air), ±8kV (contact)
- Protects one bidirectional line or two unidirectional lines
- Working Voltages: 12V (SM12)
  15V (SM15)
- Low clamping voltage
- Solid-state silicon avalanche technology

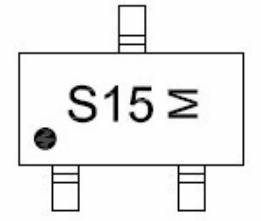
Pin Configurations

Top View





M: Month Code
SM12
SOT23-3



M: Month Code
SM15
SOT23-3

Ordering Information

Part Number	Working Voltage	Packaging Type	Channel	Marking Code	Shipping Qty
SM12	12.0V	SOT23-3	2	S12	3000pcs/7Inch Tape & Reel
SM15	15.0V			S15	

Absolute Maximum Ratings

RATING	SYMBOL	VALUE	UNITS
Peak Pulse Power (tp = 8/20μs)	P_{PK}	140	Watts
Thermal Resistance, Junction to Ambient	θ_{JA}	325	°C/W
Lead Soldering Temperature	T_L	260(10 sec.)	°C
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +125	°C

Electrical Characteristics (SM12)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Reverse Stand-Off Voltage	V_{RWM}				12	V
Reverse Breakdown Voltage	V_{BR}	It = 1mA	16		18	V
Reverse Leakage Current	I_R	V_{RWM} = 12V, T=25°C			1	μA
Clamping Voltage	V_C	I_{PP} = 5.9A, t_p = 8/20μS			23	V
Peak Pulse Current	I_{PP}	tp = 8/20μs			5.9	A
Junction Capacitance	C_J	Pin 1 to 3 and Pin 2 to 3, VR = 0V, f = 1MHz		20	30	pF
Reverse dynamic resistance	$R_{dyn,rev}$	I_{PP}<2A		1.12		Ω
Forward dynamic resistance	$R_{dyn,fwd}$			0.81		
Reverse dynamic resistance	$R_{dyn,rev}$	I_{PP} >2A		0.92		Ω
Forward dynamic resistance	$R_{dyn,fwd}$			0.42		

Electrical Characteristics (SM15)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Reverse Stand-Off Voltage	V_{RWM}				15	V
Reverse Breakdown Voltage	V_{BR}	It = 1mA	16.7		18.7	V
Reverse Leakage Current	I_R	V_{RWM} = 15V, T=25°C			1	μA
Clamping Voltage	V_C	I_{PP} = 5.9A, t_p = 8/20μS			23	V
Peak Pulse Current	I_{PP}	tp = 8/20μs			5.9	A
Junction Capacitance	C_J	Pin 1 to 3 and Pin 2 to 3, V_R = 0V, f = 1MHz		20	30	pF
Reverse dynamic resistance	$R_{dyn,rev}$	I_{PP}<2A		1.12		Ω
Forward dynamic resistance	$R_{dyn,fwd}$			0.81		
Reverse dynamic resistance	$R_{dyn,rev}$	I_{PP} >2A		0.92		Ω
Forward dynamic resistance	$R_{dyn,fwd}$			0.42		

Detailed Description

Device Connection Options

SM12/SM15 is designed to protect one bidirectional or two unidirectional data or I/O lines operating at 12V/15V. Connection options are as follows: Bidirectional: Pin 1 is connected to the data line and pin 2 is connected to ground (Since the device is symmetrical, these connections may be reversed). The ground connection should be made directly to a ground plane. The path length should be kept as short as possible to minimize parasitic inductance. Pin 3 is not connected. Unidirectional: Data lines are connected to pin 1 and pin 2. Pin 3 is connected to ground. For best results, this pin should be connected directly to a ground plane on the board. The path length should be kept as short as possible to minimize parasitic inductance.

Circuit Board Layout Recommendations for Suppression of ESD

Good circuit board layout is critical for the suppression of fast rise-time transients such as ESD. The following guidelines are recommended (Refer to application note SI99-01 for more detailed information): Place the TVS near the input terminals or connectors to restrict transient coupling. Minimize the path length between the TVS and the protected line. Minimize all conductive loops including power and ground loops. The ESD transient return path to ground should be kept as short as possible. Never run critical signals near board edges. Use ground planes whenever possible.

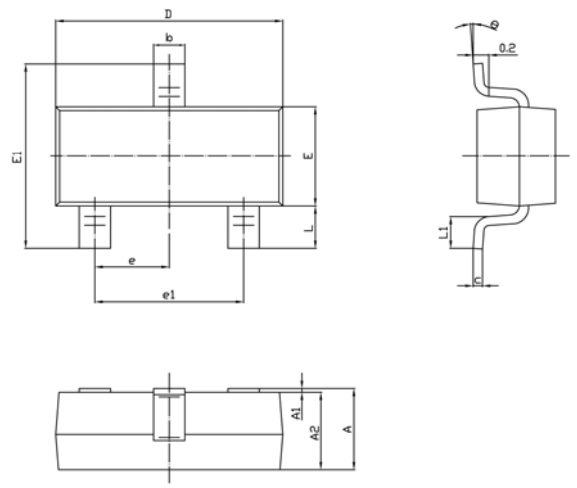
Matte Tin Lead Finish

Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. In addition, unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation of the solder joint.

Package Information

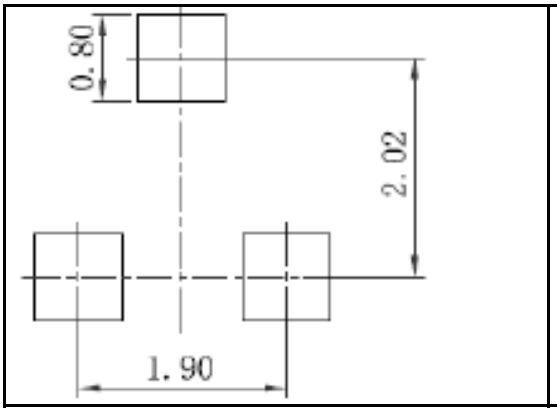
SM12/SM15: SOT23-3

Outline Drawing



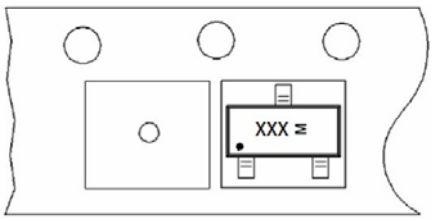
Symbol	DIMENSIONS			
	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	0.900	1.200	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.100	0.035	0.039
b	0.300	0.500	0.012	0.020
c	0.080	0.180	0.003	0.007
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950TYP		0.037TYP	
e1	1.800	2.050	0.071	0.080
L	0.550REF		0.022REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°

Land Pattern



NOTES:
1. Compound dimension: 2.90×1.30;
2. Unit: mm;
3. General tolerance±0.05mm unless otherwise specified;
4. The layout is just for reference.

Tape and Reel Orientation



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