

### OVERVIEW

The SM6104 is a 6-bit flash parallel A/D converter based on NPC's proprietary molybdenum gate CMOS technology. It features a high-speed conversion of 20 Msps, and a low current consumption of 16mA (typ). The SM6104 is available speed in 18-pin plastic DIPs and 18-pin plastic SOPs.

### FEATURES

- 6-bit resolution
- Maximum conversion speed: 20 Msps
- Non-linearity of  $\pm 1/2$  LSB (type)
- Differential non-linearity of  $\pm 1/2$  LSB (typ)
- Guaranteed mono converts without code missing
- External sample-and-hold circuits not required
- Internal output latch for 6-bit conversion data and overflow flag
- Tristate output drivers
- Supports 7-bit conversion using two devices connected in series.
- Supports 40 Msps conversion using twod evices connected in parallel (SM6104P and SM6104S only)
- Single 5 V supply
- Molybdenum gate CMOS process, low-power 16mA (typ) at 5.0V and 20 MHz (SM6104P AND SM6104S)

### SELECTION GUIDE

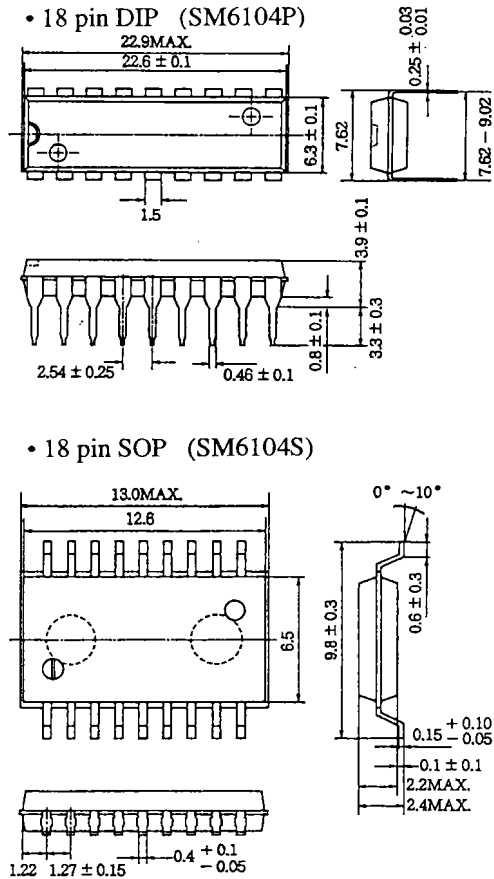
Version	Conversion	Package
SM6104P	20Msps	18 pinDIP
SM6104P1	15Msps	18 pin DIP
SM6104S	20Msps	18 pin SOP
SM6104S1	15Msps	18 pin SOP

### APPLICATIONS

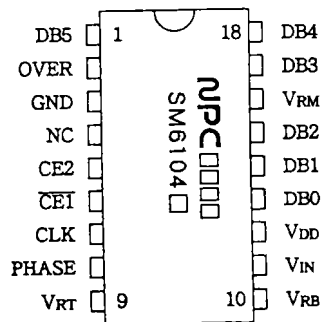
- High-speed facsimile machines
- Digital television systems
- Color television decoder units
- Radar pulse analysis
- Data acquisition systems
- Any other applications that require high-speed, low-power A/D conversion.

### PACKAGE DIMENSIONS

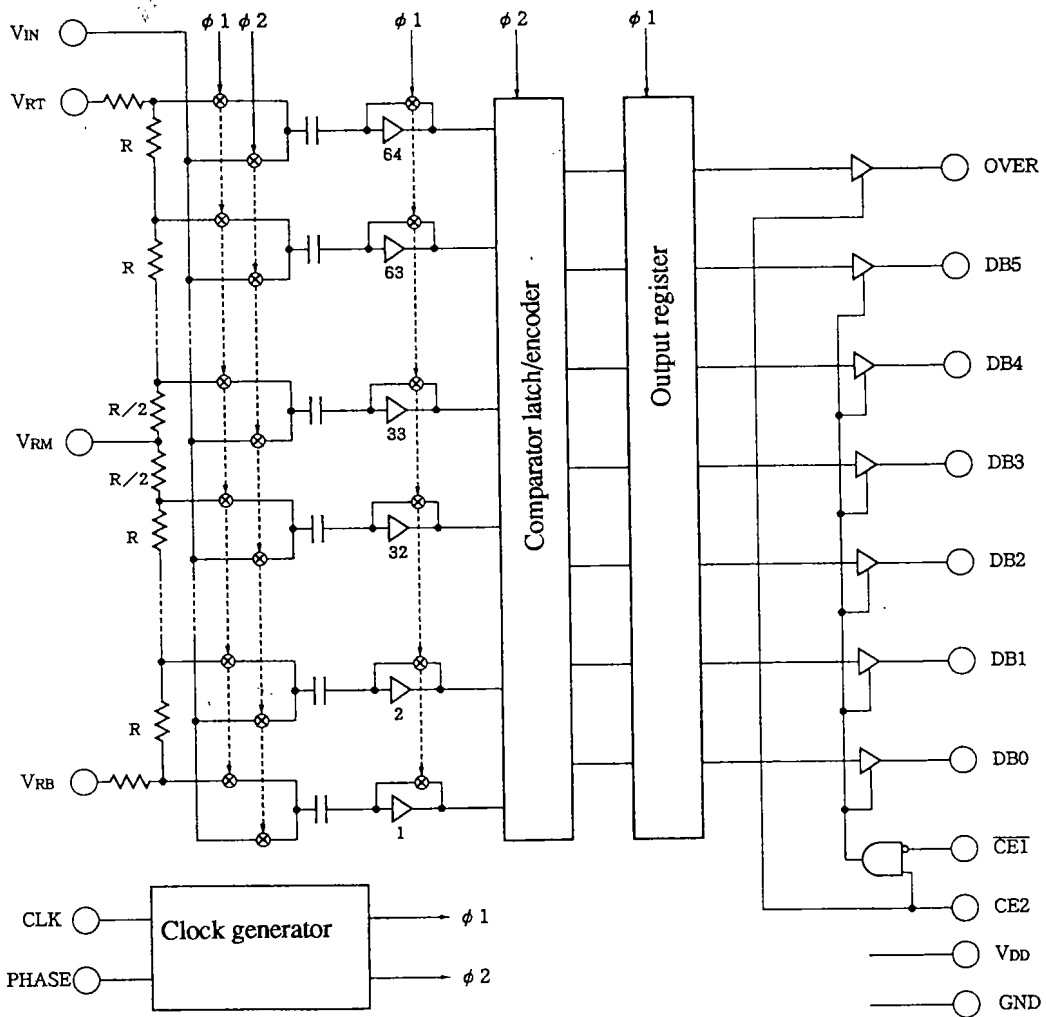
Unit: mm



### PIN OUT TOP VIEW



## ■ BLOCK DIAGRAM



## ■ PIN DESCRIPTION

No.	Pin	Description	No.	Pin	Description
1	DB5	Data output pin (MSB)	10	V <sub>RS</sub>	Reference voltage (LOW)
2	OVER	Overflow flag (tristate)	11	V <sub>IN</sub>	Analog input, V <sub>RB</sub> ≤ V <sub>IN</sub> ≤ V <sub>RT</sub>
3	GND	Ground (-)	12	V <sub>DD</sub>	Positive supply
4	NC	No connection	13	DB0	Data output (LSB)
5	CE2	Tristate control pin	14	DB1	Data output
6	CE1	Tristate control pin	15	DB2	Data output
7	CLK	Clock input	16	V <sub>RM</sub>	Reference voltage centerpoint (linearity compensation)
8	PHASE	Clock polarity select	17	DB3	Data output
9	V <sub>RT</sub>	Reference voltage (HIGH)	18	DB4	Data output

■ ABSOLUTE MAXIMUM RATINGS

(GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V <sub>DD</sub>	-0.3 to +7.0	V
Input/output voltage	V <sub>IN</sub> , V <sub>IO</sub>	-0.3 to V <sub>DD</sub> +0.3	V
Storage temperature	T <sub>STG</sub>	-40 to +125	°C
Power dissipation	P <sub>w</sub>	500	mW
Soldering temperature	T <sub>SLD</sub>	260	°C
Soldering time	t <sub>SLD</sub>	10	sec

■ DC ELECTRICAL CHARACTERISTICS

V<sub>DD</sub> = 5V±5%, f<sub>CLK</sub>=20MHz, Ta=0 to 70 °C unless otherwise noted.

Item	Symbol	Condition	Limits			Unit
			MIN	TYP	MAX	
Digital input voltage	V <sub>IH</sub>		3.5			V
	V <sub>IL</sub>				1.0	
Digital input current	I <sub>IH</sub>	V <sub>IN</sub> =V <sub>DD</sub>			2	μA
	I <sub>IL</sub>	V <sub>IN</sub> =0V	-2			
Digital output voltage	V <sub>OH</sub>	I <sub>OH</sub> =-1.0mA	*1			V
	V <sub>OL</sub>	I <sub>OL</sub> =2.0mA			0.4	
Tristate output leak voltage	I <sub>OHL</sub>	V <sub>O</sub> =V <sub>DD</sub>			3	μA
	I <sub>OLL</sub>	V <sub>O</sub> =0V	-3			
Analog input register	R <sub>VIN</sub>	V <sub>IN</sub> =DC	1			MΩ
Analog input capacitor	C <sub>VIN</sub>			50		pF
Reference input	R <sub>REF</sub>	V <sub>RT</sub> to V <sub>RB</sub>	180	250	350	Ω
Current consumption	I <sub>DD</sub>	SM6104P/S		16	25	mA
		SM6104P1/S1		16	25	

\*1: V<sub>DD</sub>=0.4

\*2: f<sub>CLK</sub>=15MHz

■ RECOMMENDED OPERATING CONDITIONS

(GND = 0V)

Item	Symbol	MIN	TYP	MAX	Unit
Supply voltage	V <sub>DD</sub>	4.75	5.0	5.25	V
Reference voltage 1	V <sub>RT</sub>	V <sub>RB</sub> +2.0		V <sub>DD</sub> +0.1	V
Reference voltage 2	V <sub>RB</sub>	-0.1		V <sub>RT</sub> -2.0	V
Analog full scale	V <sub>RT</sub> -V <sub>RB</sub>	2.0			V
Operating temperature	T <sub>OPR</sub>	0		70	°C

■ CONVERSION CHARACTERISTICS

V<sub>DD</sub> = 5V±5%, Ta=0 to 70 °C, V<sub>RT</sub>=2.0V, V<sub>RB</sub>=0V, unless otherwise noted.

SM6104P/S

Item	Symbol	Condition	Rating			Unit
			MIN	TYP	MAX	
Resolution	RES				6	Bits
Non-linearity	NL	V <sub>IN</sub> =DC	f <sub>CLK</sub> =20MHz	±1/2	±1	LSB
			f <sub>CLK</sub> =5MHz	±1/4	±1/2	
Differential Non-linearity	DNL	V <sub>IN</sub> =DC	f <sub>CLK</sub> =20MHz	±1/2	±3/4	LSB
			f <sub>CLK</sub> =5MHz	±1/4	±1/2	

■ AC ELECTRICAL CHARACTERISTICS

V<sub>DD</sub> = 5V±5%, Ta=0 to 70 °C, unless otherwise noted.

SM6104P/S

Item	Symbol	Condition	Rating			Unit
			MIN	TYP	MAX	
CLK HIGH-level pulse width	t <sub>PWH</sub>		25		5000	ns
CLK LOW-level pulse width	t <sub>PWL</sub>		25		5000	
Aperture delay time	t <sub>A</sub>			10		
Conversion delay time	t <sub>D</sub>			25	40	

SM6104P1/S1

Item	Symbol	Condition	Rating			Unit
			MIN	TYP	MAX	
Resolution	RES				6	Bits
Non-linearity	NL	V <sub>IN</sub> =DC	f <sub>CLK</sub> =15MHz	±1/2	±3/4	LSB
			f <sub>CLK</sub> =5MHz	±1/4	±1/2	
Differential Non-linearity	DNL	V <sub>IN</sub> =DC	f <sub>CLK</sub> =15MHz	±1/2	±3/4	LSB
			f <sub>CLK</sub> =5MHz	±1/4	±1/2	

SM6104P1/S1

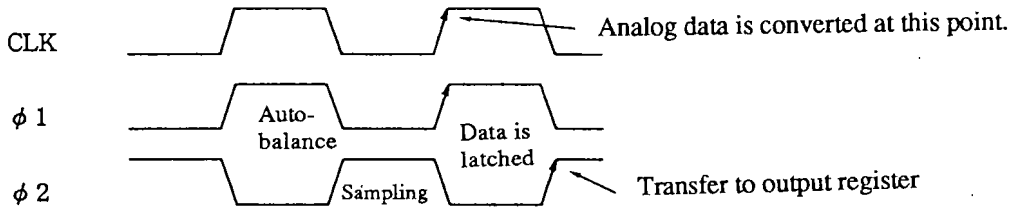
Item	Symbol	Condition	Rating			Unit
			MIN	TYP	MAX	
CLK HIGH-level pulse width	t <sub>PWH</sub>		33		5000	ns
CLK LOW-level pulse width	t <sub>PWL</sub>		33		5000	
Aperture delay time	t <sub>A</sub>			10		
Conversion delay time	t <sub>D</sub>			25	40	

1. Conversion Operation

Conversion is controlled by the external clock input to pin CLK which is used to generate the internal clocks  $\phi 1$  and  $\phi 2$ . The PHASE pin switches the polarity of the internal clocks as shown in the table on the right.

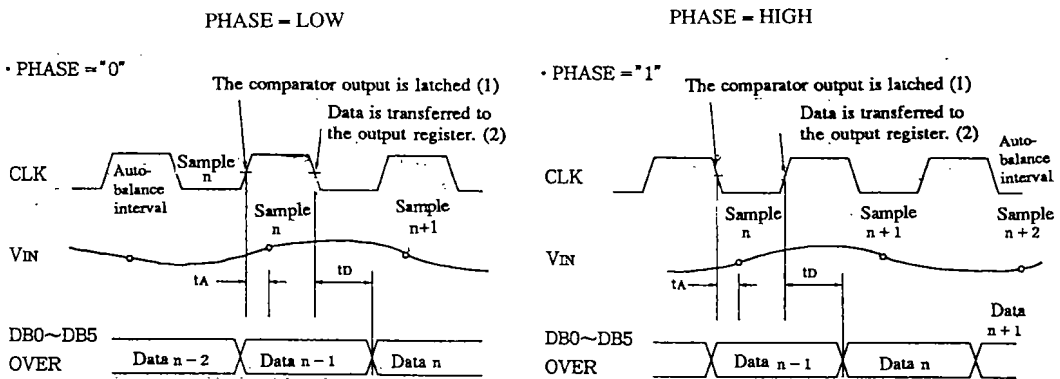
PHASE	$\phi 1$	$\phi 2$
0	CLK	$\overline{\text{CLK}}$
1	$\overline{\text{CLK}}$	CLK

ex.) When PHASE = 0:



The period during which  $\phi 1$  is HIGH is called the auto-balance interval. During this interval, the reference voltage is divided by the internal resistor ladder. These reference voltages are input to 64 comparators. The period during which  $\phi 2$  is HIGH is called the sampling interval. During this interval, the analog voltage is input to the comparators and compared with the previously latched reference voltages.

2. Timing Charts



3. Output tristate control

CE1	CE2	DB0 to DB5	OVER
0	1	Enable	Enable
1	1	Hi-Z	Enable
x	0	Hi-Z	Hi-Z

4. Output code

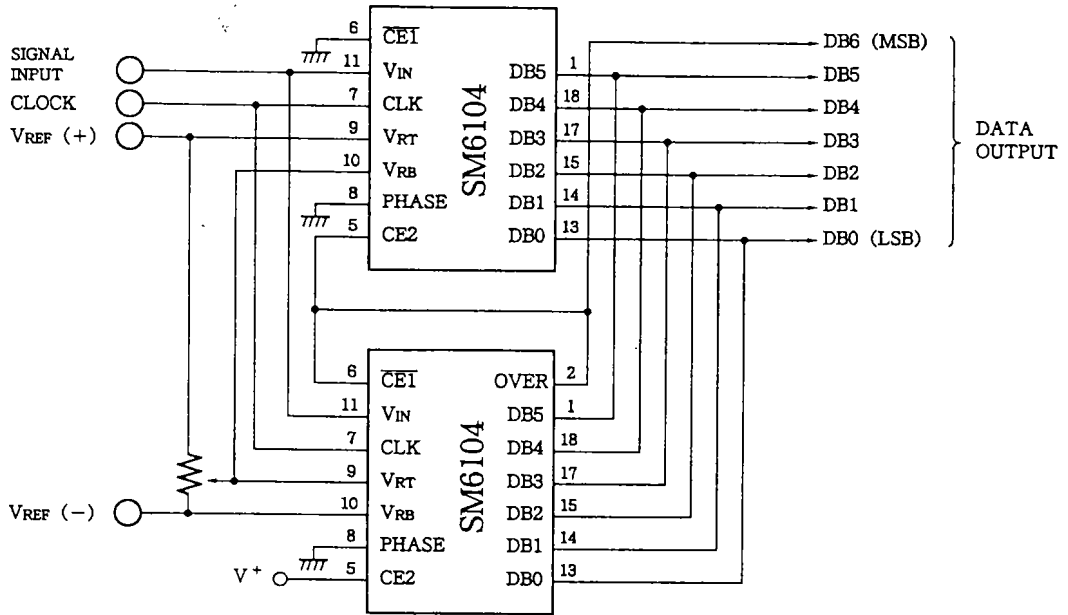
( $V_{RT}$  = about 2.56V,  $V_{RB}$  = about 0V)

Analog input voltage (V)	Input code							Decimal
	OVER	DB5	DB4	DB3	DB2	DB1	DB0	
0.00	0	0	0	0	0	0	0	0
0.04	0	0	0	0	0	0	1	1
0.08	0	0	0	0	0	1	0	2
0.12	0	0	0	0	0	1	1	3
0.16	0	0	0	0	1	0	0	4
:	:	:	:	:	:	:	:	:
1.20	0	0	1	1	1	1	1	30
1.24	0	0	1	1	1	1	1	31
1.28	0	1	0	0	0	0	0	32
1.32	0	1	0	0	0	0	0	33
1.36	0	1	0	0	0	0	0	34
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
2.40	0	1	1	1	1	0	0	60
2.44	0	1	1	1	1	0	1	61
2.48	0	1	1	1	1	1	0	62
2.52	0	1	1	1	1	1	1	63
2.56	1	1	1	1	1	1	1	127

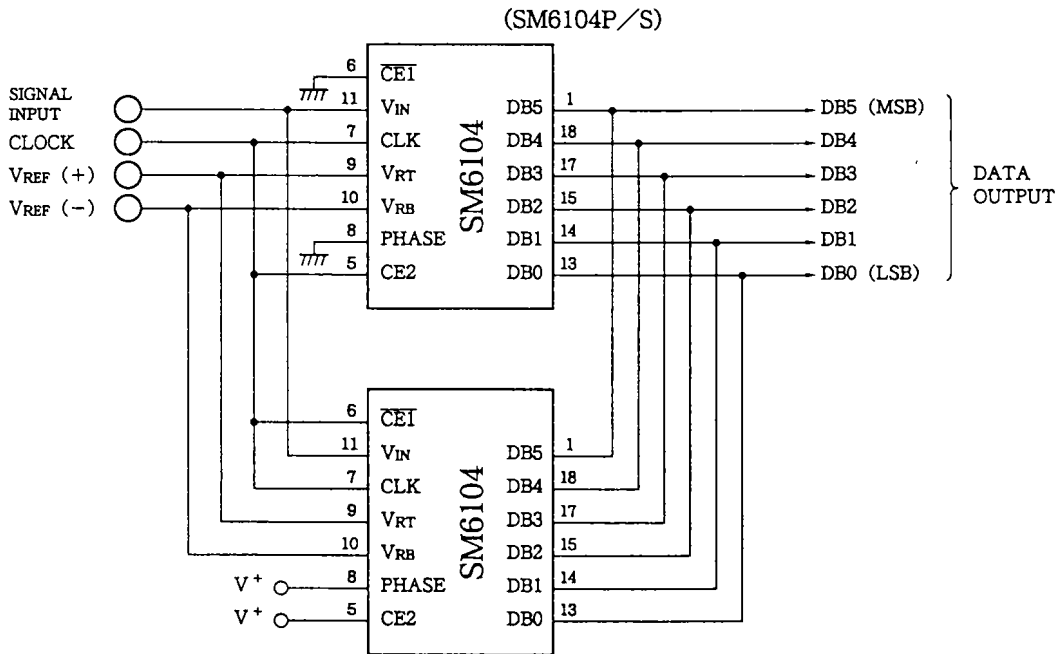
• The analog input voltages shown in this table are the center voltages of each step. Adjust  $V_{RT}$  and  $V_{RB}$  so that the zero transition voltage is 0.02 V, and the full-scale voltage is 2.50 V.

■ APPLICATION CIRCUITS

1. 7-bit resolution



2. 6-bit resolution 40MHz sampling (SM6104P/S)



\* USAGE NOTES

1. Use appropriately stabilized supplies for the power supply and reference voltages, and be sure to use tantalum and ceramic bypass capacitors.
2. Use a single-point earth for the system ground.
3. Ensure that digital noise is not fed through to the analog input. For example, design the circuit board layout so that both sides of the analog input are shielded by AGND.
4. The SM6104 uses CMOS chopper comparators. Since the analog input is alternately connected and disconnected to the input capacitance of the chopper, it must be driven from a low-impedance buffer. Using buffer amplifier is preferable.