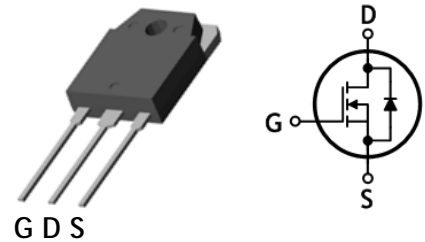


SWITCHING REGULATOR APPLICATION

Features

- Drain-Source breakdown voltage: $V_{DSS}=900V$ (Min.)
- Low gate charge: $Q_g=52nC$ (Typ.)
- Low drain-source On resistance: $R_{DS(on)}=1.4\Omega$ (Max.)
- 100% avalanche tested
- RoHS compliant device

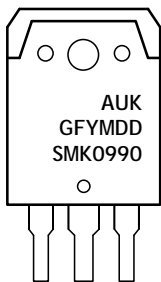


Ordering Information

Part Number	Marking	Package
SMK0990CI	SMK0990	TO-3P

TO-3P

Marking Information



Column 1: Manufacturer
 Column 2: Production Information
 e.g.) GFYMDD
 -. G: Option Code (H: Halogen Free)
 -. F: Factory Management Code
 -. YMDD: Date Code (Year, Month, Date)
 Column 3: Device Code

Absolute maximum ratings ($T_c=25^\circ C$ unless otherwise noted)

Characteristic	Symbol	Rating	Unit	
Drain-source voltage	V_{DSS}	900	V	
Gate-source voltage	V_{GSS}	± 30	V	
Drain current (DC) *	I_D	$T_c=25^\circ C$	9	A
		$T_c=100^\circ C$	5.7	A
Drain current (Pulsed) *	I_{DM}	36	A	
Single pulsed avalanche energy ^(Note 2)	E_{AS}	900	mJ	
Repetitive avalanche current ^(Note 1)	I_{AR}	9	A	
Repetitive avalanche energy ^(Note 1)	E_{AR}	13	mJ	
Power dissipation	P_D	130	W	
Junction temperature	T_J	150	$^\circ C$	
Storage temperature range	T_{stg}	-55-150	$^\circ C$	

* Limited only maximum junction temperature

Thermal Characteristics

Characteristic	Symbol	Rating	Unit
Thermal resistance, junction to case	$R_{th(j-c)}$	Max. 0.96	°C/W
Thermal resistance, junction to ambient	$R_{th(j-a)}$	Max. 40	

Electrical Characteristics ($T_c=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0$	900	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$I_D=250\mu\text{A}$, $V_{DS}=V_{GS}$	3	-	5	V
Drain-source cut-off current	I_{DSS}	$V_{DS}=900\text{V}$, $V_{GS}=0\text{V}$	-	-	1	μA
		$V_{DS}=720\text{V}$, $T_c=125^\circ\text{C}$	-	-	100	μA
Gate leakage current	I_{GSS}	$V_{DS}=0\text{V}$, $V_{GS}=\pm 30\text{V}$	-	-	± 100	nA
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=4.5\text{A}$	-	1.12	1.4	Ω
Forward transfer conductance (Note 4)	g_{fs}	$V_{DS}=10\text{V}$, $I_D=4.5\text{A}$	-	9.2	-	S
Input capacitance	C_{iss}	$V_{DS}=25\text{V}$, $V_{GS}=0\text{V}$, $f=1.0\text{MHz}$	-	2100	-	pF
Output capacitance	C_{oss}		-	175	-	
Reverse transfer capacitance	C_{rss}		-	14	-	
Turn-on delay time (Note 4,5)	$t_{d(on)}$	$V_{DD}=450\text{V}$, $I_D=9\text{A}$, $R_G=25\Omega$	-	50	-	ns
Rise time (Note 4,5)	t_r		-	120	-	
Turn-off delay time (Note 4,5)	$t_{d(off)}$		-	100	-	
Fall time (Note 4,5)	t_f		-	75	-	
Total gate charge (Note 4,5)	Q_g	$V_{DS}=720\text{V}$, $V_{GS}=10\text{V}$, $I_D=9\text{A}$	-	52	68	nC
Gate-source charge (Note 4,5)	Q_{gs}		-	16	-	
Gate-drain charge (Note 4,5)	Q_{gd}		-	20	-	

Source-Drain Diode Ratings and Characteristics ($T_c=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Source current (DC)	I_S	Integral reverse diode in the MOSFET	-	-	9	A
Source current (Pulsed)	I_{SM}		-	-	36	A
Forward voltage	V_{SD}	$V_{GS}=0\text{V}$, $I_S=9.5\text{A}$	-	-	1.4	V
Reverse recovery time (Note 4,5)	t_{rr}	$I_S=9\text{A}$, $V_{GS}=0\text{V}$ $di_F/dt=100\text{A}/\mu\text{s}$	-	550	-	ns
Reverse recovery charge (Note 4,5)	Q_{rr}		-	6.5	-	μC

Note:

1. Repeated rating: Pulse width limited by safe operating area
2. $L=21\text{mH}$, $I_{AS}=9\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\Omega$, Starting $T_J=25^\circ\text{C}$
3. Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$
4. Essentially independent of operating temperature typical characteristics

Electrical Characteristics Curve

Fig. 1 $I_D - V_{DS}$

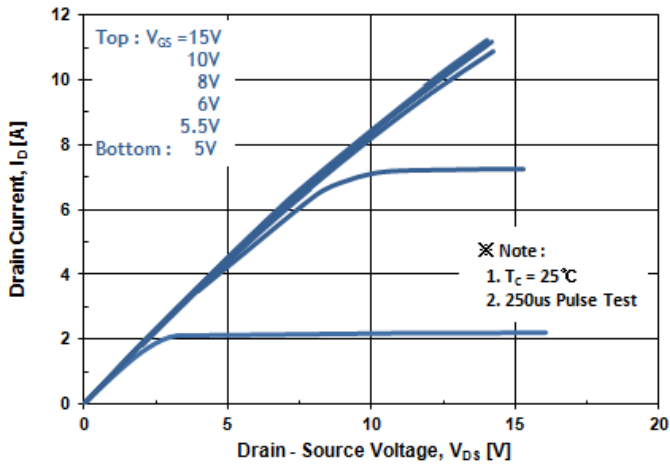


Fig. 2 $I_D - V_{GS}$

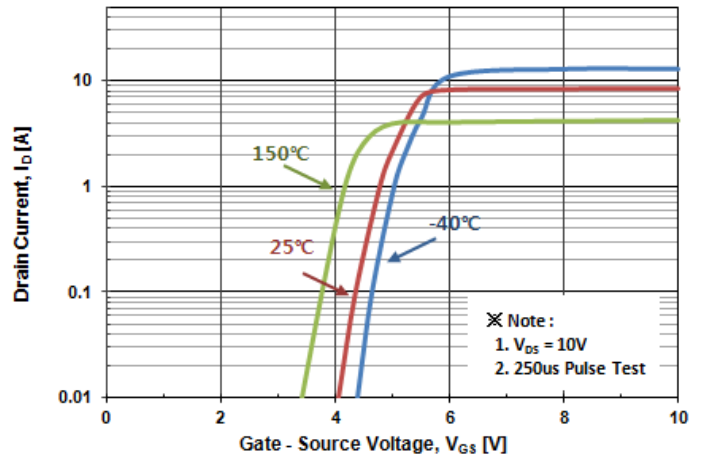


Fig. 3 $R_{DS(ON)} - I_D$

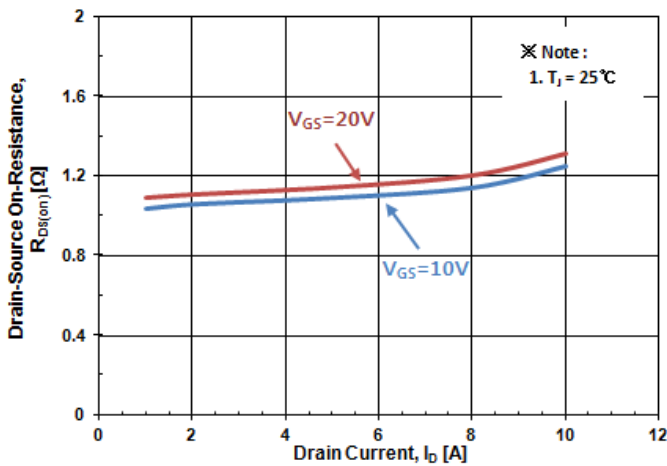


Fig. 4 $I_S - V_{SD}$

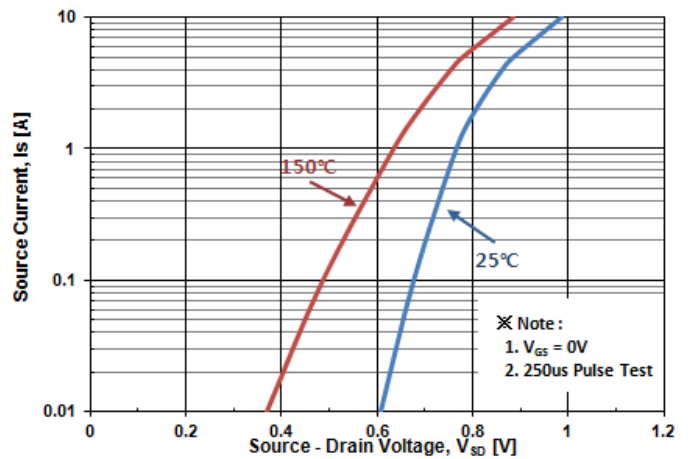


Fig. 5 Capacitance - V_{DS}

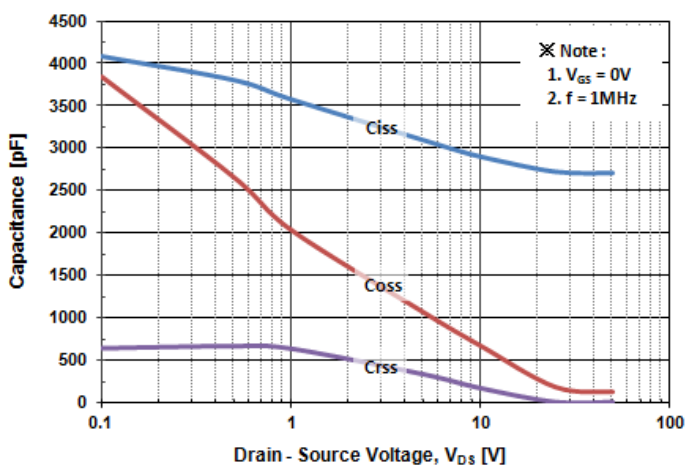
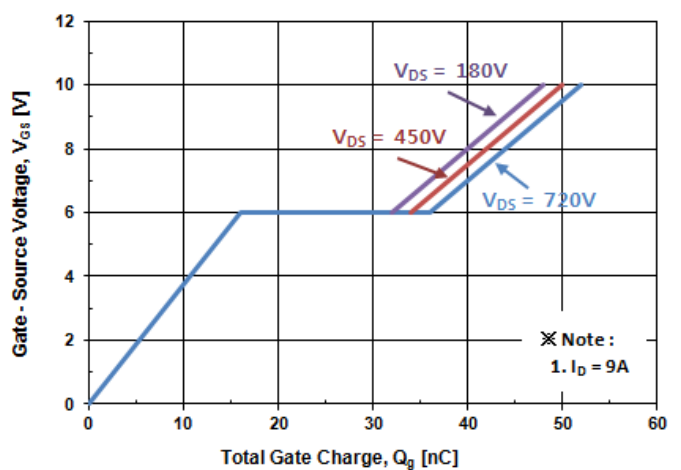


Fig. 6 $V_{GS} - Q_G$



Electrical Characteristics Curve (Continue)

Fig. 7 $BV_{DSS} - T_J$

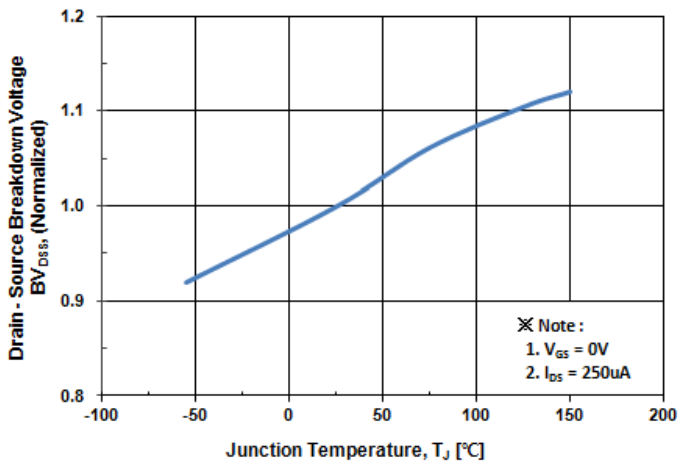


Fig. 8 $R_{DS(ON)} - T_J$

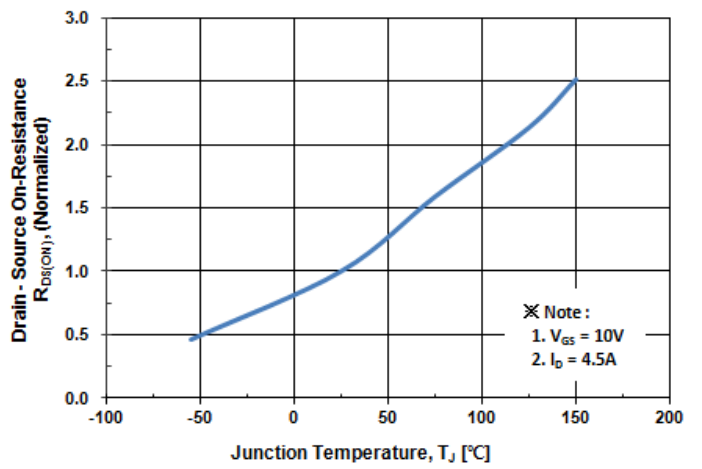


Fig. 9 $I_D - T_C$

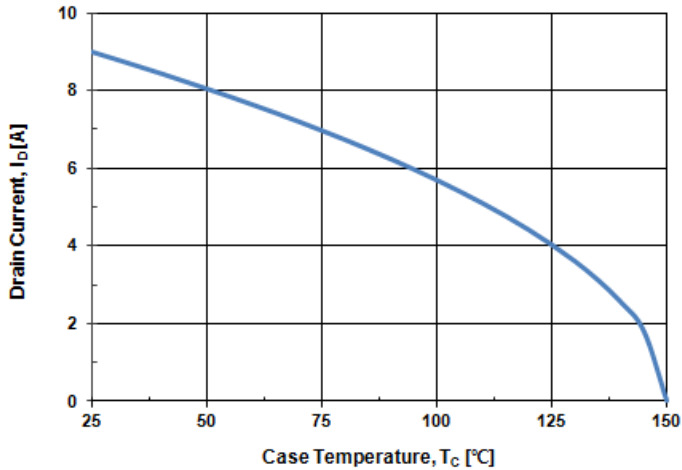


Fig. 10 Safe Operating Area

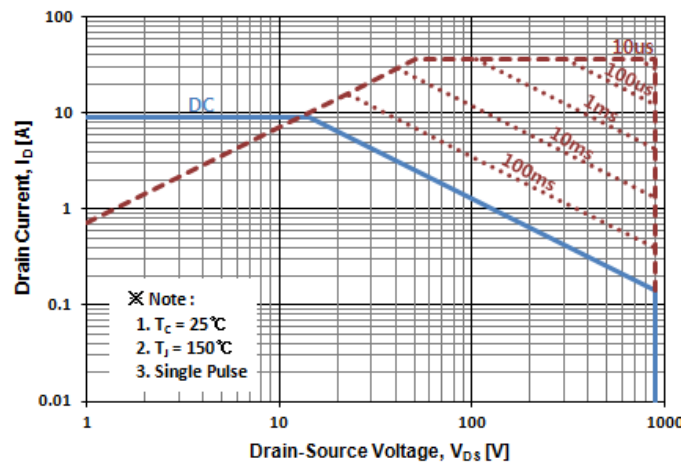


Fig. 11 Transient Thermal Impedance

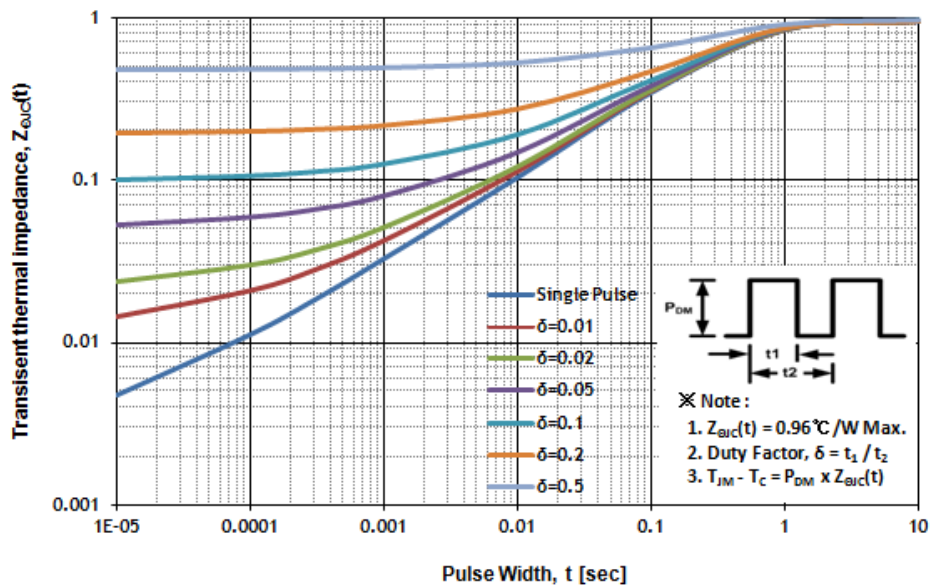


Fig. 12 Gate Charge Test Circuit & Waveform

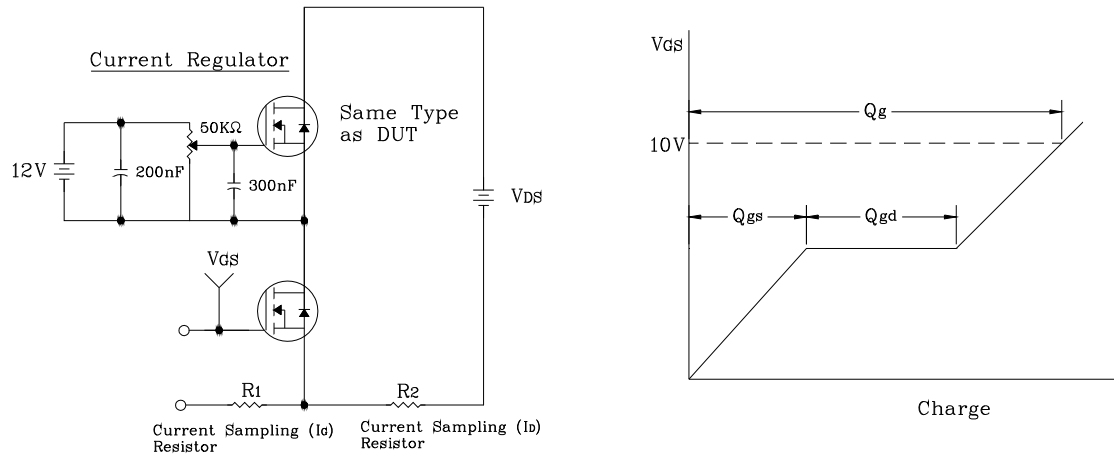


Fig. 13 Resistive Switching Test Circuit & Waveform

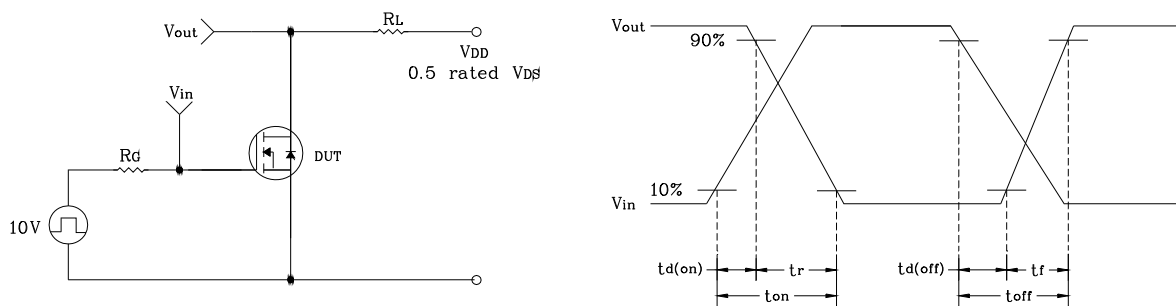


Fig. 14 E_{AS} Test Circuit & Waveform

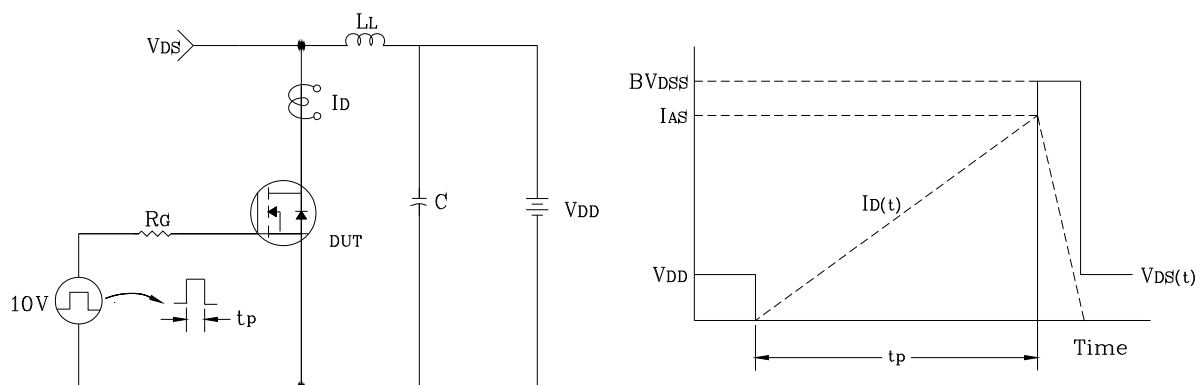
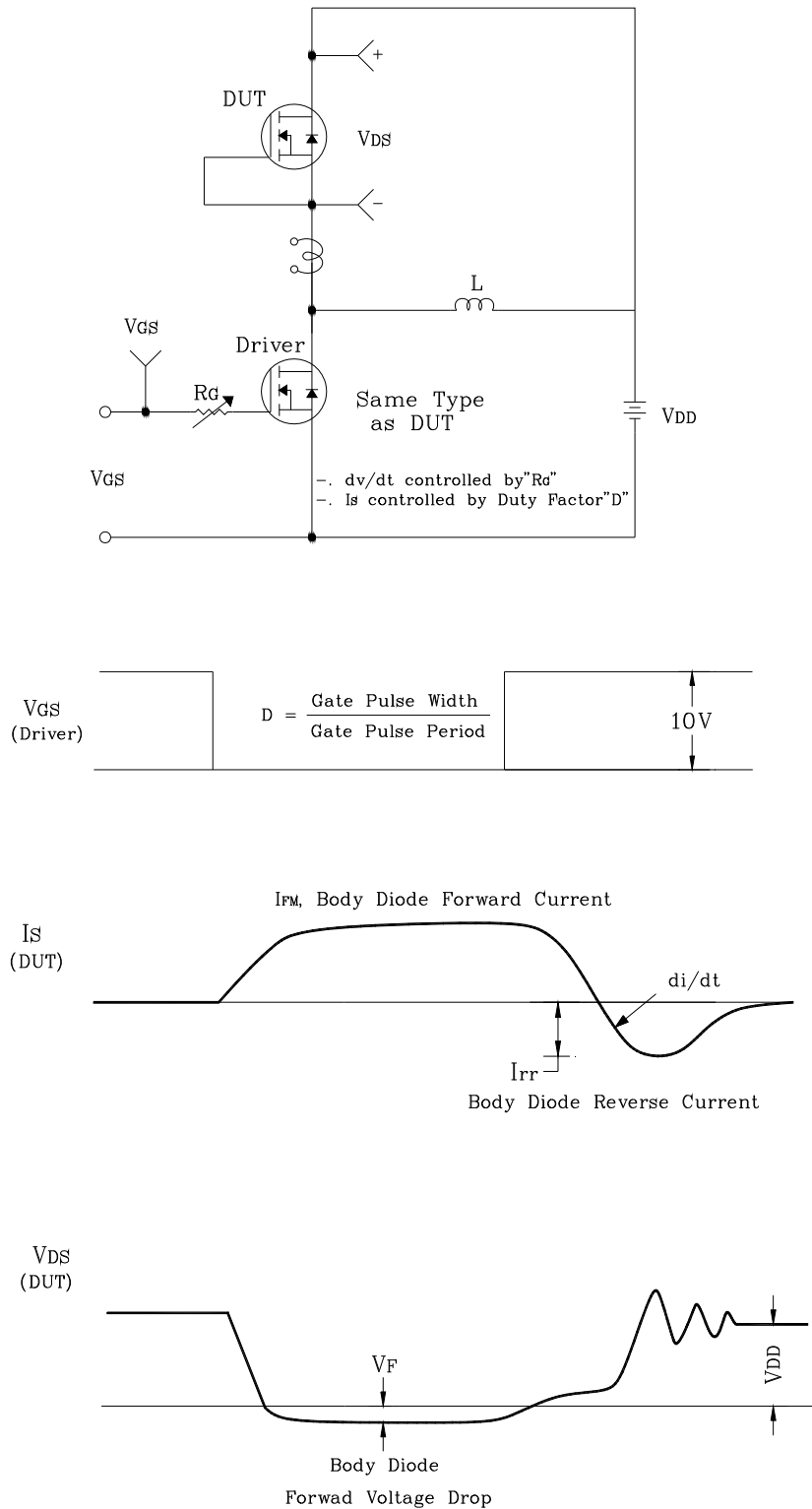
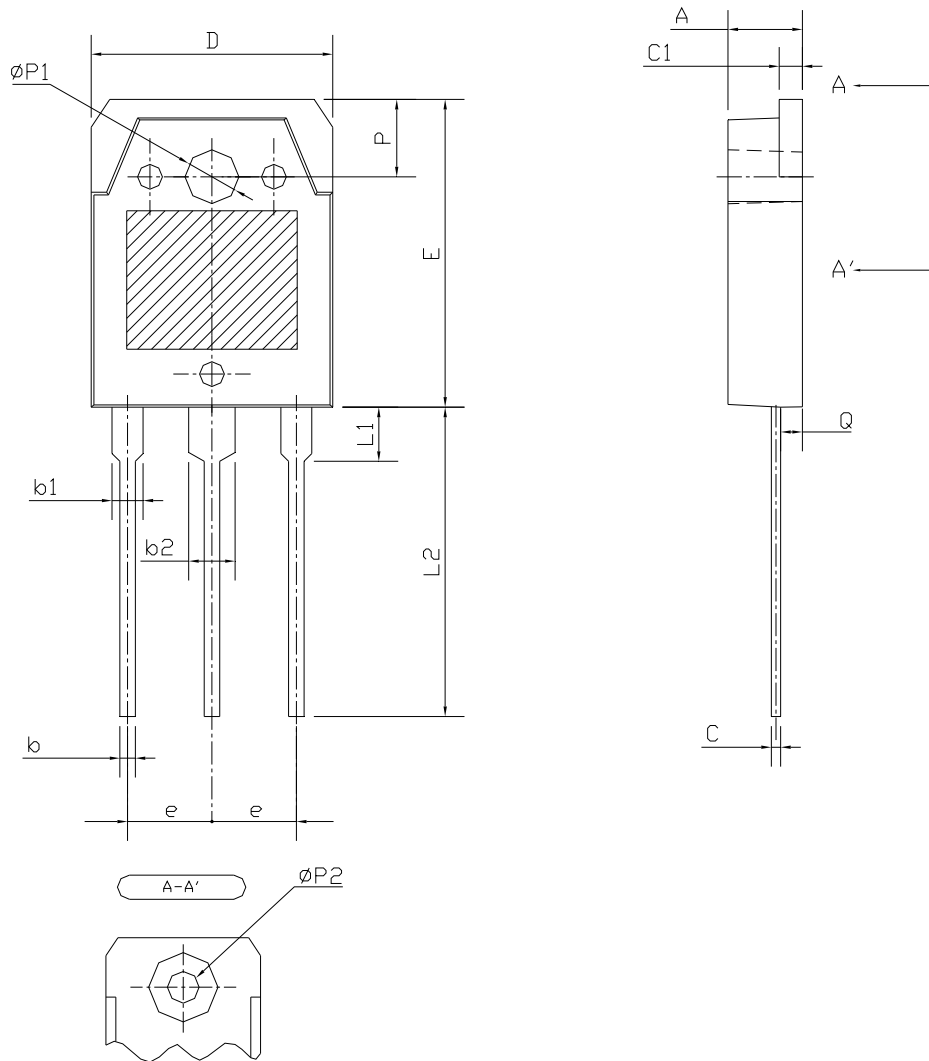


Fig. 15 Diode Reverse Recovery Time Test Circuit & Waveform



Package Outline Dimensions



SYMBOL	MIN	NOM	MAX
A	4.60	4.80	5.00
b	0.80	1.00	1.20
b1	1.80	2.00	2.20
b2	2.80	3.00	3.20
C	0.55	0.60	0.75
C1	1.45	1.50	1.65
D	15.40	15.60	15.80
E	19.70	19.90	20.10
e	5.15	5.45	5.75
L1	3.30	3.50	3.70
L2	19.80	20.00	20.20
P	4.80	5.00	5.20
$\phi P1$	3.30	3.40	3.50
$\phi P2$	(3.20)		
Q	1.20	1.40	1.60

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