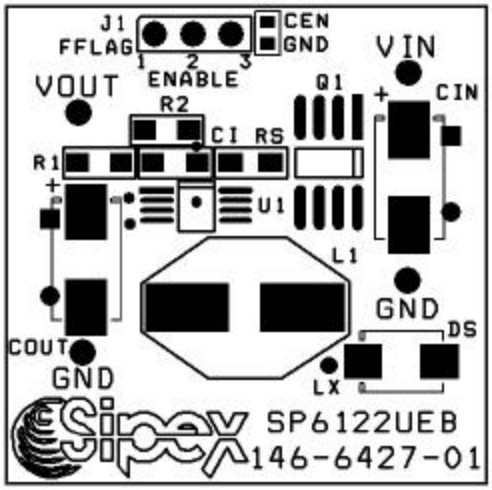
SP6122
Evaluation Board Manual

- Easy Evaluation for the SP6122 Low Voltage PFET Buck Converter
- Ideal for 1A to 5A, Small Footprint, DC-DC Power Converters
- Very Accurate 1.5% Reference over Line, Load, Temperature
- Small Micro 8 Package



DESCRIPTION

The **SP6122 Evaluation Board** is designed to help the user evaluate the performance of the SP6122 for use as a low voltage input, low voltage output PFET Buck DC-DC Controller. The SP6122 operates from a 5V or 3.3V input supply, and delivers output voltages as low as 1.5V with an accuracy of 1.5% over line, load and temperature. Unlike other "Micro-8" parts, the SP6122 has an array of value added features for you to evaluate including: optional hiccup mode, over-current protection and fault flag output.

The evaluation board is a completely assembled and tested surface mount power supply board which provides easy access to the SP6122 Input and Outputs so that the user can quickly measure electrical characteristics and waveforms.

The next two sections describe the SP6122 Board Layout and Using the SP6122 Evaluation Boards. A section on SP6122 Power Supply Data is also included with graphs on Efficiency, Line and Load Regulation. Then, drawings of the PC Layout and a schematic are included as a design-in tool for the user of the SP6122. Finally, a SP6122 Evaluation Board List of Materials table is provided with some manufacturers part numbers to use as a reference.

BOARD LAYOUT

The **SP6122 Evaluation Board** has been designed for quick and easy connection to the Input and Output of the SP6122 Power Supply under test. Position the board with the silkscreen lettering upright, (also see the drawing on the front page of this manual) and you will see U1 the SP6122 8-pin µSOIC, in the center left of the board. To the left of U1 are the output capacitor Cout and the Vout pin. To the right of U1 are Q1 and the Vin post and the input capacitor Cin. Below Cin and Cout are the two GND posts.

USING THE EVALUATION BOARD

1) Powering Up the SP6122 Circuit

The SP6122 Evaluation Board can be powered from inputs from a +3V to +7V power supply. Connect with short leads directly to the "Vin" and "Gnd" posts. Monitor the Output Voltage and connect the Load between the "Vout" post and the 2nd "GND" post.

2) Using the J1 Jumper: Enabling the SP6122 Output and using the Hiccup Mode

As you can see in table 1, the SP6122 output will be Enabled if the J1 Jumper is left open. If J1 is in the pin 2 to 3 position, the ENABLE pin is brought to GND, which puts the SP6122 in the Sleep Mode. If the Jumper at J1 is in the pin 1 to 2 position, FFLAG U1 pin 2 is connected to ENABLE U1 pin 4, and Hiccup Mode is activated. Hiccup Mode occurs if the output current exceeds the Over-Current-Protection threshold, and the part will "Soft-start", which happens every 1.2msec for a CEN capacitor value of 4.7nF. This is determined by the following relationship:

$I = CEN*dV/dt$ which yields $dt = CEN*dV/I = 1.2msec$

where the value of the CEN capacitor is 4.7nF, dV is the 1V internal threshold for charging, and I is the Enable pin source current of 4uA.

	SP6122	
J1 Position	Mode	Condition
open	Enabled	Normal
1 to 2	Hiccup	Softstarts if Over-Current
2 to 3	Sleep	Iq = 20uA (max)

Table 1. SP6122 Enable/Hiccup Jumper

3) Using External Divider Resistors: Programming the SP6122 Output Voltage

As you can see by the schematic in Figure 1, the SP6122 uses an internal feedback divider to initially trim the output voltage using Rin1 and Rin2, where Rin2 is approximately 62.5K. To accommodate the user who wants to externally program the SP6122 output voltage, the SP6122 Evaluation Board has 2 external divider resistors, R1 and R2, which can be used to program the output voltage above, but not below the voltage set by the internal resistor divider. The relationships for the external divider resistors are derived below:

$i1 = Va/Rin2 = 1.25/62.5K = 20uA$

Since Rin2 has +/-50% tolerance, ib change is +20uA/-7uA. If the SP6122 is trimmed to 1.5V output, Vb will be fixed at 1.5V in a closed loop. As a result, i2 is not affected by the variation of the internal resistors, and the +20uA/-7uA current variation will be passed on to i3.

$Vout = Vb+i3*R1,$
Therefore, $\Delta Vout = \Delta i3*R1=+20uA/-7uA*R1.$

That is, the additional variation on the output voltage is caused by the internal voltage divider. For example, with R1 selected to be 500ohm, the variation on the output voltage will be +10mV/-3.5mV.

SP612 Evaluation Board Divider Resistors: The values of R1 and R2 are selected to program 1.9V output, with 1.5V trim voltage Vb, and R1 = 500ohm:

i3 = (Vout-Vb)/R1=(1.9-1.5)/500 = 800uA.

The external voltage divider will add only 800uA to the load. **Divider Resistor R2 is:**

R2 = Vb/(i3-i1)=1.5/(800uA-20uA) = 1.9K

The user of the SP6122 Evaluation Board can use the above equations for i3 and R2 to modify R2 and change the output voltage to be any voltage from Vb (1.5V) to as high as the input voltage. And if you want the output voltage to be the preset voltage Vb (1.5V), just short a wire across R1.

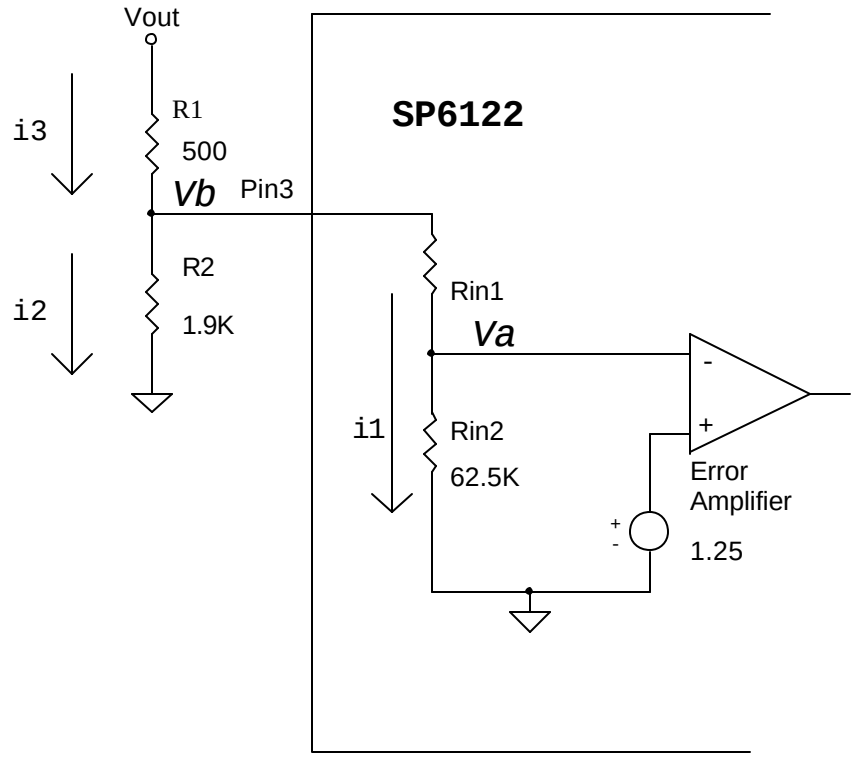


Figure 1. Schematic: Output Voltage Divider Resistors

POWER SUPPLY DATA

The SP6122 is engineered for size and minimum pin count, yet has a very accurate 1.5% reference over line, load and temperature. Figure 2 data shows a typical SP6122 Evaluation Board Efficiency plot, with efficiencies to 88% and output currents to 4A. Load Regulation plot in Figure 3 shows an essentially flat response of only 3mV change for up to 4A load. Figure 4 Line Regulation illustrates a 1.90V output that varies only 4mV or 0.2% for an input voltage change from 3.3V to 5.5V. While data on individual power supply boards may vary, the capability of the SP6122 of achieving high accuracy over load and line shown here is quite impressive and desirable for accurate power supply design.

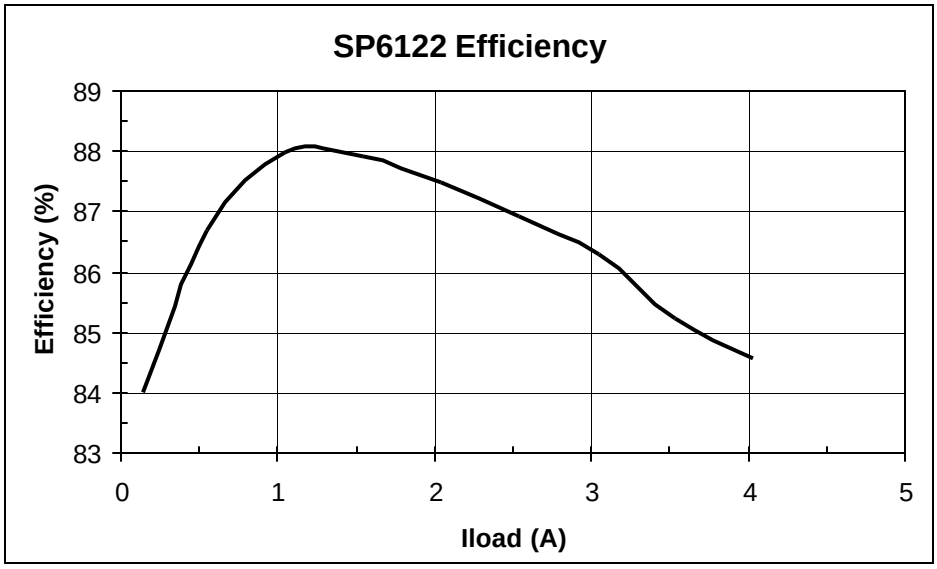


Figure 2. SP6122 Efficiency with Vin = 3.3V, Vout = 1.93V

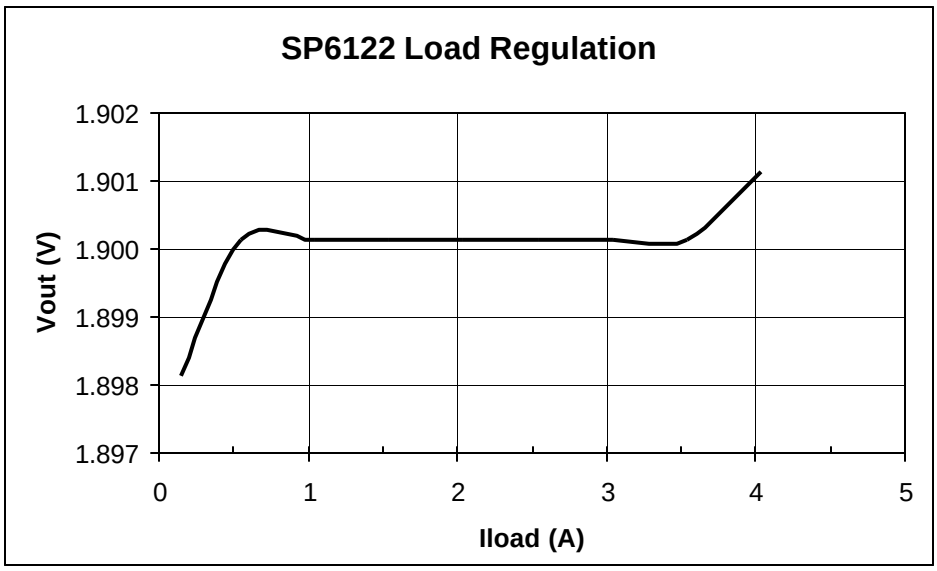


Figure 3. SP6122 Load Regulation with Input Voltage = 3.3V

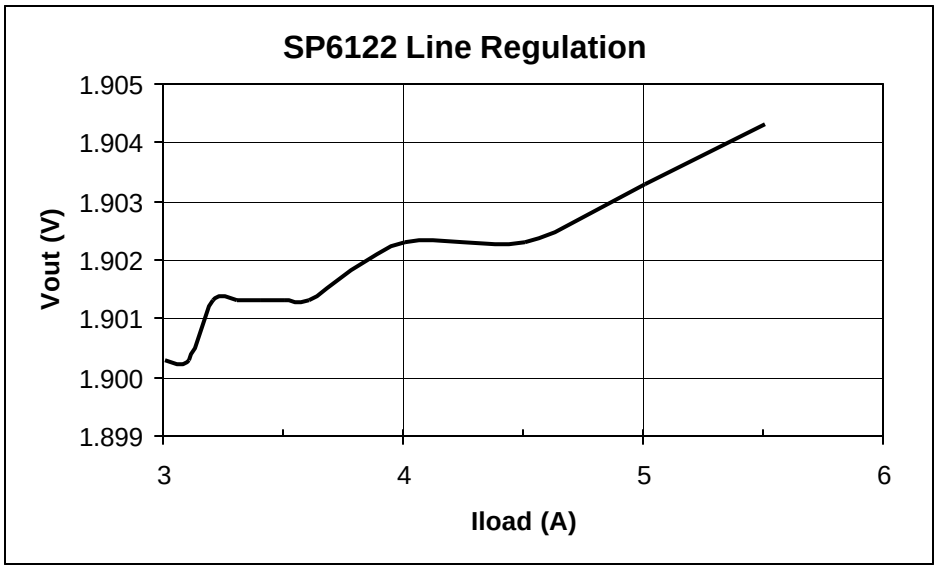


Figure 4. SP6122 Line Regulation with Iload = 2A

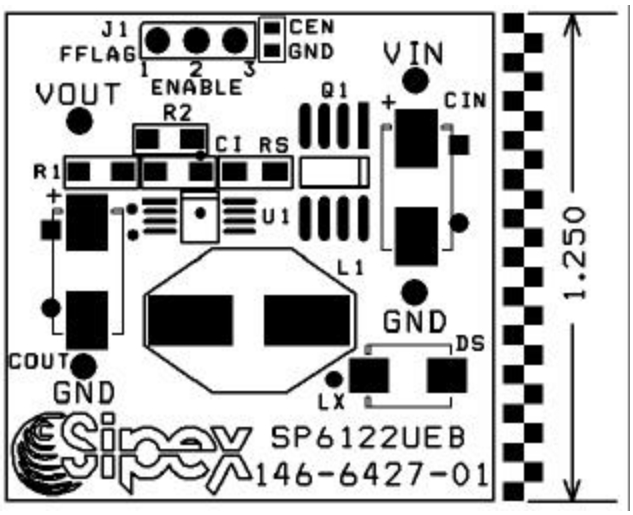


FIGURE 5: SP6122UEB COMPONENT PLACEMENT

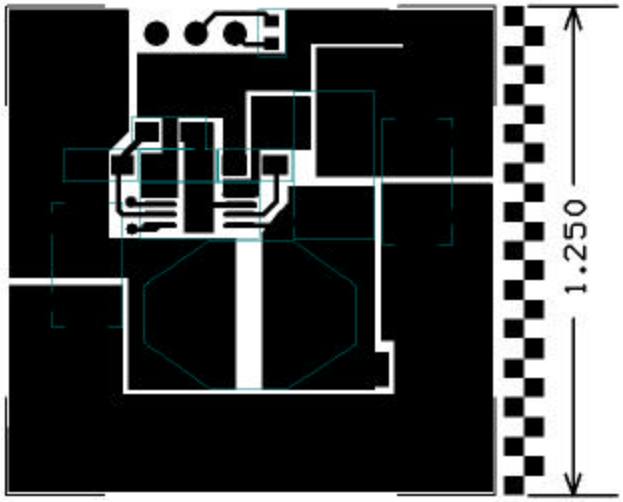


FIGURE 6: SP6122UEB PC LAYOUT TOP SIDE

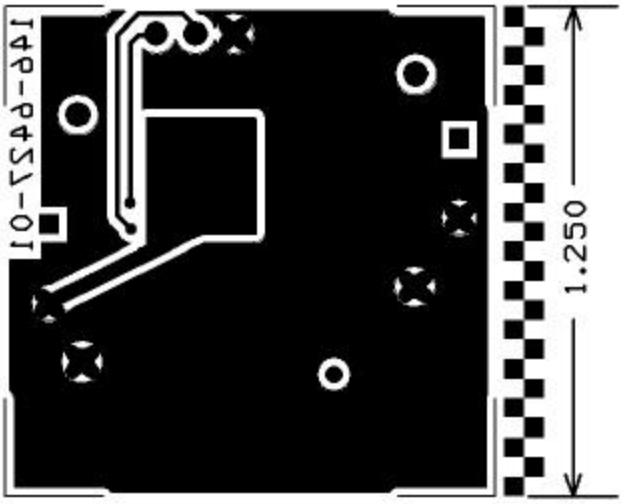


FIGURE 7: SP6122UEB PC LAYOUT BOTTOM SIDE

FIGURE 8: SP6122 EVALUATION BOARD SCHEMATIC

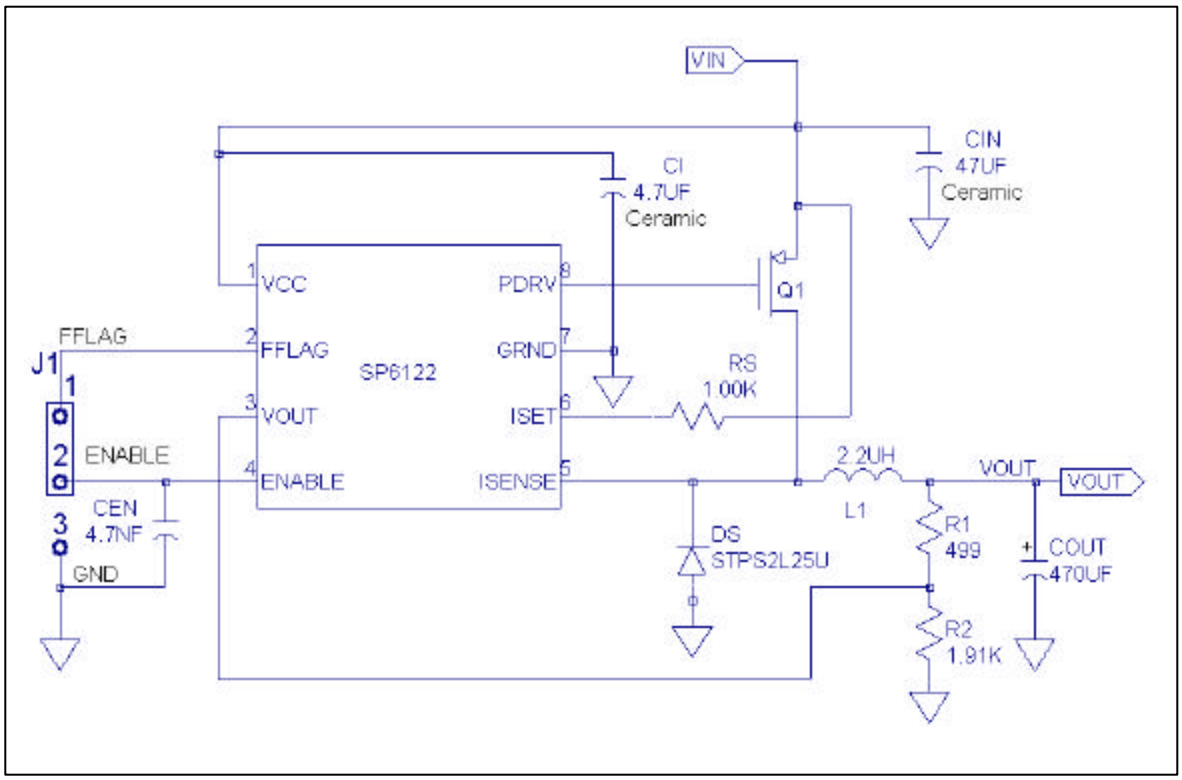


TABLE 2: SP6122EB LIST OF MATERIALS

Ref. Des.	Qty.	Manuf.	Manuf. Part Number	Layout Size	Component	Vendor Phone Number
PCB	1	Sipex	146-6427-00	1"X1.5"	SP6120 Eval PCB	978-667-7800
U1	1	Sipex	SP6122UEB	uSO-8	5A PFET Buck Ctrl	978-667-7800
Q1	1	Fairchild	FDS6375	SO-8	PFET	310-322-3331
DS	1	STMicroelectronics	STPS2L25U	SMB	2A Schottky 10A RMS	781-861-2650
L1	1	Coilcraft	DO3316P-222	12.9x9.4mm	2.2uH Coil 5A 0.012ohm	847-639-6400
CIN	1	TDK	C4532X5R0J476M	1812	47uF Ceramic SM 6.3V	847-803-6100
COUT	1	Sanyo	6TPB470M	7343H	470uF 6.3V 0.035ohm	978-922-6573
CI	1	TDK	C3216X5R1C475K	1206	4.7uF 10V SM X5R	847-803-6100
CEN	1	Panasonic	ECJ-1VB1H472K	0603	4700pF Ceramic X7R 50V	800-DIGI-KEY
R1	1	Panasonic	ERJ-8ENF5000V	1206	500 OHM Thick Film Res 1%	800-DIGI-KEY
R2	1	Panasonic	ERJ-8ENF1911V	1206	1.91K OHM Thick Film Res 1%	800-DIGI-KEY
RS	1	Panasonic	ERJ-8ENF1001V	1206	1.00K OHM Thick Film Res 1%	800-DIGI-KEY

ORDERING INFORMATION

Part Number	Package Type
SP6122UEB	SP6122 Evaluation Board
SP6122CU	8-pin µSOIC

