

SRDA05-4R2

Low Capacitance Surface Mount TVS for High-Speed Data Interfaces

The SRDA05-4 transient voltage suppressor is designed to protect equipment attached to high speed communication lines from ESD, EFT, and lightning.

Features:

- SO-8 Package
- Peak Power – 500 Watts 8 x 20 μ S
- ESD Rating:
IEC 61000-4-2 (ESD) 15 kV (air) 8 kV (contact)
IEC 61000-4-4 (EFT) 40 A (5/50 ns)
IEC 61000-4-5 (lightning) 23 (8/20 μ s)
- UL Flammability Rating of 94 V-0

Typical Applications:

- High Speed Communication Line Protection

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Power Dissipation 8 x 20 μ S @ $T_A = 25^\circ\text{C}$ (Note 1)	P_{pk}	500	W
Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$
Lead Solder Temperature – Maximum 10 Seconds Duration	T_L	260	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Non-repetitive current pulse 8 x 20 μ S exponential decay waveform

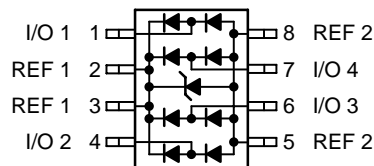


ON Semiconductor®

<http://onsemi.com>

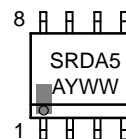
SO-8 LOW CAPACITANCE VOLTAGE SUPPRESSOR 500 WATTS PEAK POWER 6 VOLTS

PIN CONFIGURATION AND SCHEMATIC



**SO-8
CASE 751
PLASTIC**

MARKING DIAGRAM



SRDA5 = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
SRDA05-4R2	SO-8	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS

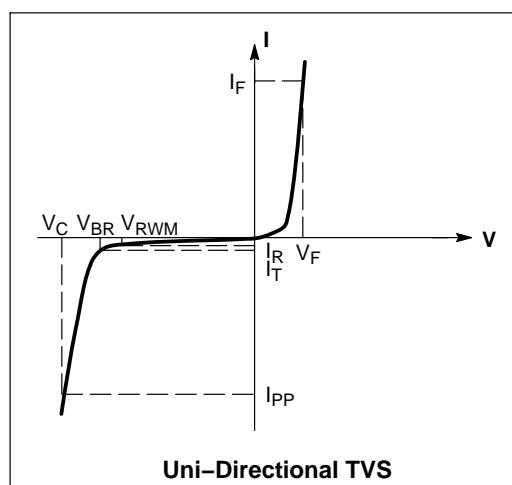
Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage @ $I_T = 1.0 \text{ mA}$	V_{BR}	6.0	-	-	V
Reverse Leakage Current @ $V_{RWM} = 5.0 \text{ Volts}$	I_R	N/A	-	10	μA
Maximum Clamping Voltage @ $I_{PP} = 1.0 \text{ A}, 8 \times 20 \mu\text{S}$	V_C	N/A	-	9.8	V
Maximum Clamping Voltage @ $I_{PP} = 10 \text{ A}, 8 \times 20 \mu\text{S}$	V_C	N/A	-	12	V
Between I/O Pins and Ground @ $V_R = 0 \text{ Volts}, 1.0 \text{ MHz}$	Capacitance	-	10	15	pF
Between I/O Pins @ $V_R = 0 \text{ Volts}, 1.0 \text{ MHz}$	Capacitance	-	5	8	pF

ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

UNIDIRECTIONAL (Circuit tied to Pins 1 and 3 or 2 and 3)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
ΘV_{BR}	Maximum Temperature Coefficient of V_{BR}
I_F	Forward Current
V_F	Forward Voltage @ I_F
Z_{ZT}	Maximum Zener Impedance @ I_{ZT}
I_{ZK}	Reverse Current
Z_{ZK}	Maximum Zener Impedance @ I_{ZK}



TYPICAL CHARACTERISTICS

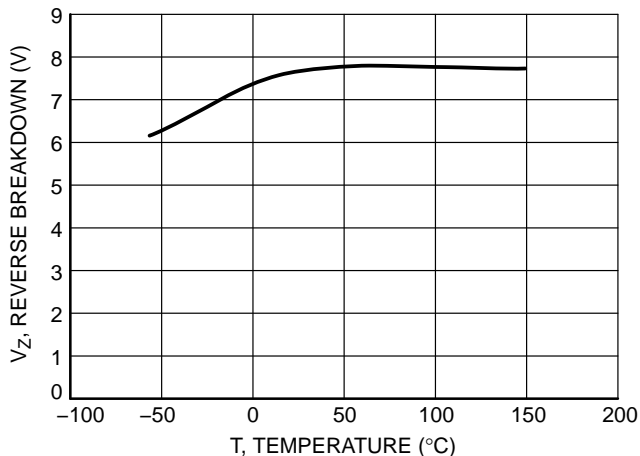


Figure 1. Reverse Breakdown versus Temperature

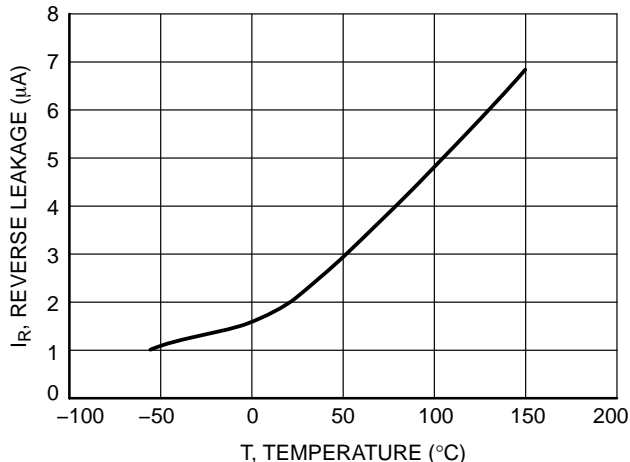


Figure 2. Reverse Leakage versus Temperature

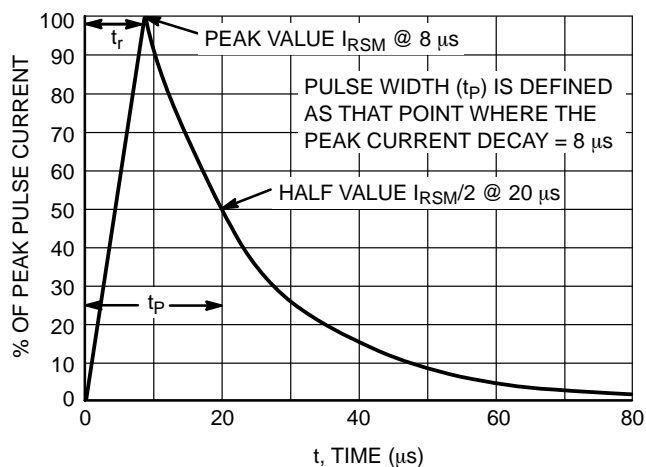


Figure 3. 8 x 20 μs Pulse Waveform

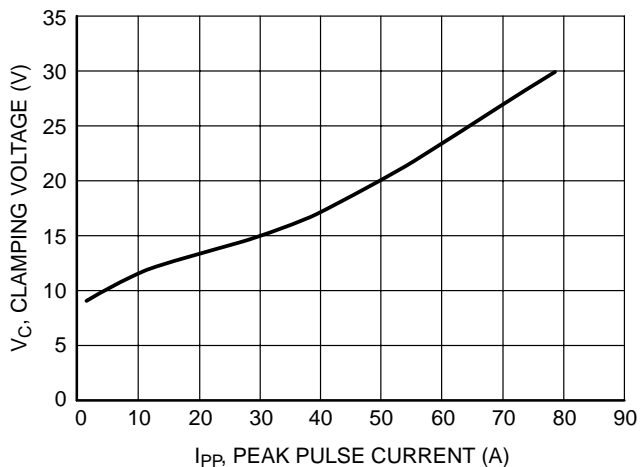


Figure 4. Clamping Voltage versus Peak Pulse Current

APPLICATIONS INFORMATION

The SRDA05-4R2 is a low capacitance TVS diode array designed to protect sensitive electronics such as communications systems, computers, and computer peripherals against damage due to ESD events or transient overvoltage conditions. Because of its low capacitance, it can be used in high speed I/O data lines. The integrated design of the SRDA05-4R2 offers surge rated, low capacitance steering diodes and a TVS diode integrated in a single package (SO-8). If a transient condition occurs, the steering diodes will drive the transient to the positive rail of the power supply or to ground. The TVS device protects the power line against overvoltage conditions avoiding damage to the power supply and other downstream components.

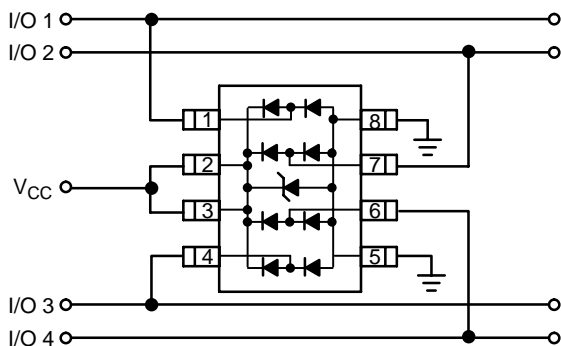
SRDA05-4R2 Configuration Options

The SRDA05-4R2 is able to protect up to four data lines against transient overvoltage conditions by driving them to a fixed reference point for clamping purposes. The steering diodes will be forward biased whenever the voltage on the protected line exceeds the reference voltage (V_f or $V_{cc}+V_f$). The diodes will force the transient current to bypass the sensitive circuit.

Data lines are connected at pins 1, 4, 6 and 7. The negative reference is connected at pins 5 and 8. These pins must be connected directly to ground using a ground plane to minimize the PCB's ground inductance. It is very important to reduce the PCB trace lengths as much as possible to minimize parasitic inductances.

Option 1

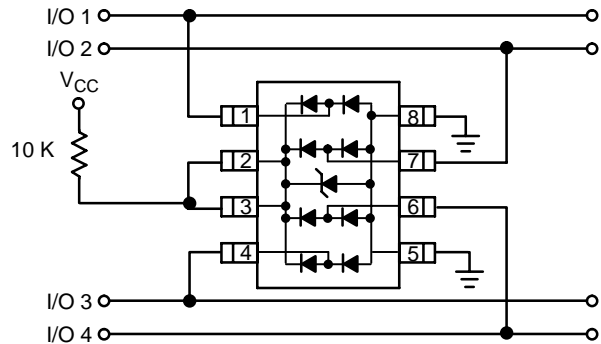
Protection of four data lines and the power supply using V_{cc} as reference.



For this configuration, connect pins 2 & 3 directly to the positive supply rail (V_{cc}). The data lines are referenced to the supply voltage. The internal TVS diode prevents overvoltage on the supply rail. Biasing of the steering diodes reduces their capacitance.

Option 2

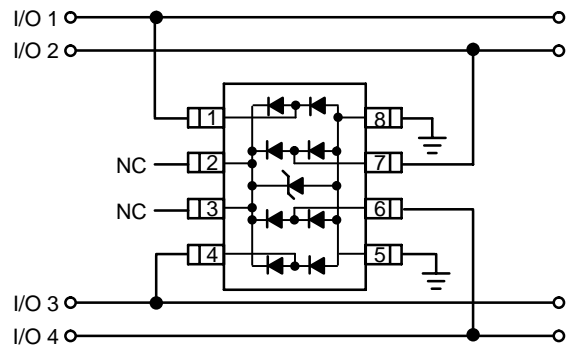
Protection of four data lines with bias and power supply isolation resistor.



The SRDA05-4R2 can be isolated from the power supply by connecting a series resistor between pins 2 & 3 and V_{cc} . A 10 k Ω resistor is recommended for this application. This will maintain a bias on the internal TVS and steering diodes, reducing their capacitance.

Option 3

Protection of four data lines using the internal TVS diode as reference.

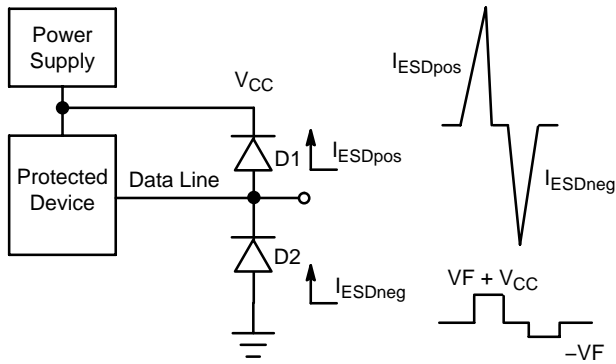


In applications lacking a positive supply reference or those cases in which a fully isolated power supply is required, the internal TVS can be used as the reference. For these applications, pins 2 and 3 are not connected. In this configuration, the steering diodes will conduct whenever the voltage on the protected line exceeds the working voltage of the TVS plus one diode drop ($V_c = V_f + V_{TVS}$).

ESD Protection of Power Supply Lines

When using diodes for data line protection, referencing to a supply rail provides advantages. Biasing the diodes reduces their capacitance and minimizes signal distortion. Implementing this topology with discrete devices does have disadvantages. This configuration is shown below:

SRDA05-4R2



Looking at the figure above, it can be seen that when a positive ESD condition occurs, diode D1 will be forward biased while diode D2 will be forward biased when a negative ESD condition occurs. For slower transient conditions, this system may be approximated as follows:

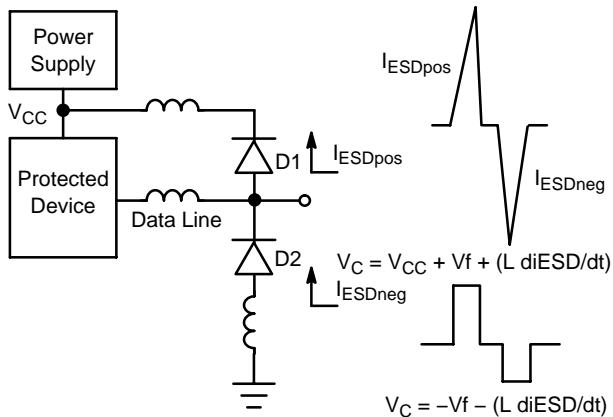
For positive pulse conditions:

$$V_c = V_{CC} + V_{fD1}$$

For negative pulse conditions:

$$V_c = -V_{fD2}$$

ESD events can have rise times on the order of some number of nanoseconds. Under these conditions, the effect of parasitic inductance must be considered. A pictorial representation of this is shown below.



An approximation of the clamping voltage for these fast transients would be:

For positive pulse conditions:

$$V_c = V_{CC} + V_f + (L \, di_{ESD}/dt)$$

For negative pulse conditions:

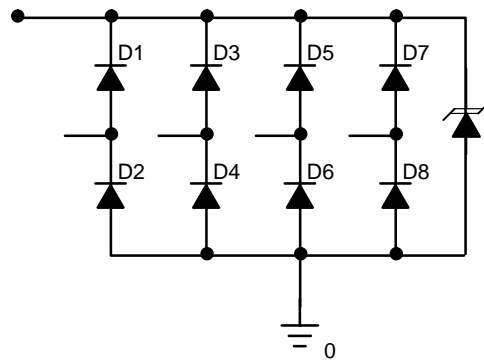
$$V_c = -V_f - (L \, di_{ESD}/dt)$$

As shown in the formulas, the clamping voltage (V_c) not only depends on the V_f of the steering diodes but also on the $L \, di_{ESD}/dt$ factor. A relatively small trace inductance can result in hundreds of volts appearing on the supply rail. This endangers both the power supply and anything attached to that rail. This highlights the importance of good board layout. Taking care to minimize the effects of parasitic

inductance will provide significant benefits in transient immunity.

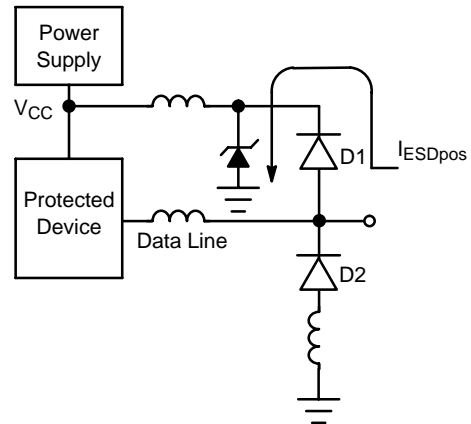
Even with good board layout, some disadvantages are still present when discrete diodes are used to suppress ESD events across datalines and the supply rail. Discrete diodes with good transient power capability will have larger die and therefore higher capacitance. This capacitance becomes problematic as transmission frequencies increase. Reducing capacitance generally requires reducing die size. These small die will have higher forward voltage characteristics at typical ESD transient current levels. This voltage combined with the smaller die can result in device failure.

The ON Semiconductor SRDA05-4R2 was developed to overcome the disadvantages encountered when using discrete diodes for ESD protection. This device integrates a TVS diode within a network of steering diodes.



SRDA05-4R2 Equivalent Circuit

During an ESD condition, the ESD current will be driven to ground through the TVS diode as shown below.



The resulting clamping voltage on the protected IC will be:

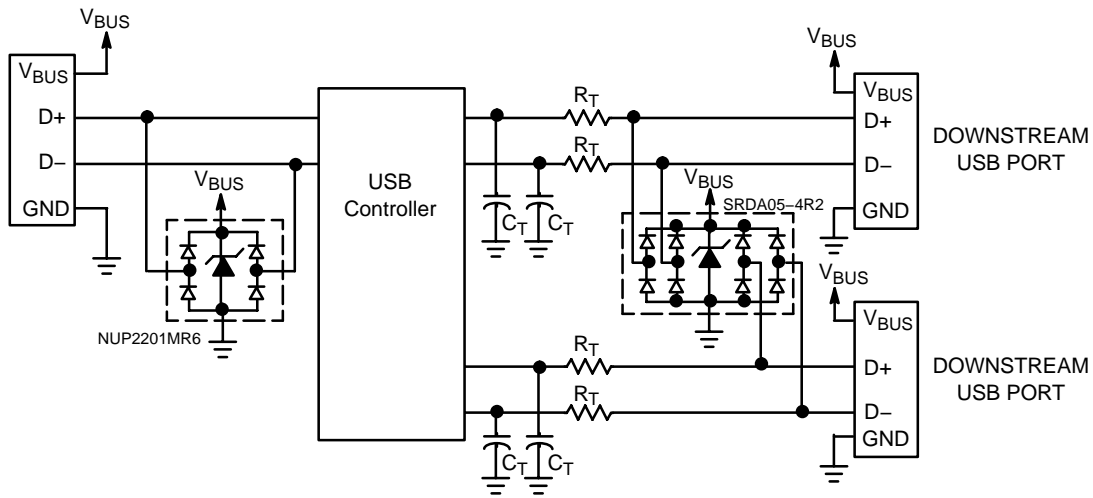
$$V_c = V_{fD1} + V_{TVS}$$

The clamping voltage of the TVS diode is provided in Figure 4 and depends on the magnitude of the ESD current. The steering diodes are fast switching devices with unique forward voltage and low capacitance characteristics.

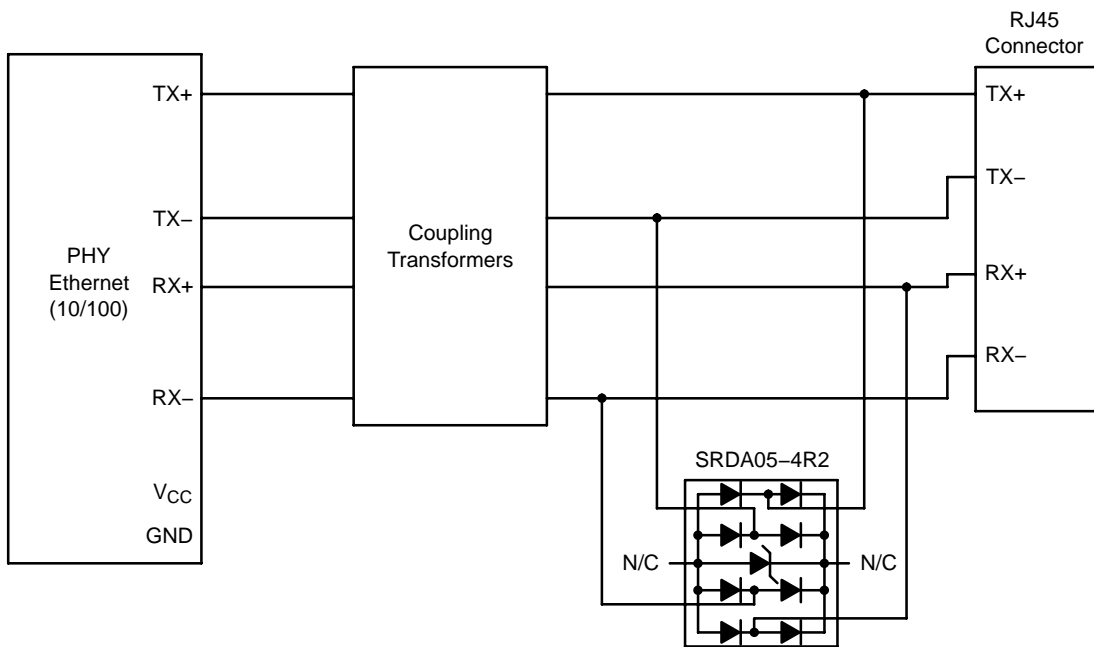
SRDA05-4R2

TYPICAL APPLICATIONS

UPSTREAM
USB PORT

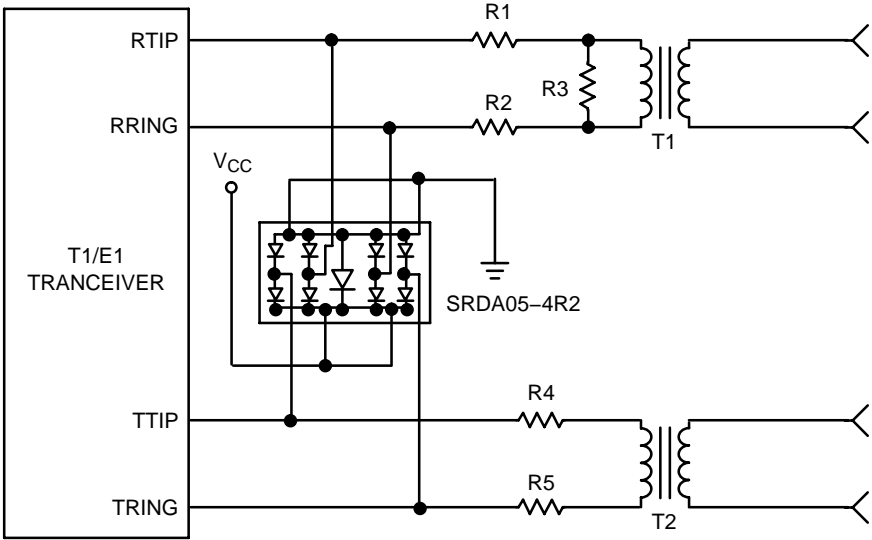


ESD Protection for USB Port



Protection for Ethernet 10/100 (Differential mode)

SRDA05-4R2

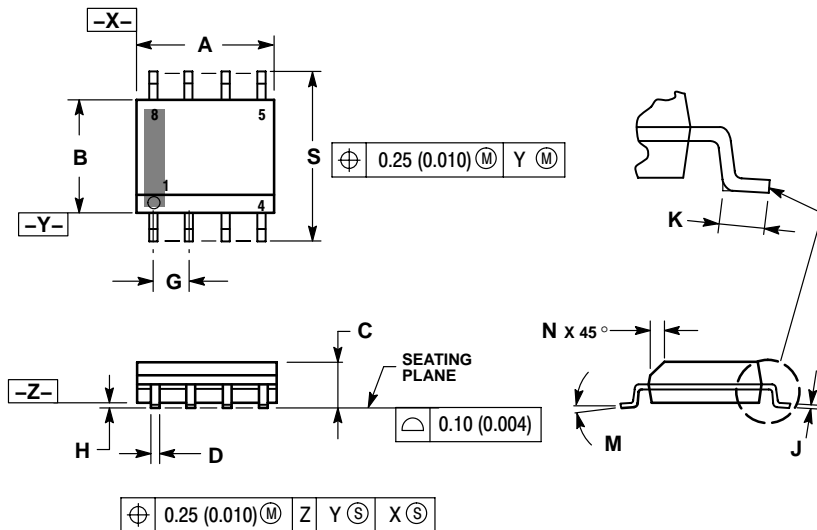


T1/E1 Interface Protection

SRDA05-4R2

PACKAGE DIMENSIONS

SO-8
CASE 751-07
ISSUE AG

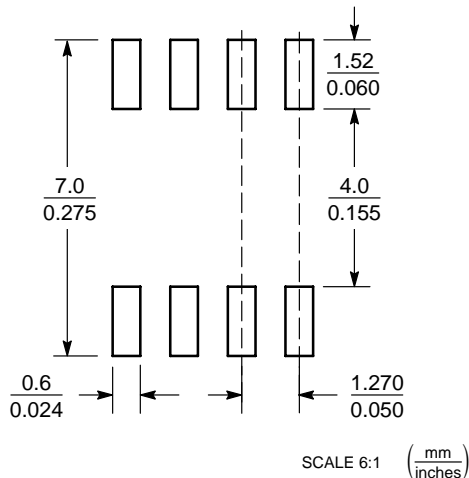


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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