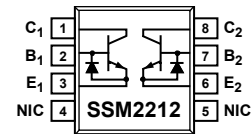


### FEATURES

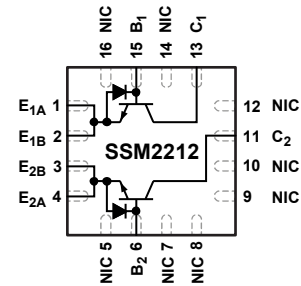
- Very low voltage noise: 1 nV/ $\sqrt{\text{Hz}}$  maximum at 100 Hz
- Excellent current gain match: 0.5%
- Low offset voltage ( $V_{OS}$ ): 200  $\mu\text{V}$  maximum (SOIC)
- Outstanding offset voltage drift: 0.03  $\mu\text{V}/^\circ\text{C}$
- High gain bandwidth product: 200 MHz

### PIN CONNECTIONS



NOTES  
1. NIC = NO INTERNAL CONNECTION.

Figure 1. 8-Lead SOIC\_N



NOTES  
1. NIC = NO INTERNAL CONNECTION.

Figure 2. 16-Lead LFCSP\_WQ

### GENERAL DESCRIPTION

The **SSM2212** is a dual, NPN-matched transistor pair that is specifically designed to meet the requirements of ultralow noise audio systems.

With its extremely low input base spreading resistance ( $r_{bb'}$  is typically 28  $\Omega$ ) and high current gain ( $h_{FE}$  typically exceeds 600 at  $I_C = 1 \text{ mA}$ ), the **SSM2212** can achieve outstanding signal-to-noise ratios. The high current gain results in superior performance compared to systems incorporating commercially available monolithic amplifiers.

Excellent matching of the current gain ( $\Delta h_{FE}$ ) to approximately 0.5% and low  $V_{OS}$  of less than 10  $\mu\text{V}$  typical make the **SSM2212** ideal for symmetrically balanced designs, which reduce high-order amplifier harmonic distortion.

Stability of the matching parameters is guaranteed by protection diodes across the base-emitter junction. These diodes prevent degradation of beta and matching characteristics due to reverse biasing of the base-emitter junction.

The **SSM2212** is also an ideal choice for accurate and reliable current biasing and mirroring circuits. Furthermore, because the accuracy of a current mirror degrades exponentially with mismatches of  $V_{BE}$  between transistor pairs, the low  $V_{OS}$  of the **SSM2212** does not need offset trimming in most circuit applications.

The **SSM2212** SOIC performance and characteristics are guaranteed over the extended temperature range of  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

The **SSM2212** is available in 8-lead SOIC and 16-lead LFCSP packages.

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## REVISION HISTORY

### 6/15—Rev. B to Rev. C

Added LFCSP Package.....	Universal
Changes to Features Section and General Description Section.....	1
Changed Pin Configuration Section to Pin Connections Section ..	1
Added Figure 2; Renumbered Sequentially .....	1
Added Electrical Characteristics—LFCSP Package Section and Table 2; Renumbered Sequentially .....	4
Changes to Table 4.....	5
Added Pin Configurations and Function Descriptions Section, Figure 17, Table 5, Figure 18, and Table 6 .....	9
Added Figure 21.....	11
Updated Outline Dimensions .....	11
Changes to Ordering Guide.....	11

### 7/10—Rev. A to Rev. B

Changes to Figure 1.....	1
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### 6/10—Rev. 0 to Rev. A

Changes to Fast Logarithmic Amplifier Section .....	8
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### 6/10—Revision 0: Initial Version

## SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS—SOIC PACKAGE

$V_{CB} = 15\text{ V}$ ,  $I_O = 10\text{ }\mu\text{A}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise specified.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DC AND AC CHARACTERISTICS						
Current Gain <sup>1</sup>	$h_{FE}$	$I_C = 1\text{ mA}$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	300	605		
		$I_C = 10\text{ }\mu\text{A}$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	300			
			200	550		
			200			
Current Gain Match <sup>2</sup>	$\Delta h_{FE}$	$10\text{ }\mu\text{A} \leq I_C \leq 1\text{ mA}$		0.5	5	%
Noise Voltage Density <sup>3</sup>	$e_N$	$I_C = 1\text{ mA}$ , $V_{CB} = 0\text{ V}$ $f_O = 10\text{ Hz}$		1.6	2	nV/ $\sqrt{\text{Hz}}$
		$f_O = 100\text{ Hz}$		0.9	1	nV/ $\sqrt{\text{Hz}}$
		$f_O = 1\text{ kHz}$		0.85	1	nV/ $\sqrt{\text{Hz}}$
		$f_O = 10\text{ kHz}$		0.85	1	nV/ $\sqrt{\text{Hz}}$
Low Frequency Noise (0.1 Hz to 10 Hz)	$e_N\text{ p-p}$	$I_C = 1\text{ mA}$		0.4		$\mu\text{V p-p}$
Offset Voltage	$V_{OS}$	$V_{CB} = 0\text{ V}$ , $I_C = 1\text{ mA}$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		10	200	$\mu\text{V}$
					220	$\mu\text{V}$
Offset Voltage Change vs. $V_{CB}$	$\Delta V_{OS}/\Delta V_{CB}$	$0\text{ V} \leq V_{CB} \leq V_{MAX}^4$ , $1\text{ }\mu\text{A} \leq I_C \leq 1\text{ mA}^5$		10	50	$\mu\text{V}$
Offset Voltage Change vs. $I_C$	$\Delta V_{OS}/\Delta I_C$	$1\text{ }\mu\text{A} \leq I_C \leq 1\text{ mA}^5$ , $V_{CB} = 0\text{ V}$		5	70	$\mu\text{V}$
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ , $V_{OS}$ trimmed to 0V		0.08	1	$\mu\text{V}/^\circ\text{C}$
				0.03	0.3	$\mu\text{V}/^\circ\text{C}$
Breakdown Voltage	$BV_{CEO}$		40			V
Gain Bandwidth Product	$f_T$	$I_C = 10\text{ mA}$ , $V_{CE} = 10\text{ V}$		200		MHz
Collector-to-Base Leakage Current	$I_{CBO}$	$V_{CB} = V_{MAX}$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		25	500	pA
				3		nA
Collector-to-Collector Leakage Current	$I_{CC}$	$V_{CC} = V_{MAX}^{6,7}$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		35	500	pA
				4		nA
Collector-to-Emitter Leakage Current	$I_{CES}$	$V_{CE} = V_{MAX}$ , $V_{BE} = 0\text{ V}^{6,7}$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		35	500	pA
				4		nA
Input Bias Current	$I_B$	$I_C = 10\text{ }\mu\text{A}$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$			50	nA
					50	nA
Input Offset Current	$I_{OS}$	$I_C = 10\text{ }\mu\text{A}$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$			6.2	nA
					13	nA
Input Offset Current Drift	$\Delta I_{OS}/\Delta T$	$I_C = 10\text{ }\mu\text{A}^6$ , $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		40	150	pA/ $^\circ\text{C}$
Collector Saturation Voltage	$V_{CE(SAT)}$	$I_C = 1\text{ mA}$ , $I_B = 100\text{ }\mu\text{A}$		0.05	0.2	V
Output Capacitance	$C_{OB}$	$V_{CB} = 15\text{ V}$ , $I_E = 0\text{ }\mu\text{A}$		23		pF
Bulk Resistance	$R_{BE}$	$10\text{ }\mu\text{A} \leq I_C \leq 10\text{ mA}^6$		0.3	1.6	$\Omega$
Collector-to-Collector Capacitance	$C_{CC}$	$V_{CC} = 0\text{ V}$		35		pF

<sup>1</sup> Current gain is guaranteed with collector-to-base voltage ( $V_{CB}$ ) swept from 0V to  $V_{MAX}$  at the indicated collector currents.

<sup>2</sup> Current gain match ( $\Delta h_{FE}$ ) is defined as follows:  $\Delta h_{FE} = (100(\Delta I_B)/(h_{FE\text{ min}})/I_C)$ .

<sup>3</sup> Noise voltage density is guaranteed, but not 100% tested.

<sup>4</sup> This is the maximum change in  $V_{OS}$  as  $V_{CB}$  is swept from 0V to 40V.

<sup>5</sup> Measured at  $I_C = 10\text{ }\mu\text{A}$  and guaranteed by design over the specified range of  $I_C$ .

<sup>6</sup> Guaranteed by design.

<sup>7</sup>  $I_{CC}$  and  $I_{CES}$  are verified by measurement of  $I_{CBO}$ .

**ELECTRICAL CHARACTERISTICS—LFCSP PACKAGE**

$V_{CB} = 15\text{ V}$ ,  $I_O = 100\ \mu\text{A}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise specified.

**Table 2.**

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DC AND AC CHARACTERISTICS						
Current Gain <sup>1</sup>	$h_{FE}$	$I_C = 1\text{ mA}$ , $V_{CB} = 15\text{ V}$	300	1800	2400	
		$I_C = 1\text{ mA}$ , $V_{CB} = 0\text{ V}$	200	1300	2200	
		$I_C = 100\ \mu\text{A}$ , $V_{CB} = 15\text{ V}$	350	2100	2500	
		$I_C = 100\ \mu\text{A}$ , $V_{CB} = 0\text{ V}$	250	1500	2300	
Current Gain Match <sup>2</sup>	$\Delta h_{FE}$	$100\ \mu\text{A} \leq I_C \leq 1\text{ mA}$		0.5	5	%
Noise Voltage Density <sup>3</sup>	$e_N$	$I_C = 1\text{ mA}$ , $V_{CB} = 0\text{ V}$				
		$f_O = 10\text{ Hz}$		1.6	2	nV/ $\sqrt{\text{Hz}}$
		$f_O = 100\text{ Hz}$		0.9	1	nV/ $\sqrt{\text{Hz}}$
		$f_O = 1\text{ kHz}$		0.85	1	nV/ $\sqrt{\text{Hz}}$
		$f_O = 10\text{ kHz}$		0.85	1	nV/ $\sqrt{\text{Hz}}$
Low Frequency Noise (0.1 Hz to 10 Hz)	$e_N\text{ p-p}$	$I_C = 1\text{ mA}$		0.4		$\mu\text{V p-p}$
Offset Voltage	$V_{OS}$	$V_{CB} = 0\text{ V}$ , $I_C = 1\text{ mA}$		25	250	$\mu\text{V}$
		$V_{CB} = 0\text{ V}$ , $I_C = 100\ \mu\text{A}$		10	250	$\mu\text{V}$
Gain Bandwidth Product	$f_T$	$I_C = 10\text{ mA}$ , $V_{CE} = 10\text{ V}$		200		MHz
Input Bias Current	$I_B$	$I_C = 100\ \mu\text{A}$			200	nA
Input Offset Current	$I_{OS}$	$I_C = 100\ \mu\text{A}$			10	nA
Output Capacitance	$C_{OB}$	$V_{CB} = 15\text{ V}$ , $I_E = 0\ \mu\text{A}$		23		pF
Collector-to-Collector Capacitance	$C_{CC}$	$V_{CC} = 0\text{ V}$		35		pF

<sup>1</sup> Current gain is guaranteed with collector-to-base voltage ( $V_{CB}$ ) swept from 0 V to  $V_{MAX}$  at the indicated collector currents.

<sup>2</sup> Current gain match ( $\Delta h_{FE}$ ) is defined as follows:  $\Delta h_{FE} = (100(\Delta I_B)(h_{FE\text{min}})/I_C)$ .

<sup>3</sup> Noise voltage density is guaranteed, but not 100% tested.

## ABSOLUTE MAXIMUM RATING

Table 3.

Parameter	Rating
Breakdown Voltage of Collector-to-Base Voltage ( $BV_{CBO}$ )	40 V
Breakdown Voltage of Collector-to-Emitter Voltage ( $BV_{CEO}$ )	40 V
Breakdown Voltage of Collector-to-Collector Voltage ( $BV_{CC}$ )	40 V
Breakdown Voltage of Emitter-to-Emitter Voltage ( $BV_{EE}$ )	40 V
Collector Current ( $I_C$ )	20 mA
Emitter Current ( $I_E$ )	20 mA
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-40°C to +85°C
Junction Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

$\theta_{JA}$  is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
8-Lead SOIC (R-8)	120	45	°C/W
16-Lead LFCSP (CP-16-22)	75	4.4	°C/W

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

T<sub>A</sub> = 25°C, V<sub>CE</sub> = 5 V, unless otherwise specified.

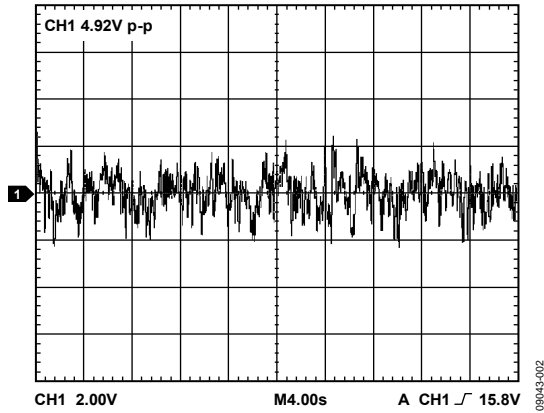


Figure 3. Low Frequency Noise (0.1 Hz to 10 Hz), I<sub>C</sub> = 1 mA, Gain = 10,000,000

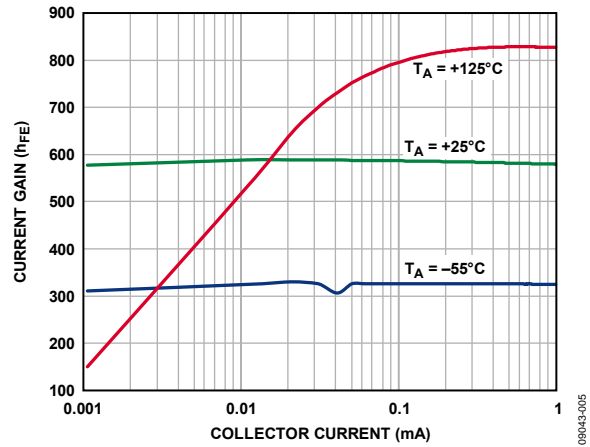


Figure 6. Current Gain vs. Collector Current (V<sub>CB</sub> = 0 V)

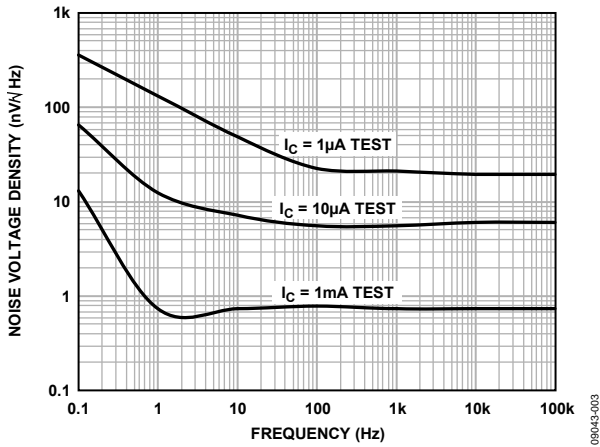


Figure 4. Noise Voltage Density vs. Frequency

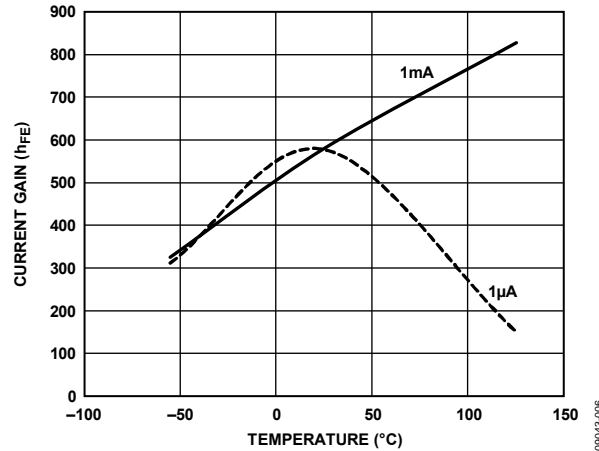


Figure 7. Current Gain vs. Temperature (Excludes I<sub>CB0</sub>)

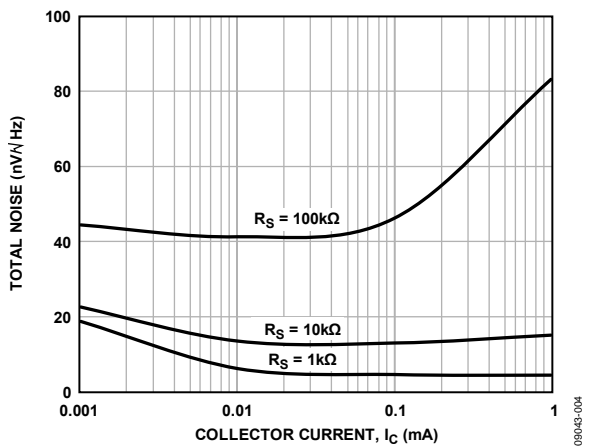


Figure 5. Total Noise vs. Collector Current, f = 1 kHz

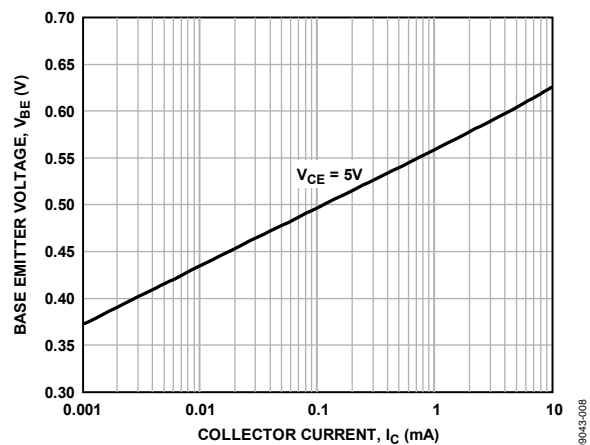


Figure 8. Base Emitter Voltage vs. Collector Current

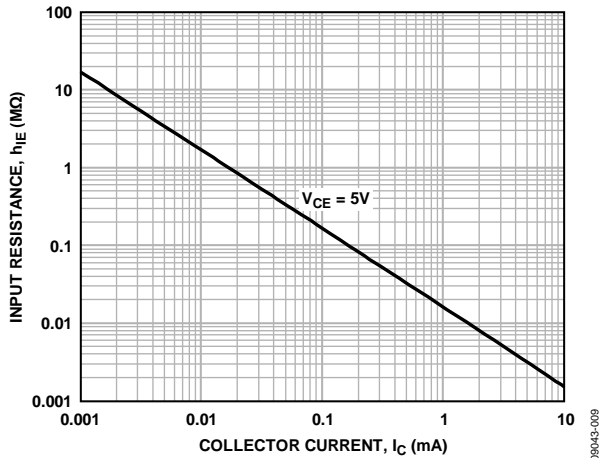


Figure 9. Small Signal Input Resistance vs. Collector Current

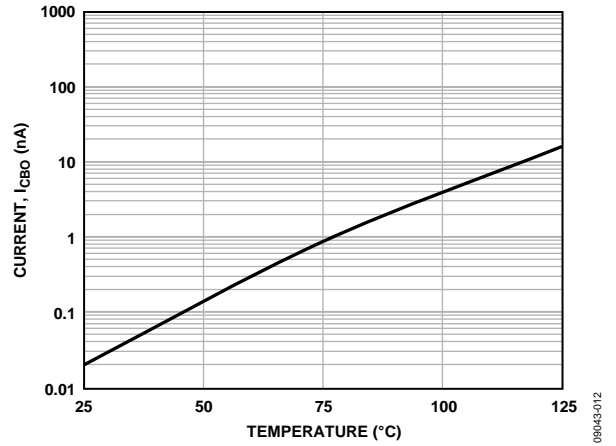


Figure 12. Collector-to-Base Leakage Current vs. Temperature

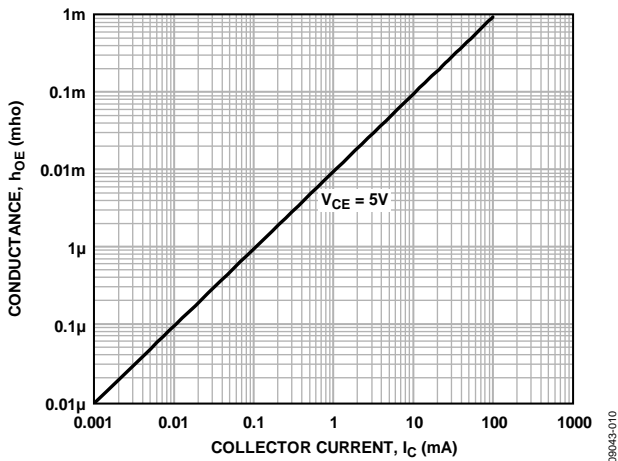


Figure 10. Small Signal Output Conductance vs. Collector Current

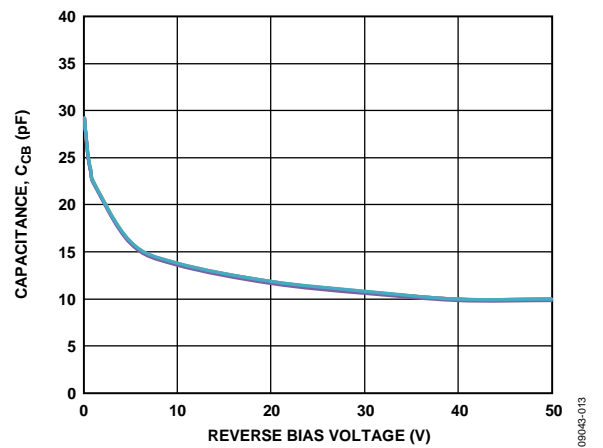


Figure 13. Collector-to-Base Capacitance vs. Reverse Bias Voltage

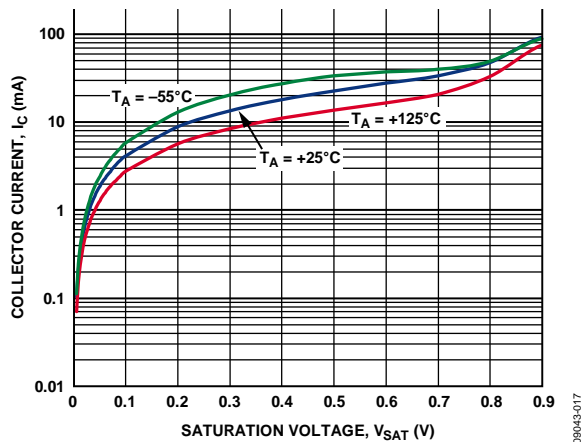


Figure 11. Collector Current vs. Saturation Voltage

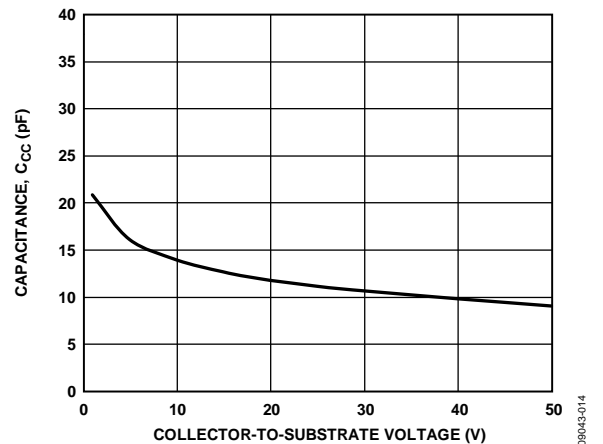


Figure 14. Collector-to-Collector Capacitance vs. Collector-to-Substrate Voltage

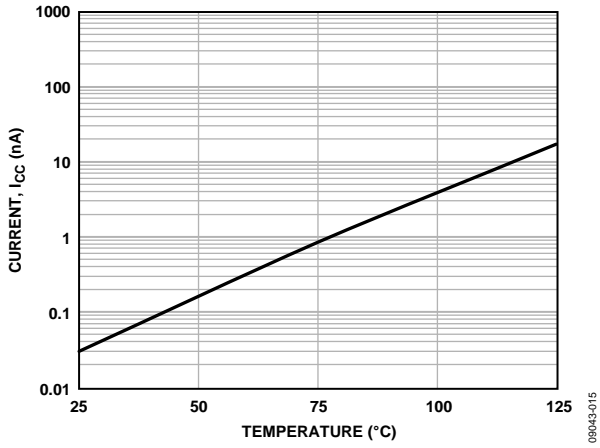


Figure 15. Collector-to-Collector Leakage Current vs. Temperature

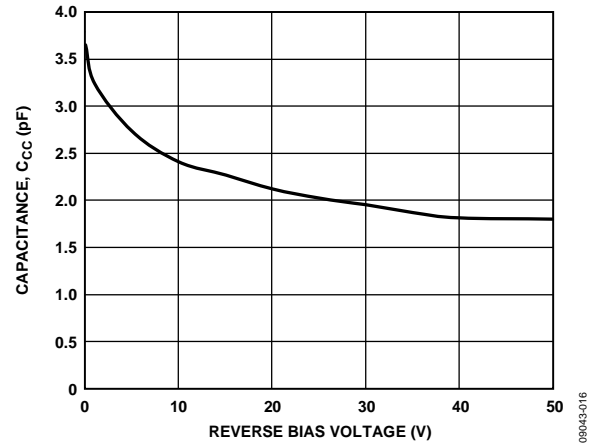


Figure 16. Collector-to-Collector Capacitance vs. Reverse Bias Voltage



## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

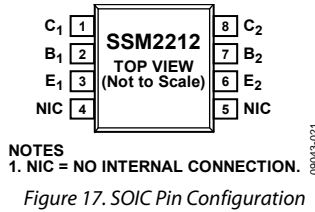


Table 5. SOIC Pin Function Descriptions

Pin No.	Mnemonic	Description
1	C <sub>1</sub>	Collector of Channel 1.
2	B <sub>1</sub>	Base of Channel 1.
3	E <sub>1</sub>	Emitter of Channel 1.
4, 5	NIC	No Internal Connection.
6	E <sub>2</sub>	Emitter of Channel 2.
7	B <sub>2</sub>	Base of Channel 2.
8	C <sub>2</sub>	Collector of Channel 2.

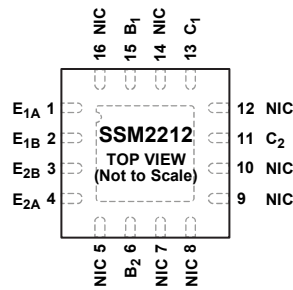


Table 6. LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	E <sub>1A</sub>	Emitter of Channel 1. Must be connect to E <sub>1B</sub> .
2	E <sub>1B</sub>	Emitter of Channel 1. Must be connect to E <sub>1A</sub> .
3	E <sub>2B</sub>	Emitter of Channel 2. Must be connect to E <sub>2A</sub> .
4	E <sub>2A</sub>	Emitter of Channel 2. Must be connect to E <sub>2B</sub> .
5, 7, 8, 9, 10, 12, 14, 16	NIC	No Internal Connection.
6	B <sub>2</sub>	Base of Channel 2.
11	C <sub>2</sub>	Collector of Channel 2.
13	C <sub>1</sub>	Collector of Channel 1.
15	B <sub>1</sub>	Base of Channel 1.
	EPAD	Exposed Pad. The exposed pad must be connected to the lowest potential.

## APPLICATIONS INFORMATION

### FAST LOGARITHMIC AMPLIFIER

The circuit in Figure 19 is a modification of a standard logarithmic amplifier configuration. Running the SSM2212 at 2.5 mA per side (full scale) allows a fast response with a wide dynamic range. The circuit has a 7 decade current range and a 5 decade voltage range, and it is capable of 2.5  $\mu$ s settling time to 1% with a 1 V to 10 V step. The output follows the equation:

$$V_O = \frac{R_3 + R_2}{R_2} \frac{kT}{q} \ln \frac{V_{REF}}{V_{IN}}$$

To compensate for the temperature dependence of the  $kT/q$  term, a resistor with a positive 0.35%/°C temperature coefficient is chosen for  $R_2$ . The output is inverted with respect to the input and is nominally  $-1$  V/decade using the component values indicated.

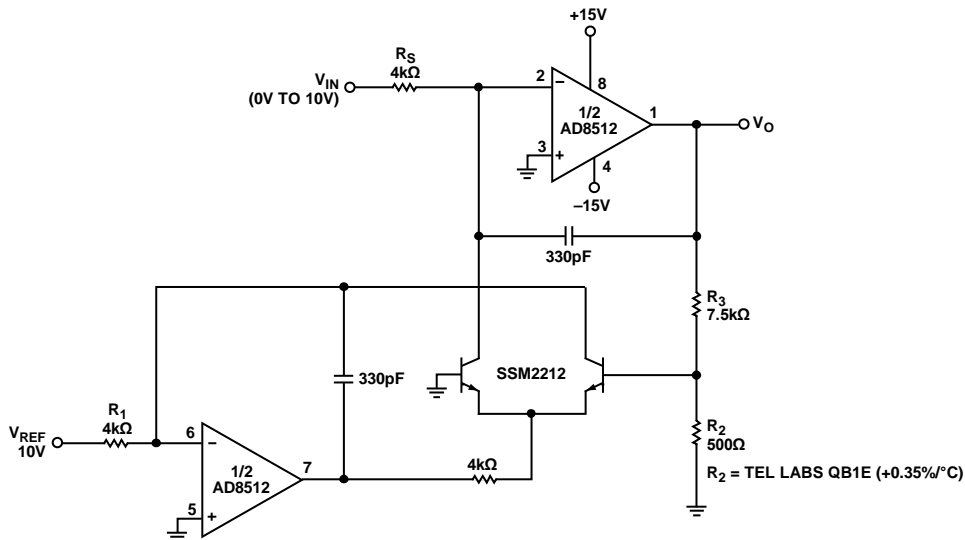
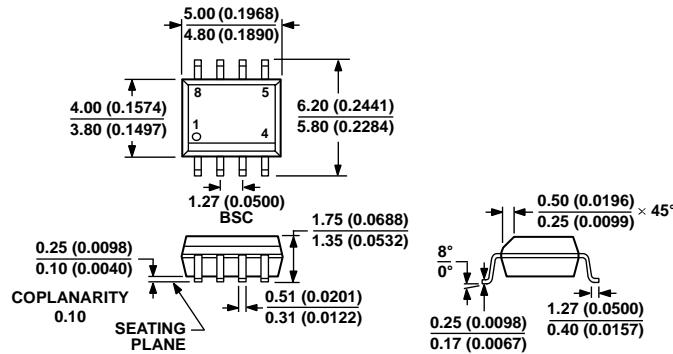


Figure 19. Fast Logarithmic Amplifier

09043-018

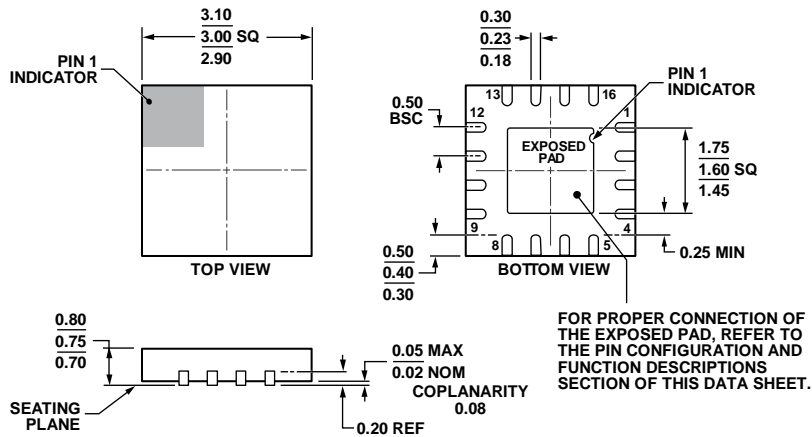
# OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA  
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 20. 8-Lead Standard Small Outline Package [SOIC\_N]  
 Narrow Body  
 (R-8)

Dimensions shown in millimeters (and inches)



COMPLIANT TO JEDEC STANDARDS MO-220-WEED-6.

Figure 21. 16-Lead Lead Frame Chip Scale Package [LFCSP\_WQ]  
 3 mm x 3 mm Body, Very Very Thin Quad  
 (CP-16-22)

Dimensions shown in millimeters

## ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option	Branding
SSM2212RZ	-40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
SSM2212RZ-R7	-40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
SSM2212RZ-RL	-40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
SSM2212CPZ-R7	-40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-22	A3F
SSM2212CPZ-RL	-40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-22	A3F

<sup>1</sup>Z = RoHS Compliant Part.

**NOTES**