1 Mbit Serial Flash
SST45LF010

Data Sheet

FEATURES:

- **Single 3.0-3.6V Read and Write Operations**
- **Serial Interface Architecture**
- **Byte Serial Read with Single Command**
- **Superior Reliability**
  - Endurance: 100,000 Cycles (typical)
  - Greater than 100 years Data Retention
- **Low Power Consumption**
  - Active Current: 10 mA (typical)
  - Standby Current: 10 µA (typical)
- **Sector or Chip-Erase Capability**
  - Uniform 4 KByte sectors
- **Fast Erase and Byte-Program**
  - Chip-Erase Time: 70 ms (typical)
  - Sector-Erase Time: 18 ms (typical)
  - Byte-Program Time: 14 µs (typical)
- **Automatic Write Timing**
  - Internal V_{PP} Generation
- **End-of-Write Detection**
  - Software Status
- **10 MHz Max Clock Frequency**
- **Hardware Reset Pin (RST#)**
  - Resets the device to Standby Mode
- **CMOS I/O Compatibility**
- **Hardware Data Protection (WP#)**
  - Protects and unprotects the device from Write operation
- **Packages Available**
  - 8-lead SOIC (4.9mm x 6mm)
  - 8-contact WSON

PRODUCT DESCRIPTION

The SST45LF010 is a 1 Mbit serial flash memory manufactured with SST's proprietary, high performance CMOS SuperFlash technology. The 1 Mbit of memory is organized as 32 sectors of 4096 Bytes. The flash memory uses a 4-wire serial interface and a chip enable to select and sequentially access its data. The serial interface consists of; serial data input (SI), serial data output (SO), serial clock (SCK), and chip enable (CE#). A write protect (WP#) inhibits the entire memory from Write operation and a hardware reset pin (RST#) resets the device to standby mode.

The SST45LF010 device is offered in both 8-lead SOIC and 8-contact WSON packages. See Figure 2 for the pin assignments.

Device Operation

The SST45LF010 uses bus cycles of 8 bits each for commands, data, and addresses to execute operations. The operation instructions are listed in Table 3.

All instructions are synchronized off a high to low transition of CE#. The first low to high transition on SCK will initiate the instruction sequence. Inputs will be accepted on the rising edge of SCK starting with the most significant bit. Any low to high transition on CE# before the input instruction completes will terminate any instruction in progress and return the device to the standby mode.

Read

The Read operation outputs the data in order from the initial accessed address. While SCK is input, the address will be incremented automatically until end (top) of the address space (1FFFFH), then the internal address pointer automatically increments to beginning (bottom) of the address space (00000H), and data out stream will continue. The read data stream is continuous through all addresses until terminated by a low to high transition on CE#.

Sector/Chip-Erase Operation

The Sector-Erase operation clears all bits in the selected sector to FFH. The Chip-Erase instruction clears all bits in the device to FFH.

Byte-Program Operation

The Byte-Program operation programs the bits in the selected byte to the desired data. The selected byte must be in the erased state (FFH) when initiating a Program operation. The data is input from bit 7 to bit 0 in order.

Software Status Operation

The Status operation determines if an Erase or Program operation is in progress. If bit 0 is at a "0" an Erase or Program operation is in progress, the device is busy. If bit 0 is at a "1" the device is ready for any valid operation. The status read is continuous with ongoing clock cycles until terminated by a low to high transition on CE#.

Reset

Reset will terminate any operation, e.g., Read, Erase and Program, in progress. It is activated by a high to low transition on the RST# pin. The device will remain in reset condition as long as RST# is low. Minimum reset time is 10 µs. See Figure 15 for reset timing diagram. RST# is internally pulled-up and could remain unconnected during normal operation. After reset, the device is in standby mode, a high to low transition on CE# is required to start the next operation.

An internal power-on reset circuit protects against accidental data writes. Applying a logic level low to RST# during the power-on process then changing to a logic level high when V_{DD} has reached the correct voltage level will provide additional protection against accidental writes during power on.

Read SST ID/Read Device ID

The Read SST ID and Read Device ID operations read the JEDEC assigned manufacturer's identification and the manufacturer assigned device IDs. These IDs may be used to determine the actual device resident in the system.

TABLE 1: PRODUCT IDENTIFICATION

	Byte	Data
Manufacturer's ID	0000H	BFH
Device ID	0001H	42H

T1.2 372

Write Protect

The WP# pin provides inadvertent write protection. The WP# pin must be held high for any Erase or Program operation. The WP# pin can be V_{IL} or V_{IH}, but no other value, for all other operations. In typical use, the WP# pin is connected to V_{SS} with a standard pull-down resistor. WP# is then driven high whenever an Erase or Program operation is required. If the WP# pin is tied to V_{DD} with a pull-up resistor, then all operations may occur and the write protection feature is disabled. The WP# pin has an internal pull-up and could remain unconnected when not used.

Reduced-Function Option (SST45LF010-10-4C-SA-DD014)

The SST45LF010-10-4C-SA-DD014 is a reduced-function option of the SST45LF010-10-4C-xA.

For these devices, SST only tests and guarantees functionality when separate serial input and serial output data lines are used. Valid connections must be as illustrated in Figure 1.

The RESET# pin is not tested during production; it must be left unconnected or tied to V_{DD}.

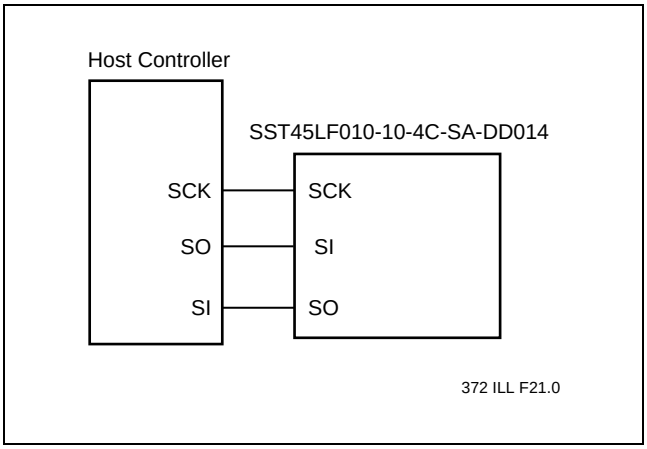
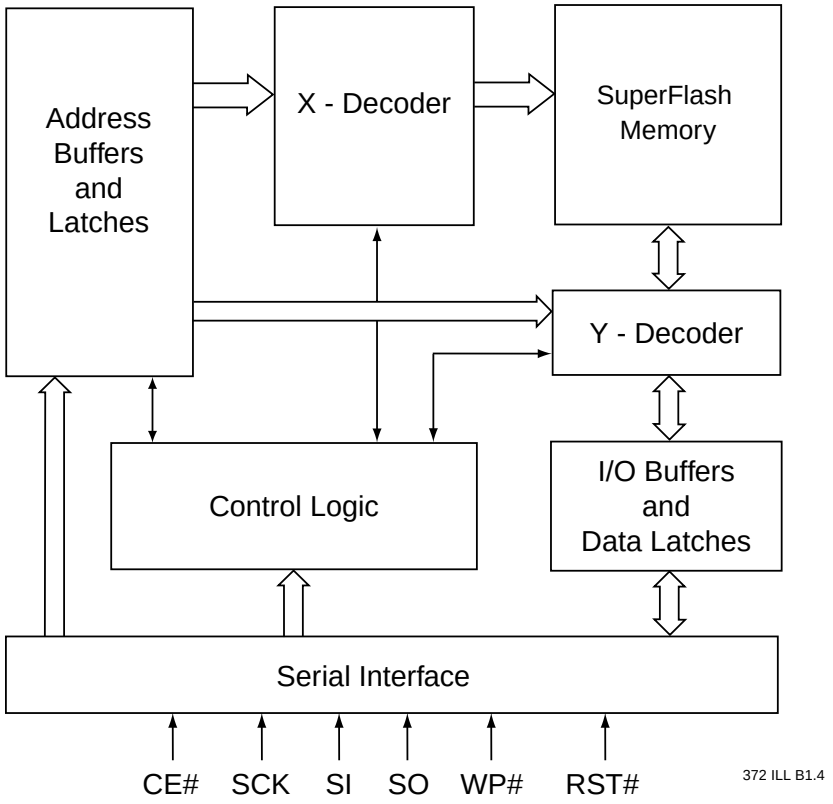
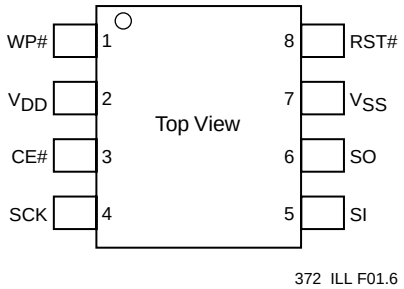
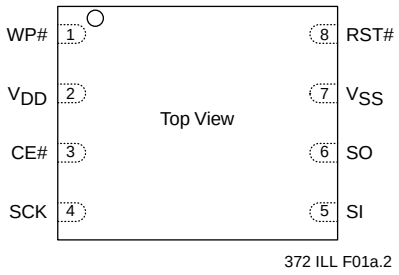


FIGURE 1: VALID CONNECTIONS FOR SST45LF010-10-4C-SA-DD014

FUNCTIONAL BLOCK DIAGRAM







8-LEAD SOIC **8-CONTACT WSON**

FIGURE 2: PIN ASSIGNMENTS

TABLE 2: PIN DESCRIPTION

Symbol	Pin Name	Functions
SCK	Serial Clock	To provide the timing of the serial interface. Commands, addresses, or input data are latched on the rising edge of the clock input, while output data is shifted out on the falling edge of the clock input.
SI	Serial Data Input	To transfer commands, addresses, or data serially into the device. Inputs are latched on the rising edge of the serial clock.
SO	Serial Data Output	To transfer data serially out of the device. Data is shifted out on the falling edge of the serial clock.
CE#	Chip Enable	The device is enabled by a high to low transition on CE#.
WP#	Write Protect	To protect the device from unintentional Write (Erase or Program) operations. When WP# is low, all Erase and Program commands are ignored. When WP# is high, the device may be erased or programmed. This pin has an internal pull-up and could remain unconnected when not used.
RST#	Reset	A high to low transition on RST# will terminate any operation in progress and reset the internal logic to the standby mode. The device will remain in the reset condition as long as the RST# is low. Operations may only occur when RST# is high. This pin has an internal pull-up and could remain unconnected when not used.
V_{DD}	Power Supply	To provide power supply (3.0-3.6V).
V_{SS}	Ground	

T2.5 372

TABLE 3: DEVICE OPERATION INSTRUCTIONS[1]

Bus Cycle[2]	1		2		3		4		5		6		7	
Cycle Type/ Operation[3,4]	S_{IN}	S_{OUT}	S_{IN}	S_{OUT}	S_{IN}	S_{OUT}	S_{IN}	S_{OUT}	S_{IN}	S_{OUT}	S_{IN}	S_{OUT}	S_{IN}	S_{OUT}
Read	FFH	Hi-Z	A_{23}-A_{16}	Hi-Z	A_{15}-A_8	Hi-Z	A_7-A_0	Hi-Z	X	Hi-Z	X	Hi-Z	X	D_{OUT}
Sector-Erase[5]	20H	Hi-Z	A_{23}-A_{16}	Hi-Z	A_{15}-A_8	Hi-Z	X	Hi-Z	D0H	Hi-Z	X	Hi-Z	X	Hi-Z
Chip-Erase	60H	Hi-Z	X	Hi-Z	X	Hi-Z	X	Hi-Z	D0H	Hi-Z	X	Hi-Z	X	Hi-Z
Byte-Program	10H	Hi-Z	A_{23}-A_{16}	Hi-Z	A_{15}-A_8	Hi-Z	A_7-A_0	Hi-Z	D_{IN}	Hi-Z	X	Hi-Z	X	Hi-Z
Status Reg.	9FH	X	X	D_{OUT}	X	Note[6]	X	Note[6]	X	Note[6]	X	Note[6]	X	Note[6]
Read-ID	90H	Hi-Z	00H	Hi-Z	00H	Hi-Z	ID Addr[7]	Hi-Z	X	D_{OUT}[7]	X	Note[8]	X	Note[8]

T3.10 372

1. For SST45LF010, A_{23}-A_{17} can be V_{IL} or V_{IH}, but no other value.
2. One bus cycle is eight clock periods
3. Operation: S_{IN}=Serial In, S_{OUT}=Serial Out
4. X = Dummy cycles (can be V_{IL} or V_{IH}, but no other value.)
5. A_{16}-A_{12} are used to determine sector address, A_{11}-A_8 can be V_{IL} or V_{IH}, but no other value.
6. The status read is continuous with ongoing clock cycles until terminated by a low to high transition on CE#.
7. Manufacturer's ID = BFH, is read with A_0 = 0 and Device ID = 42H, is read with A_0 = 1; All other address bits are 0
8. The data output is arbitrary.

TABLE 4: DEVICE OPERATION TABLE

Operation	SI	SO	CE#[1]	WP#	RST#
Read	X	D_{OUT}	Low	X	High
Sector-Erase	X	X	Low	High	High
Chip-Erase	X	X	Low	High	High
Byte-Program	D_{IN}	X	Low	High	High
Software-Status	X	D_{OUT}	Low	X	High
Reset[2]	X	X	X	X	Low
Read SST ID	X	D_{OUT}	Low	X	High
Read Device ID	X	D_{OUT}	Low	X	High

T4.6 372

1. A high to low transition on CE# will be required to start any device operation except for Reset.
2. The RST# low will return the device to standby and terminate any Erase or Program operation in progress.

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential . . . . . -0.5V to V_{DD}+0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential . . . . . -2.0V to V_{DD}+2.0V
Package Power Dissipation Capability (Ta = 25°C) 1.0W
Surface Mount Lead Soldering Temperature (3 Seconds) . . . . . 240°C
Output Short Circuit Current[1] . . . . . 50 mA

1. Outputs shorted for no more than one second. No more than one output shorted at a time.

OPERATING RANGE

Range	Ambient Temp	V_{DD}
Commercial	0°C to +70°C	3.0-3.6V

AC CONDITIONS OF TEST

Input Rise/Fall Time	5 ns
Output Load	C_L = 30 pF
See Figures 3 and 4	

TABLE 5: DC OPERATING CHARACTERISTICS V_{DD} = 3.0-3.6V

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I_{DD}	Active V_{DD} Current				SCK input=V_{ILT}/V_{IHT} at f=10 MHz Max
	Read		20	mA	CE#=V_{IL}, V_{DD}=V_{DD} Max
	Program and Erase		30	mA	CE#=V_{IL}, V_{DD}=V_{DD} Max
I_{SB}	Standby V_{DD} Current		15	µA	CE#=V_{IHC}, V_{DD}=V_{DD} Max
I_{LI}	Input Leakage Current		1	µA	V_{IN}=GND to V_{DD}, V_{DD}=V_{DD} Max
I_{LO}	Output Leakage Current		1	µA	V_{OUT}=GND to V_{DD}, V_{DD}=V_{DD} Max
I_{IL}	Input Low Current[1]		360	µA	WP#, RST#=GND
V_{IL}	Input Low Voltage		0.8	V	V_{DD}=V_{DD} Min
V_{IH}	Input High Voltage	0.7 V_{DD}		V	V_{DD}=V_{DD} Max
V_{IHC}	Input High Voltage (CMOS)	V_{DD}-0.3		V	V_{DD}=V_{DD} Max
V_{OL}	Output Low Voltage		0.2	V	I_{OL}=100 µA, V_{DD}=V_{DD} Min
V_{OH}	Output High Voltage	V_{DD}-0.2		V	I_{OH}=-100 µA, V_{DD}=V_{DD} Min

T5.4 372

1. This parameter only applies to WP# and RST# pins.

TABLE 6: CAPACITANCE (Ta = 25°C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
C_{OUT}[1]	Output Pin Capacitance	V_{OUT} = 0V	12 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	6 pF

T6.1 372

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 7: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}[1]	Endurance	10,000	Cycles	JEDEC Standard A117
T_{DR}[1]	Data Retention	100	Years	JEDEC Standard A103
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

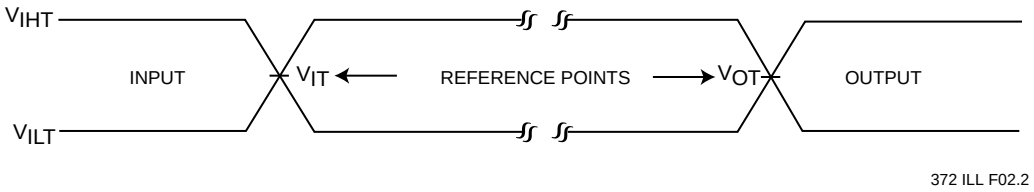
T7.1 372

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 8: AC OPERATING CHARACTERISTICS, V_{DD} = 3.0-3.6V

		Limits		
Symbol	Parameter	Min	Max	Units
F_{CLK}	Serial Clock Frequency		10	MHz
T_{SCKH}	Serial Clock High Time	45		ns
T_{SCKL}	Serial Clock Low Time	45		ns
T_{CES}	CE# Setup Time	250		ns
T_{CEH}	CE# Hold Time	250		ns
T_{CPH}	CE# High Time	250		ns
T_{CHZ}	CE# High to High-Z Output		25	ns
T_{CLZ}	SCK Low to Low-Z Output	0		ns
T_{RLZ}	RST# Low to High-Z Output		25	ns
T_{DS}	Data In Setup Time	20		ns
T_{DH}	Data In Hold Time	20		ns
T_{OH}	Output Hold from SCK Change	0		ns
T_{V}	Output Valid from SCK		35	ns
T_{WPS}	Write Protect Setup Time	10		ns
T_{WPH}	Write Protect Hold Time	10		ns
T_{SE}	Sector-Erase		25	ms
T_{SCE}	Chip-Erase		100	ms
T_{BP}	Byte-Program		20	µs
T_{RST}	Reset Pulse Width	10		µs
T_{REC}	Reset Recovery Time		1	µs
T_{PURST}	Reset Time After Power-Up	10		µs

T8.2 372



AC test inputs are driven at V_{IHT} (0.9 V_{DD}) for a logic "1" and V_{ILT} (0.1 V_{DD}) for a logic "0". Measurement reference points for inputs and outputs are V_{IT} (0.5 V_{DD}) and V_{OT} (0.5 V_{DD}). Input rise and fall times (10% ↔ 90%) are <5 ns.

Note: V_{IT} - V_{INPUT} Test
V_{OT} - V_{OUTPUT} Test
V_{IHT} - V_{INPUT} HIGH Test
V_{ILT} - V_{INPUT} LOW Test

FIGURE 3: AC INPUT/OUTPUT REFERENCE WAVEFORMS

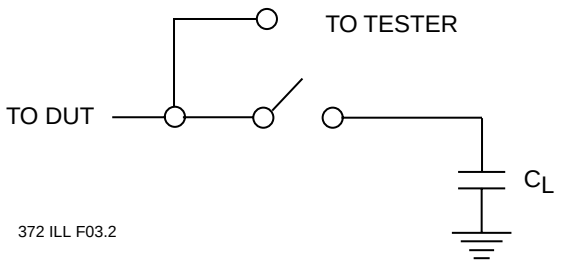


FIGURE 4: A TEST LOAD EXAMPLE

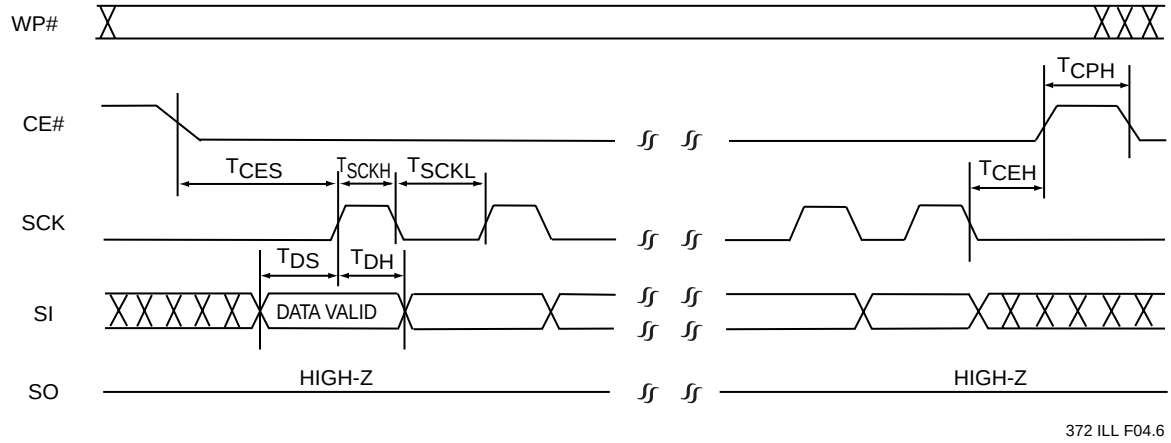


FIGURE 5: SERIAL INPUT TIMING DIAGRAM (INACTIVE SERIAL CLOCK LOW)

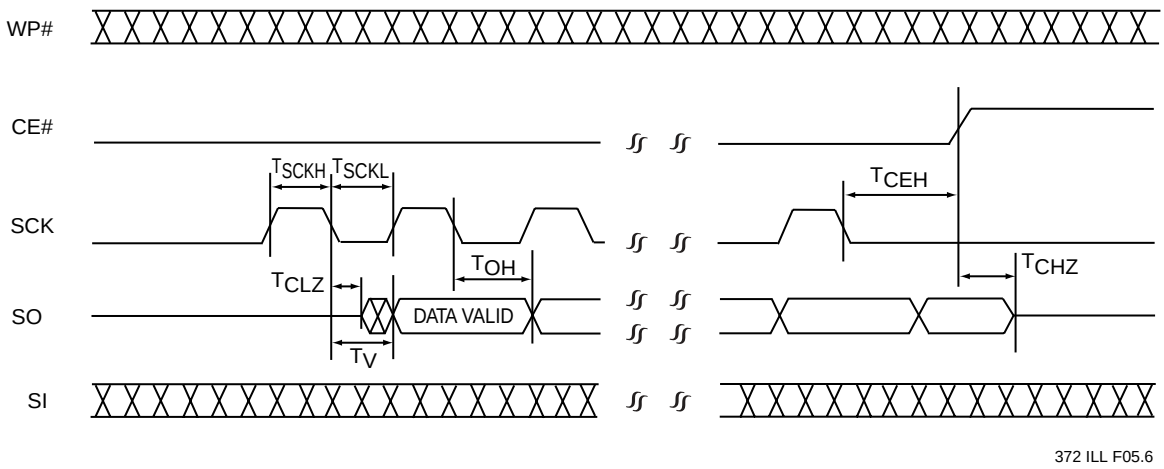


FIGURE 6: SERIAL OUTPUT TIMING DIAGRAM (INACTIVE SERIAL CLOCK LOW)

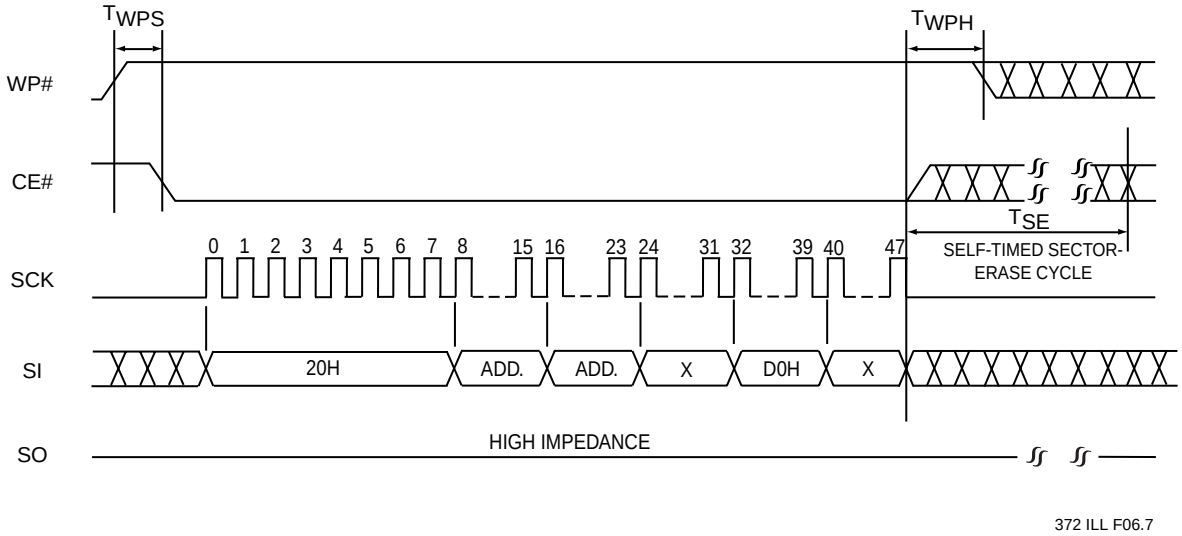


FIGURE 7: SECTOR-ERASE TIMING DIAGRAM

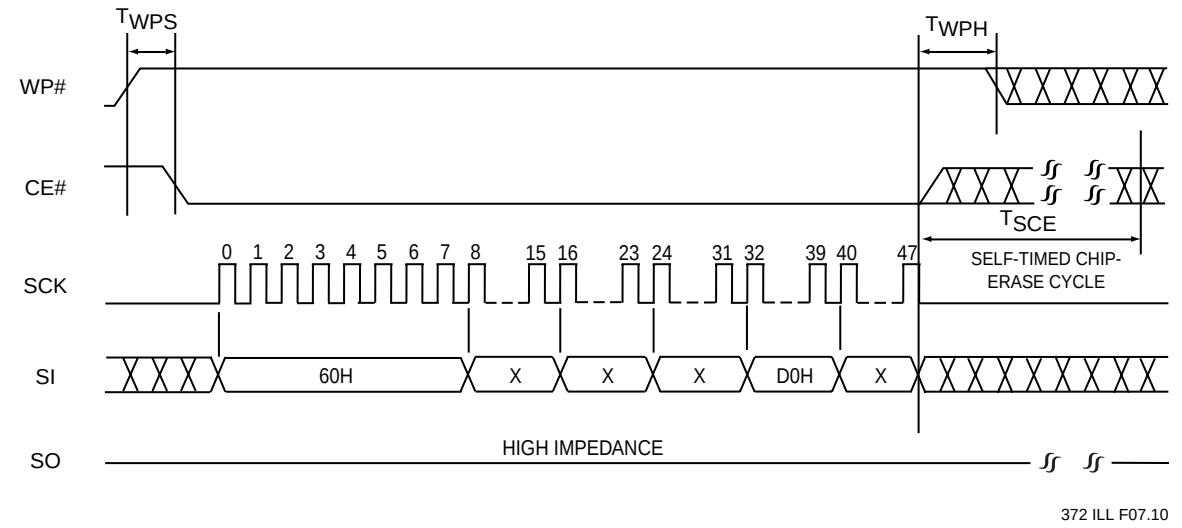


FIGURE 8: CHIP-ERASE TIMING DIAGRAM

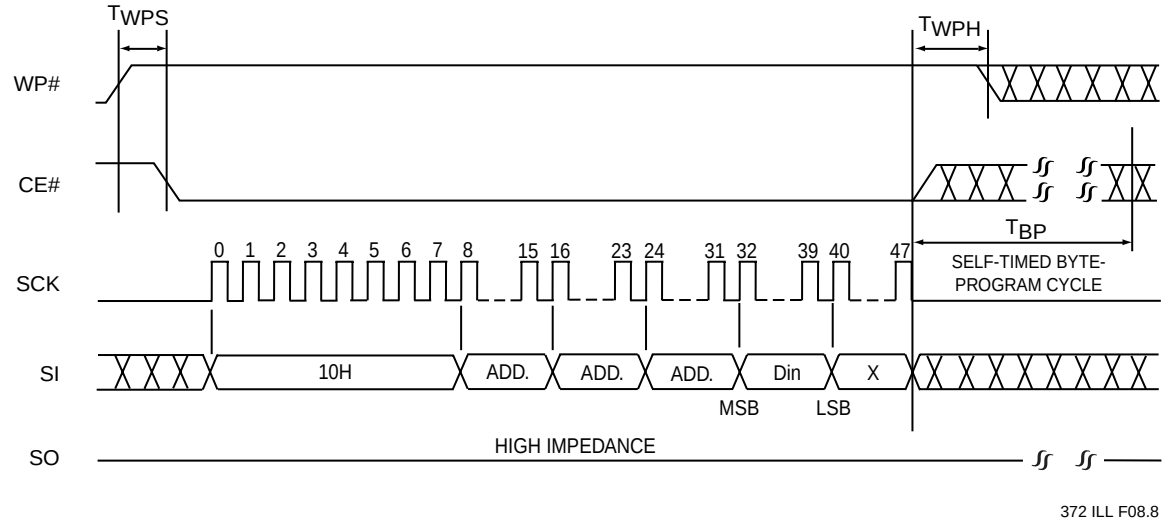


FIGURE 9: BYTE-PROGRAM TIMING DIAGRAM

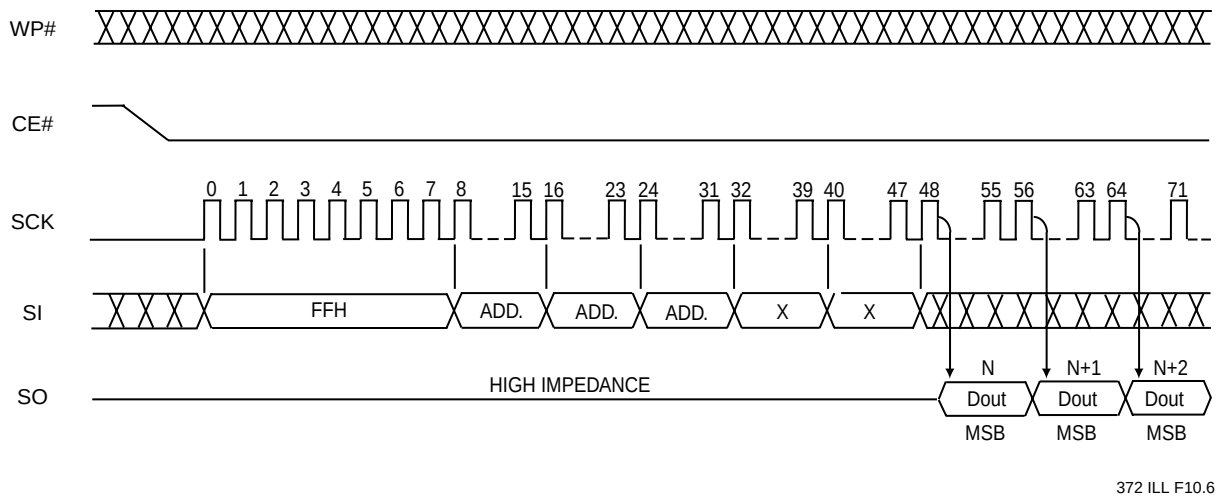
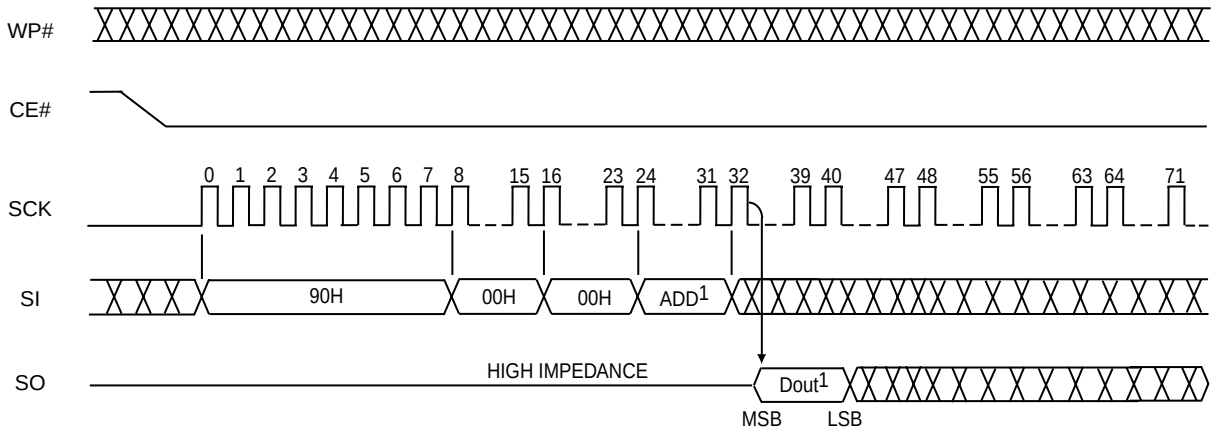


FIGURE 10: READ TIMING DIAGRAM



Note: 1. SST Manufacturer's ID = BFH is read with A_0=0
SST45LF010 Device ID = 42H is read with A_0=1

FIGURE 11: READ-ID TIMING DIAGRAM

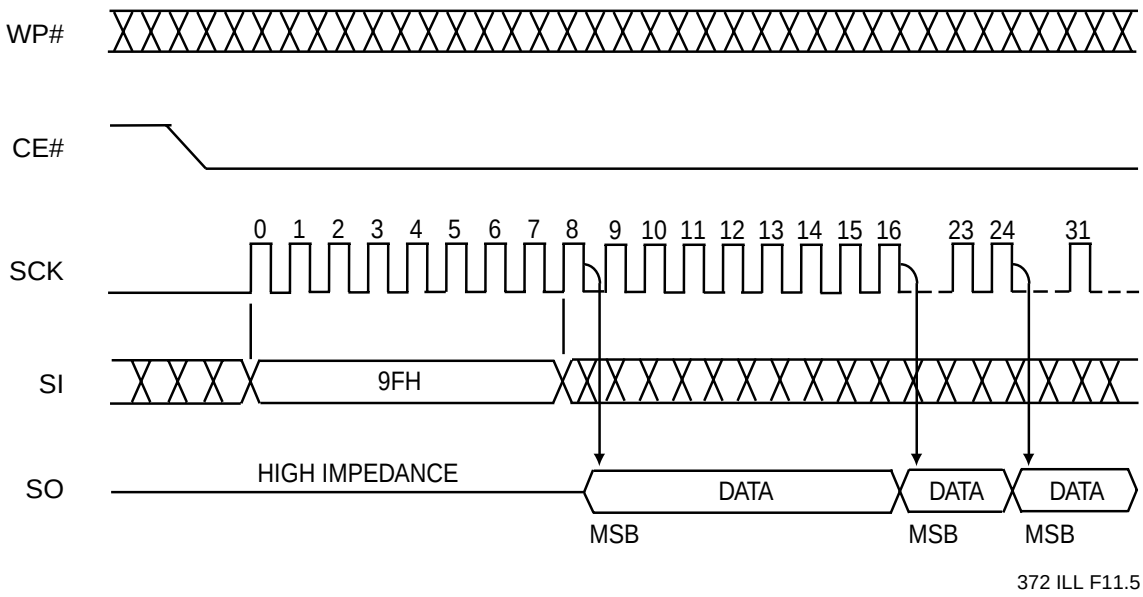


FIGURE 12: SOFTWARE-STATUS TIMING DIAGRAM

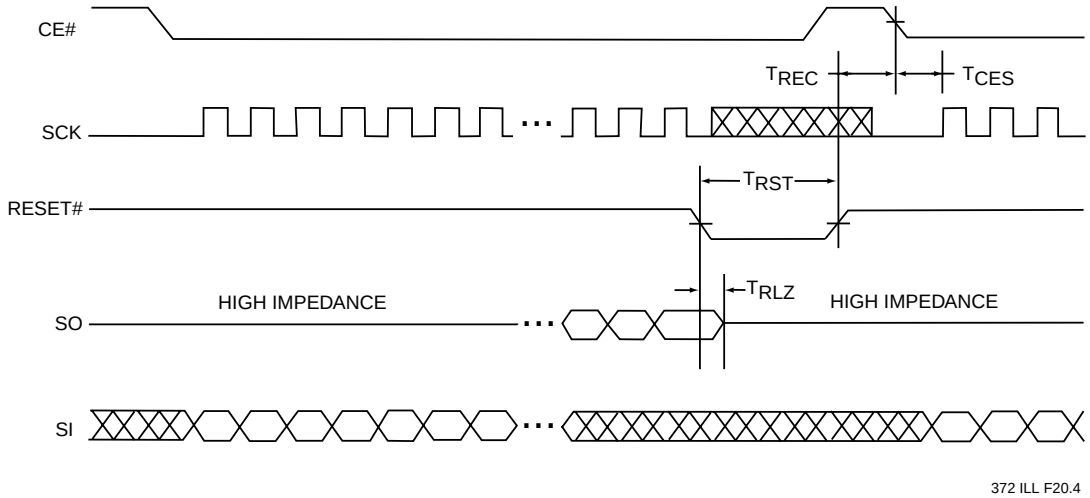


FIGURE 13: RESET TIMING DIAGRAM (INACTIVE CLOCK POLARITY LOW)

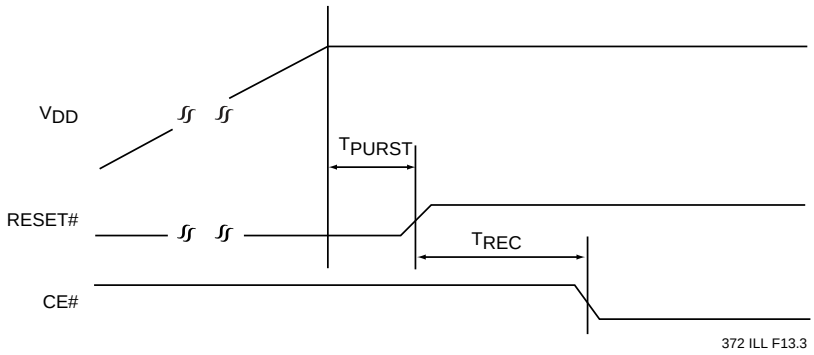


FIGURE 14: POWER-ON RESET TIMING DIAGRAM

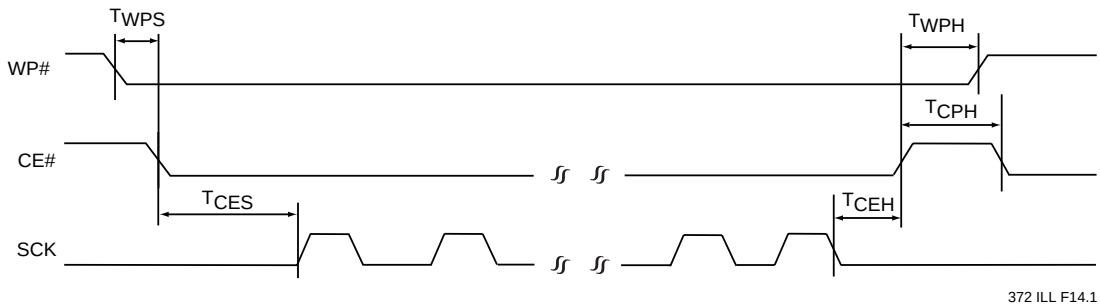
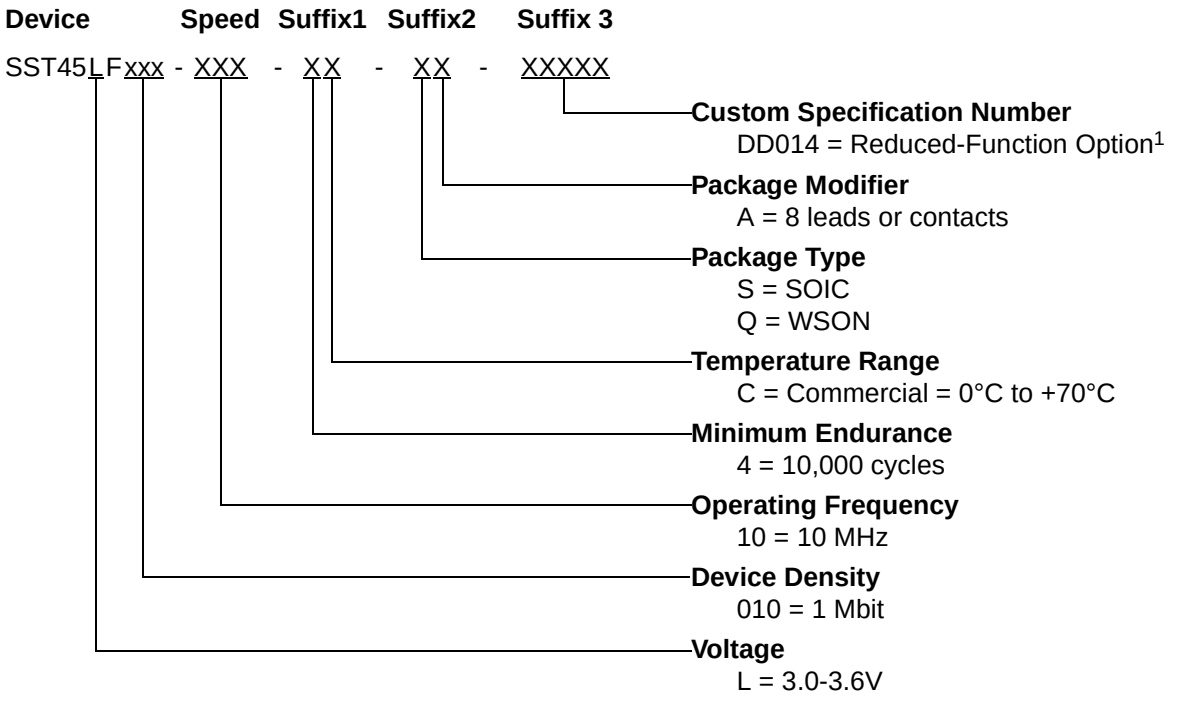


FIGURE 15: WRITE PROTECT TIMING DIAGRAM

PRODUCT ORDERING INFORMATION



1. For details, see "Reduced-Function Option (SST45LF010-10-4C-SA-DD014)" on page 2.

Valid combinations for SST45LF010

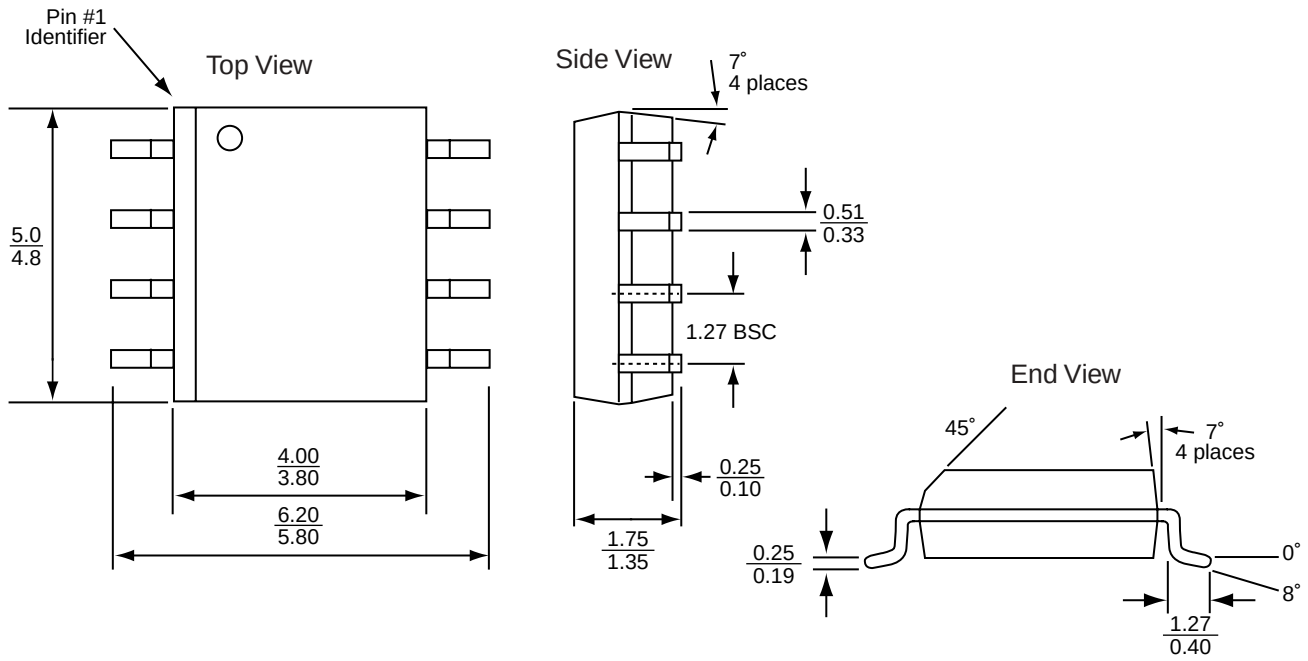
SST45LF010-10-4C-SA SST45LF010-10-4C-QA

SST45LF010-10-4C-SA-DD014

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Non-Pb: Several devices in this data sheet are also offered in non-Pb (no lead added) packages.
The non-Pb part number is simply the standard part number with the letter "E" added to the end of the package code.
The non-Pb package codes corresponding to the packages listed above are SAE and QAE.

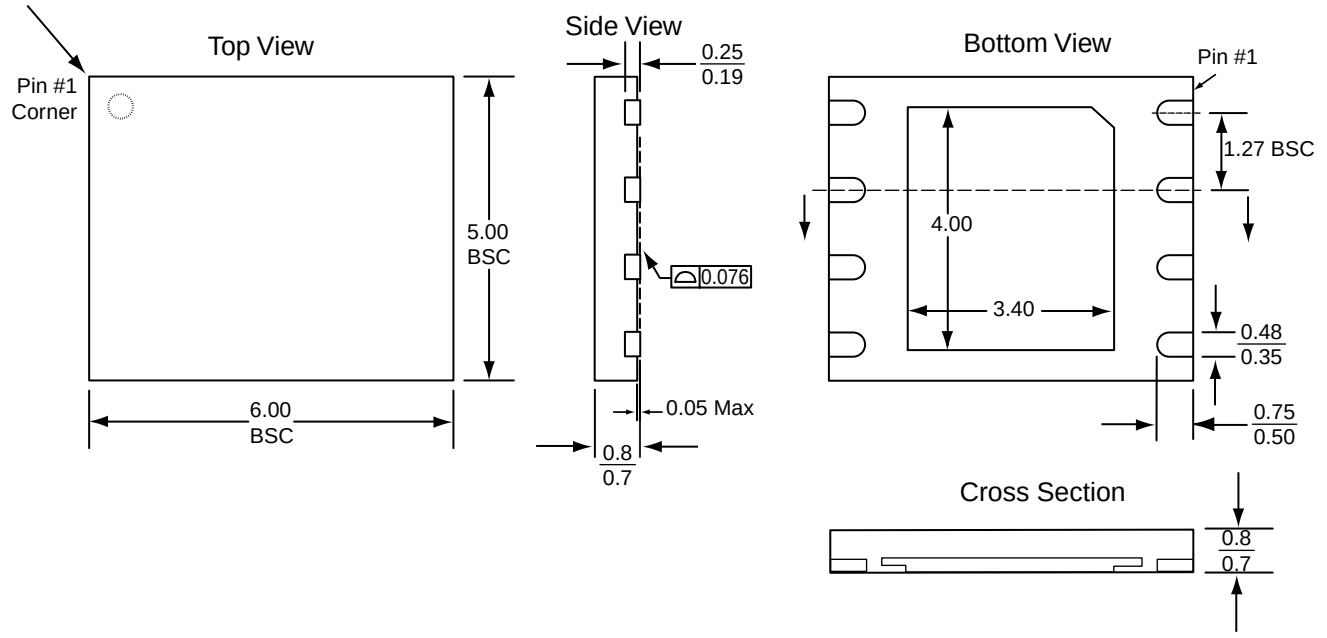
PACKAGING DIAGRAMS



Note: 1. Complies with JEDEC publication 95 MS-012 AA dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in millimeters (max/min).
3. Coplanarity: 0.1 mm
4. Maximum allowable mold flash is 0.15 mm at the package ends and 0.25 mm between leads.

08-soic-5x6-SA-7

8-LEAD SMALL OUTLINE INTEGRATED CIRCUIT (SOIC)
SST PACKAGE CODE: SA



8-CONTACT ULTRA-THIN SMALL OUTLINE NO-LEAD (WSON)
SST PACKAGE CODE: QA

TABLE 9: REVISION HISTORY

Number	Description	Date
03	• 2002 Data Book	May 2002
04	• Added section for Custom Specification number DD014 on page 2 • Part number changes - see page 14 for additional information • Clarified the Test Conditions for Active V_{DD} Current parameter in Table 5 on page 6	Mar 2003