STP3052D

P Channel Enhancement Mode MOSFET

-25.0A

DESCRIPTION

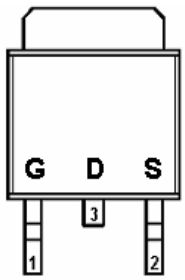
STP3052D is the P-Channel logic enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application. Such as DC/DC converter and Desktop computer power management.

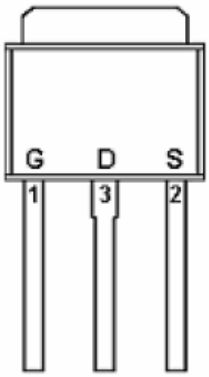
The package is universally preferred for commercial industrial surface mount applications.

PIN CONFIGURATION (D-PAK)

TO-252



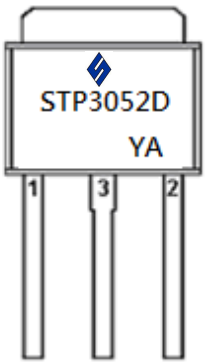
TO-251

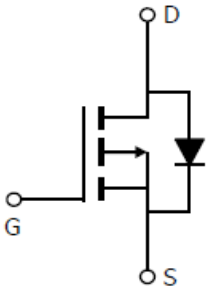


FEATURE

- -30V/-25.0A, $R_{DS(ON)}$ = 45mΩ (Typ.) @V_{GS} = -10V
- -30V/-16.0A, $R_{DS(ON)}$ = 78mΩ @V_{GS} =-5.0V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- TO-252,TO-251 package design

PART MARKING





Y: Year Code A: Process Code

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ABSOULTE MAXIMUM RATINGS (Ta = 25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		VDSS	-30	V
Gate-Source Voltage		VGSS	±20	V
Continuous Drain Current (TJ=150℃)	TA=25℃ TA=70℃	ID	-25.0 -18.0	A
Pulsed Drain Current		IDM	-100	A
Continuous Source Current (Diode Conduction)		IS	-15	A
Power Dissipation	TA=25℃ TA=70℃	PD	40 20	W
Operation Junction Temperature		TJ	150	℃
Storgae Temperature Range		TSTG	-55/150	℃
Thermal Resistance-Junction to Ambient		RθJA	105	℃/W

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ELECTRICAL CHARACTERISTICS (Ta = 25℃ Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,ID=-250uA	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},ID=-250uA	-1.0		-3.0	V
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-40V,V_{GS}=0V			-1	uA
		V_{DS}=-40V,V_{GS}=0V T_J=55℃			-5	
Drain-source On-Resistance	$R_{DS(on)}$	V_{GS}=-10V,I_D=-25A V_{GS}=-5.0V,I_D=-16A		45 78	50 85	mΩ
Forward Transconductance	gfs	V_{DS}=-10V,I_D=-8A		8		S
Diode Forward Voltage	V_{SD}	I_S=-16A,V_{GS}=0V			-1.2	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=-15V,V_{DS}=-100V I_D=-3.5A		16.5		nC
Gate-Source Charge	Q_{gs}			2.8		
Gate-Drain Charge	Q_{gd}			4.5		
Input Capacitance	C_{iss}	V_{DS} =-15V,VGS=0V F=1MHz		700		pF
Output Capacitance	C_{oss}			129		
Reverse TransferCapacitance	C_{rss}			75		
Turn-On Time	$t_{d(on)}$	V_{DD}=-15V,R_L=15Ω R_{GEN}=-10V,R_G=6Ω I_D≡-1.0A			25	nS
	tr				26	
Turn-Off Time	$t_{d(off)}$				70	
	tf				50	

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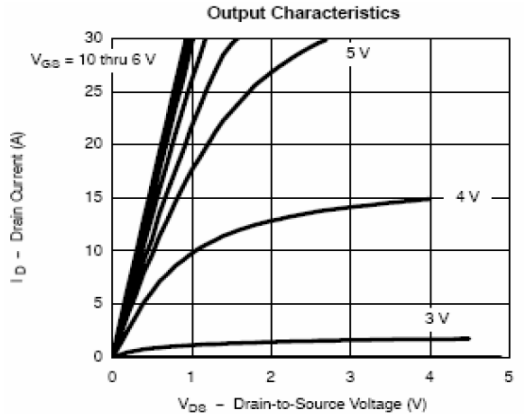
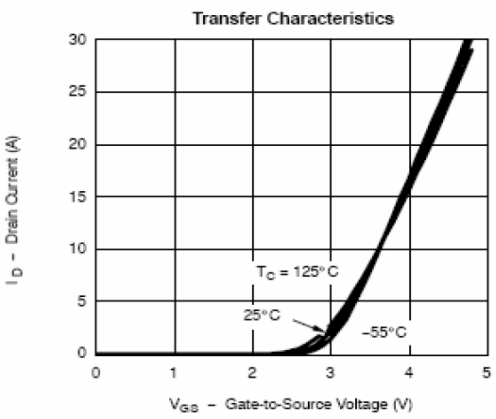
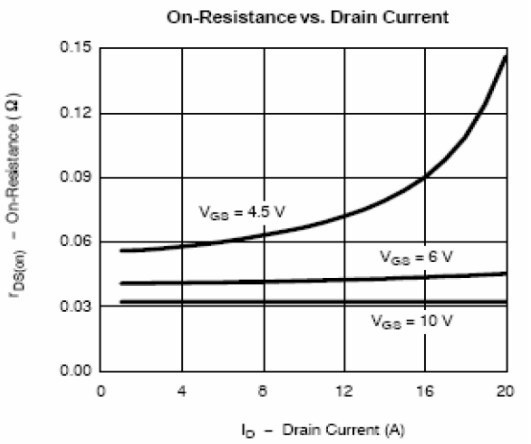
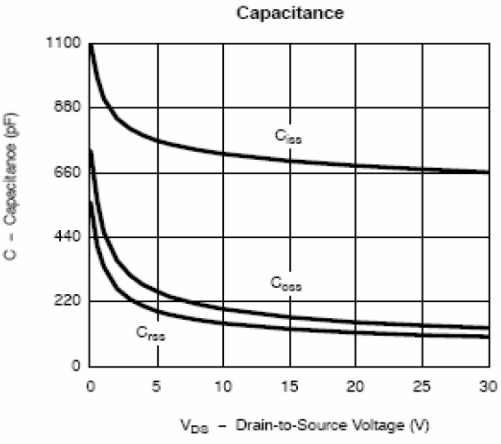
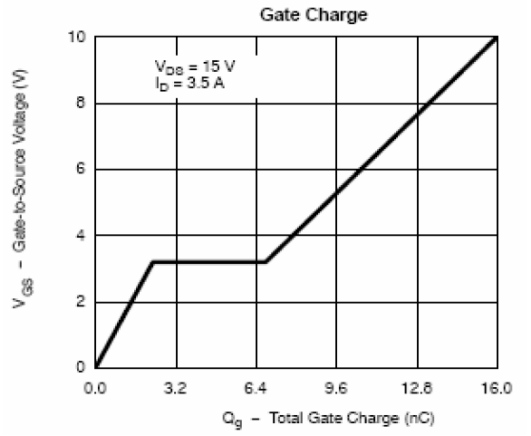
TYPICAL CHARACTERICTICS

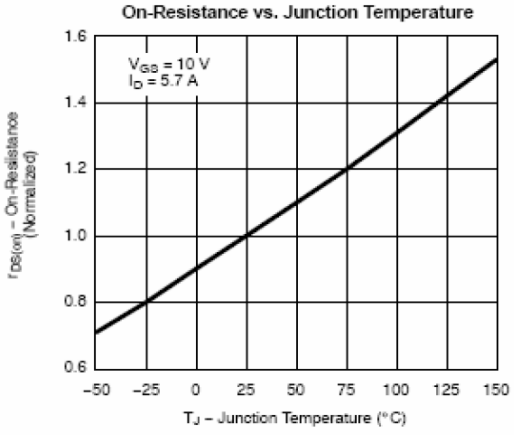












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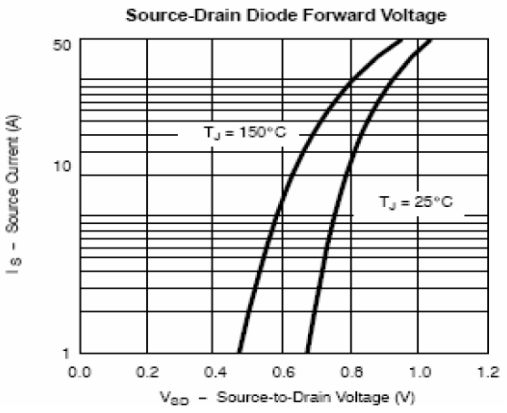

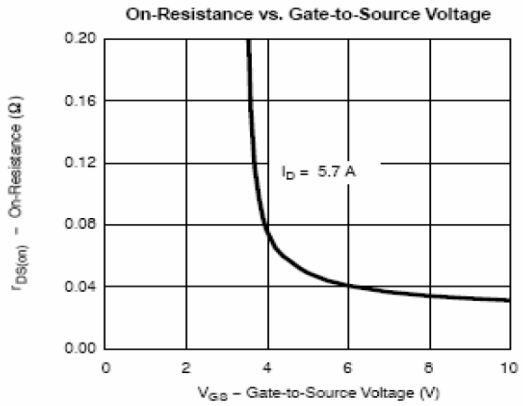

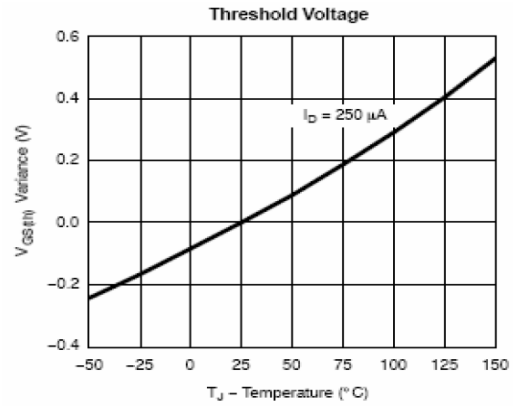

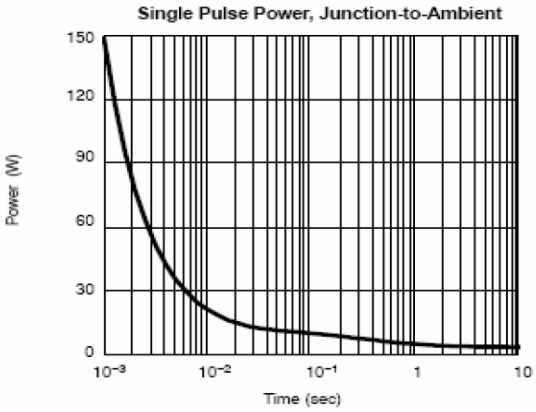

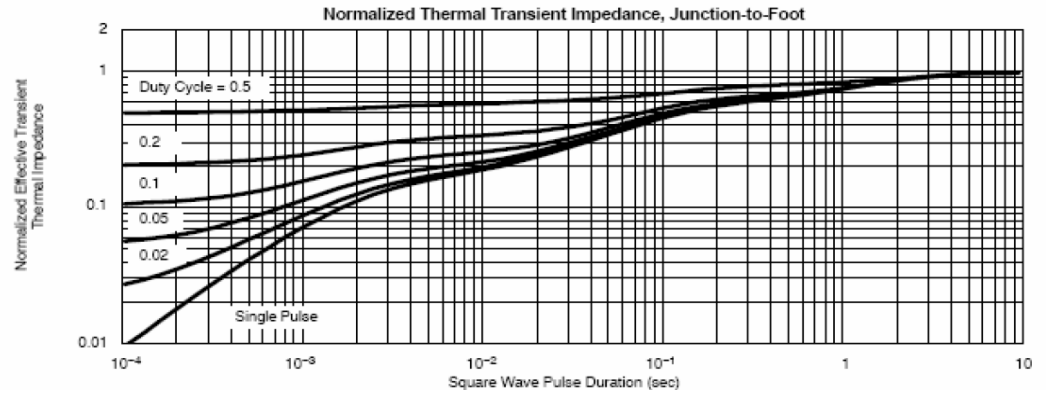

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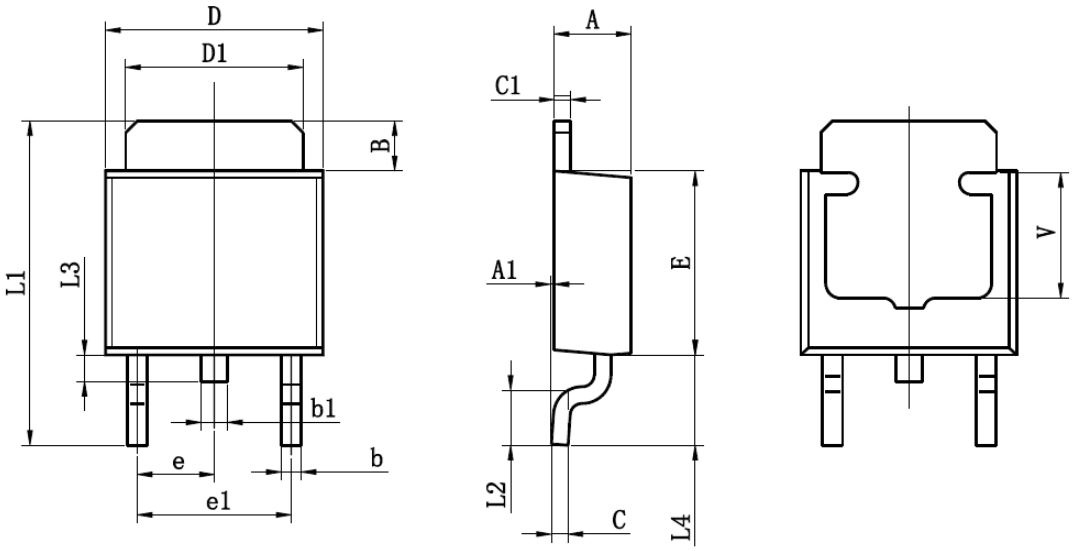
TO-252-2L PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
B	1.350	1.650	0.053	0.065
b	0.500	0.700	0.020	0.028
b1	0.700	0.900	0.028	0.035
c	0.430	0.580	0.017	0.023
c1	0.430	0.580	0.017	0.023
D	6.350	6.650	0.250	0.262
D1	5.200	5.400	0.205	0.213
E	5.400	5.700	0.213	0.224
e	2.300TYP		0.091TYP	
e1	4.500	4.700	0.177	0.185
L1	9.500	9.900	0.374	0.390
L2	1.400	1.780	0.055	0.070
L3	0.650	0.950	0.026	0.037
L4	2.550	2.900	0.100	0.114
V	3.80REF		0.150REF	

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