

## Audio/Video Switch Matrix

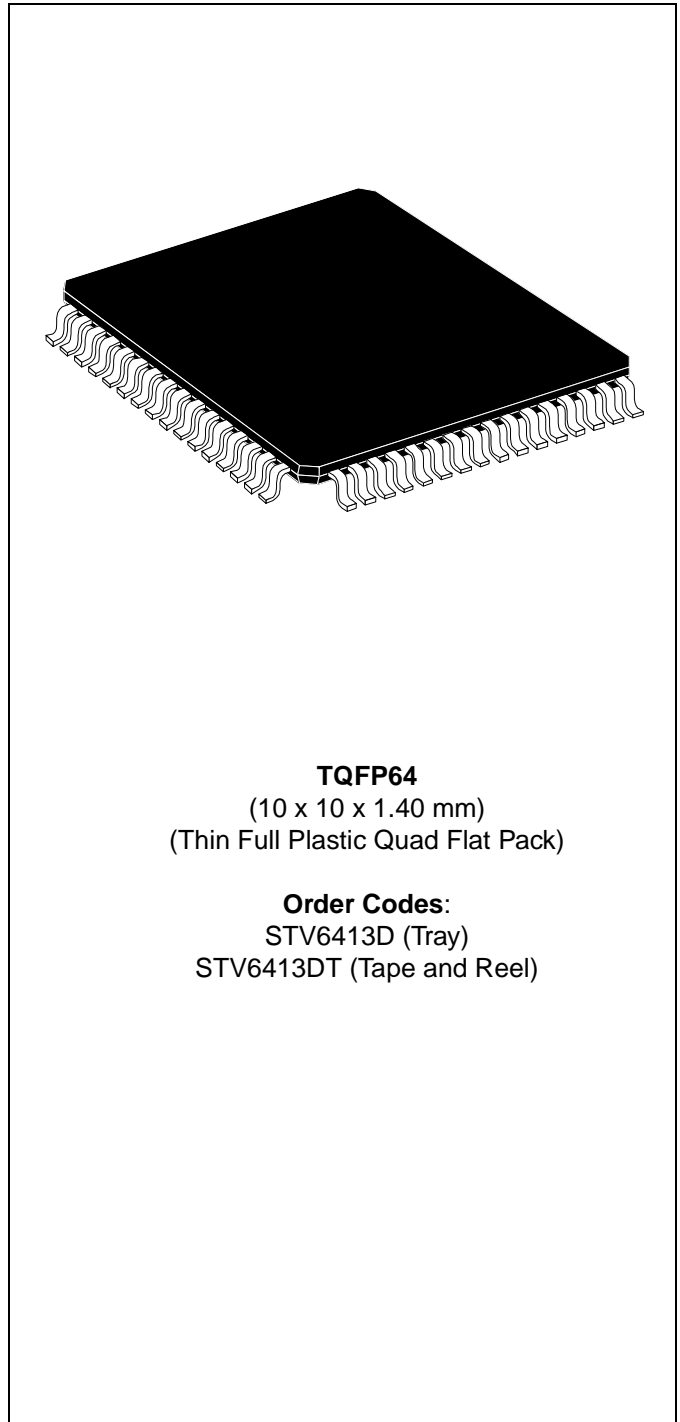
### Main Features

- **I<sup>2</sup>C Bus Control**
- **Standby Mode with Interrupt Signal Output**
- **Video Section**
  - 3 CVBS Inputs, 2 CVBS Outputs
  - 3 Y/C Inputs, 2 Y/C Outputs
  - 6 dB Gain on all CVBS/Y and C Outputs
  - Integrated 150  $\Omega$  Buffers
  - 2 RGB/FB Inputs, 1 Tri-state RGB/FB Output with 6 dB Adjustable Gain (from +3 dB to +9 dB)
  - Video Muting on all Outputs
  - 2 Slow Blanking Inputs/Outputs
  - Sync Bottom Clamp on all CVBS/Y and RGB Inputs, Average Clamp on C Inputs
  - Bandwidth: 15 MHz
  - Crosstalk: 50 dB Minimum
- **Audio Section**
  - 3 Stereo Inputs, 3 Stereo Outputs
  - Stereo-to-Mono Sound Capability
  - 0/6/9 dB Selectable Gain on one Stereo Input
  - Full Range Volume Control with Soft Control
  - Audio Muting on all Outputs

### Description

The STV6413 is a highly integrated I<sup>2</sup>C bus-controlled audio and video switch matrix, optimized for use in digital set-top box applications. It provides the audio and video routings required in a two SCART set-top box design.

In a TQFP64 (10 x 10 mm) package, the STV6413 is compatible with the STV6412A (TQFP64 14 x 14 mm) used for designing boards with two levels of integration.

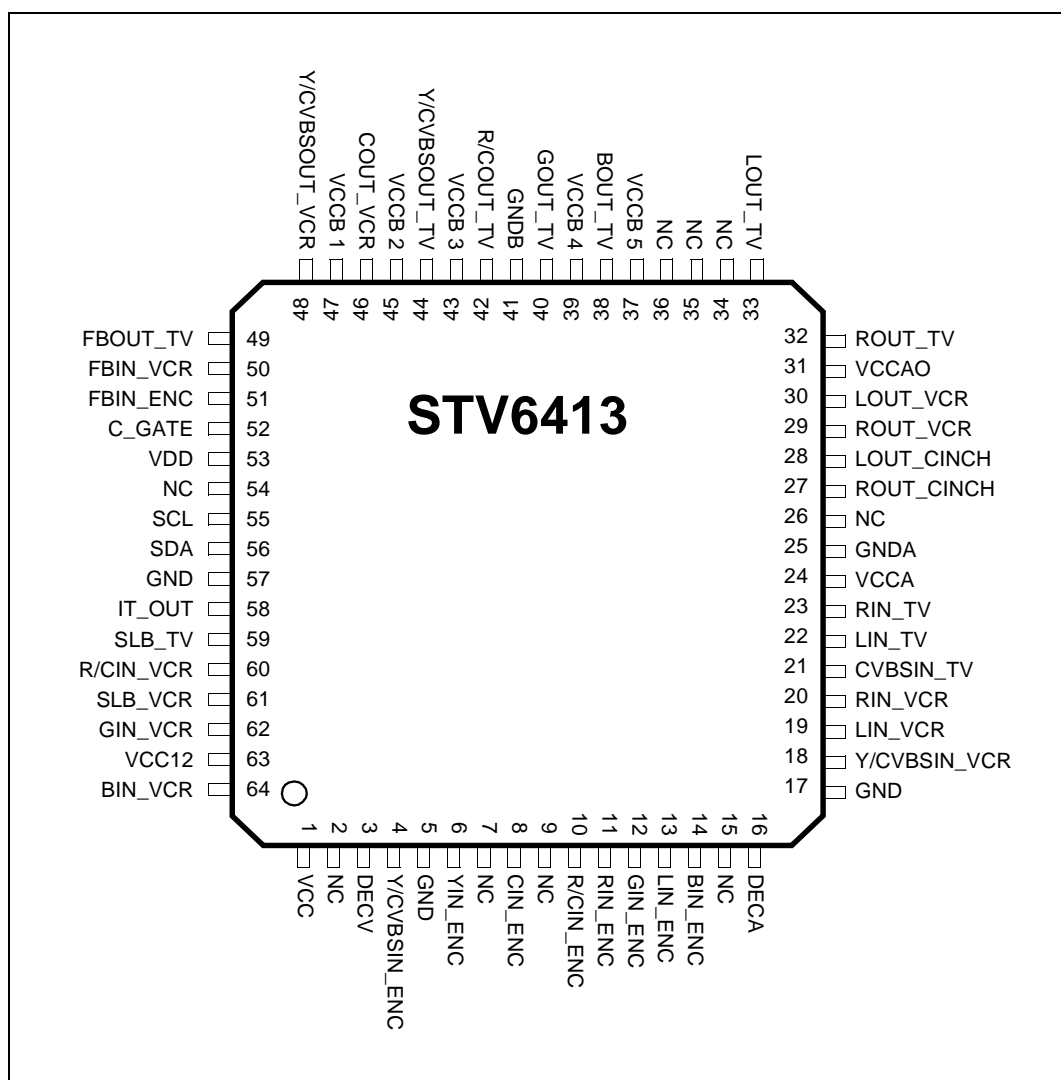


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# 1 General Information

Figure 1: STV6413 Pinout Diagram



## 1.1 I/O Pin Description

Table 1: Pin Description (Sheet 1 of 3)

Pin No.	Name	Function
1	VCC	+5 V Supply
2	NC	Not connected
3	DECV	Video Decoupling Capacitor
4	Y/CVBSIN_ENC	Y/CVBS Input from Encoder
5	GND	Ground
6	YIN_ENC	Y Input from Encoder
7	NC	Not connected

Table 1: Pin Description (Sheet 2 of 3)

Pin No.	Name	Function
8	CIN_ENC	Chroma Input from Encoder
9	NC	Not connected
10	R/CIN_ENC	Red/Chroma Input from Encoder
11	RIN_ENC	Audio Right, Input from Encoder
12	GIN_ENC	Green Input from Encoder
13	LIN_ENC	Audio Left, Input from Encoder
14	BIN_ENC	Blue Input from Encoder
15	NC	Not Connected
16	DECA	Audio Decoupling Capacitor
17	GND	Ground
18	Y/CVBSIN_VCR	Y/CVBS Input from VCR SCART
19	LIN_VCR	Audio Left, Input from VCR SCART
20	RIN_VCR	Audio Right, Input from VCR SCART
21	CVBSIN_TV	CVBS Input from TV SCART
22	LIN_TV	Audio Left, Input from TV SCART
23	RIN_TV	Audio Right, Input from TV SCART
24	VCCA	Audio Supply Voltage - or - Audio Supply Decoupling
25	GNDA	Audio Ground
26	NC	Not Connected
27	ROUT_CINCH	Audio Right Output to Cinch
28	LOUT_CINCH	Audio Left Output to Cinch
29	ROUT_VCR	Audio Right Output to VCR SCART
30	LOUT_VCR	Audio Left Output to VCR SCART
31	VCCAO	Audio Output Supply Voltage - or - Main Audio Supply Voltage
32	ROUT_TV	Audio Right Output to TV SCART
33	LOUT_TV	Audio Left Output to TV SCART
34	NC	Not connected
35	NC	Not connected
36	NC	Not connected
37	VCCB5	Video Output Buffer Supply Pin
38	BOUT_TV	Blue Output to TV SCART
39	VCCB4	Video Output Buffer Supply Pin
40	GOUT_TV	Green Output to TV SCART
41	GNDB	Video Buffer Ground
42	R/COUT_TV	Red/Chroma Output to TV SCART

Table 1: Pin Description (Sheet 3 of 3)

Pin No.	Name	Function
43	VCCB3	Video Output Buffer Supply Pin
44	Y/CVBSOUT_TV	Y/CVBS Output to TV SCART
45	VCCB2	Video Output Buffer Supply Pin
46	COUT_VCR	Chroma Output to VCR SCART
47	VCCB1	Video Output Buffer Supply Pin
48	Y/CVBSOUT_VCR	Y/CVBS Output to VCR SCART
49	FBOUT_TV	Fast Blanking Output to TV SCART
50	FBIN_VCR	Fast Blanking Input from VCR SCART
51	FBIN_ENC	Fast Blanking Input from Encoder
52	C_GATE	External MOS Command for C_VCR bidirectional mode
53	VDD	+5 V I <sup>2</sup> C Supply
54	NC	Not connected
55	SCL	I <sup>2</sup> C Bus Clock
56	SDA	I <sup>2</sup> C Bus Data
57	GND	Ground Digital
58	IT_OUT	Interrupt Output
59	SLB_TV	Slow Blanking Input/Output from TV SCART
60	R/CIN_VCR	Red Input (or C Input) from VCR SCART
61	SLB_VCR	Slow Blanking Input/Output from VCR SCART
62	GIN_VCR	Green Input from VCR SCART
63	VCC12	+12 V Supply
64	BIN_VCR	Blue Input from VCR SCART

Figure 2: STV6413 Block Diagram

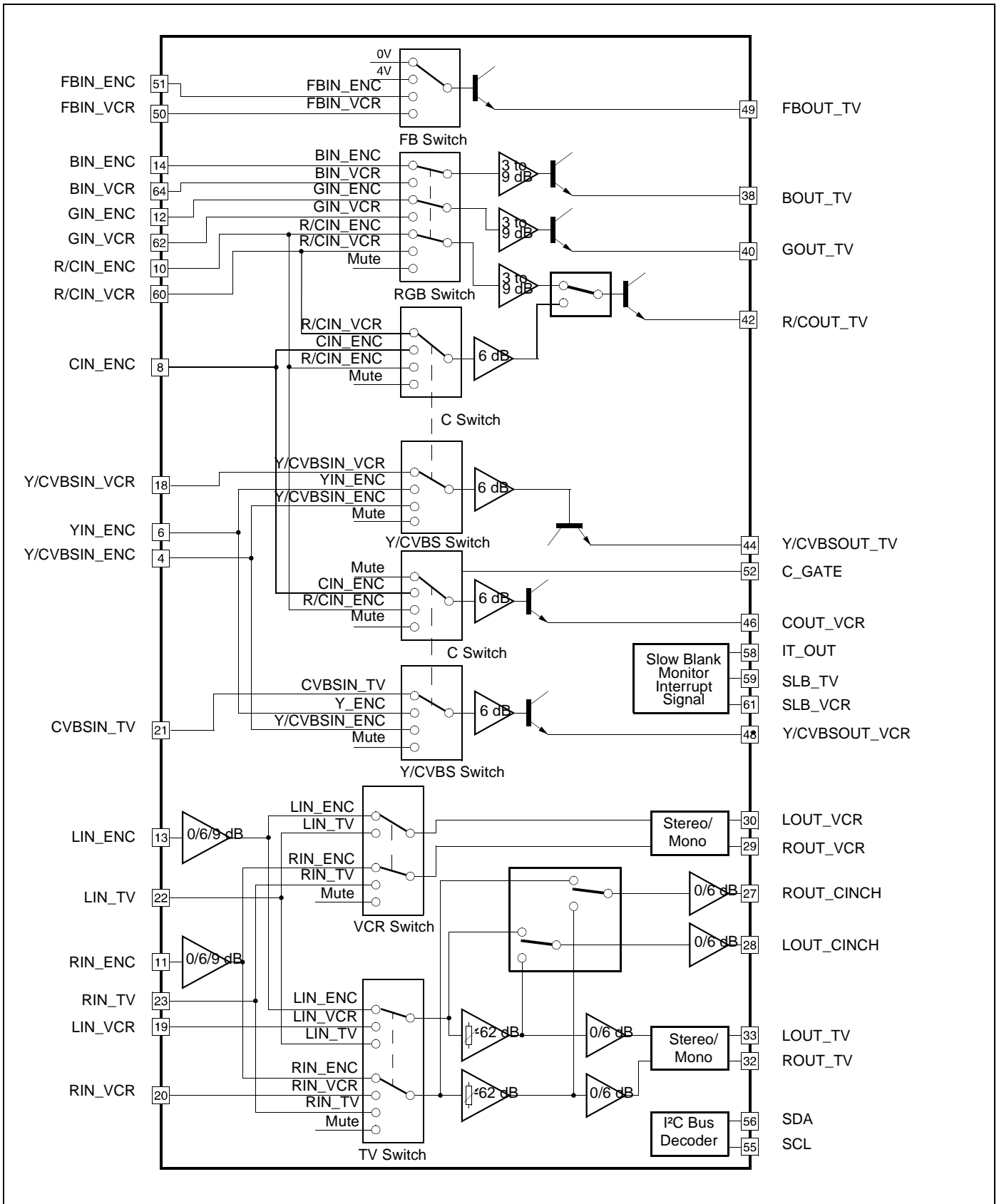
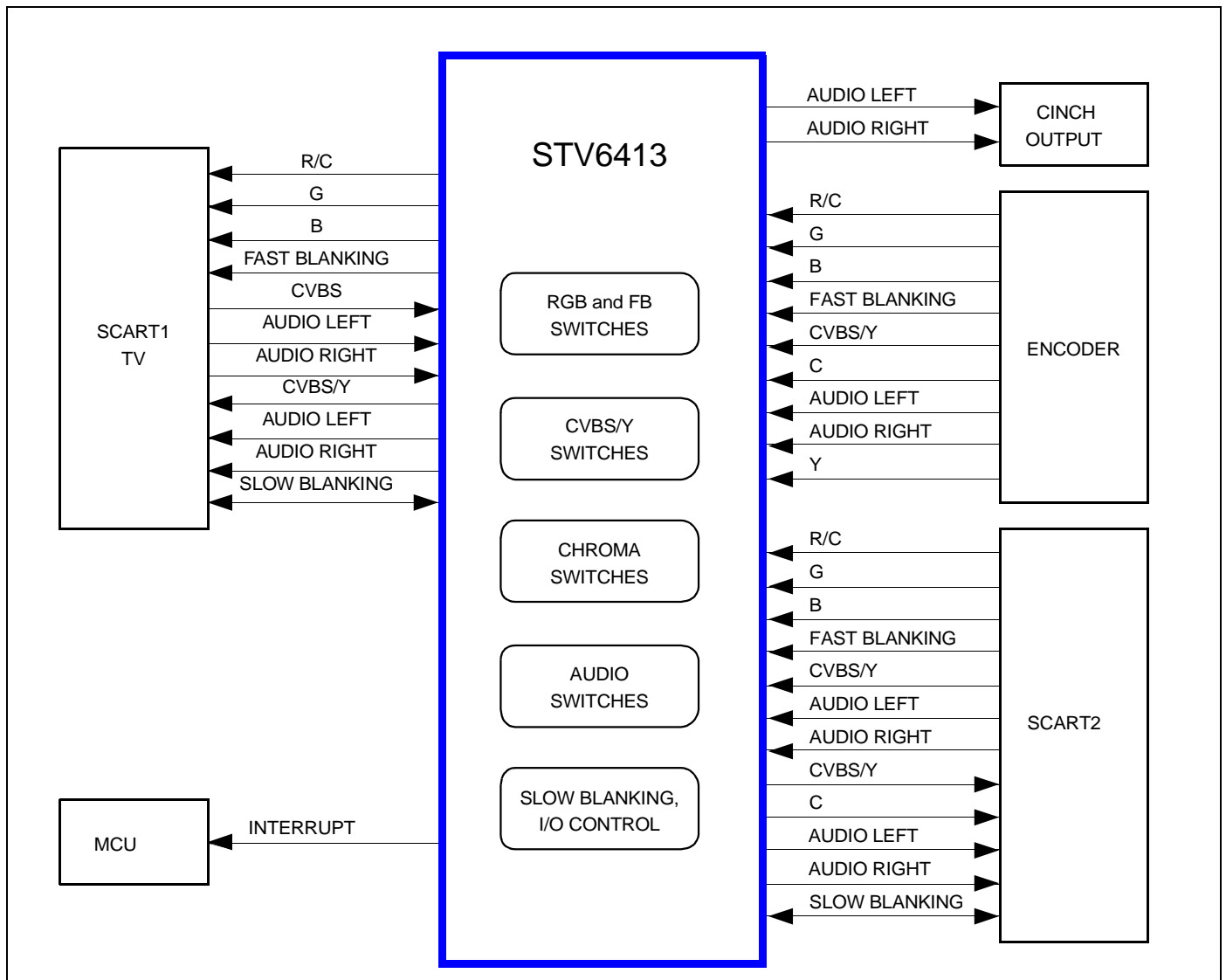


Figure 3: STV6413 Functional Diagram



## 2 Electrical Characteristics

### 2.1 Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
$V_{CC12}$	Supply voltage for Slow Blanking sections		13.2	V
$V_{CCAO}$	Supply voltage for Audio Drivers		13.2	V
$V_{CCA}$	Supply voltage for Digital Audio sections		10	V
$V_{DD}$	Supply voltage for Digital sections		6	V
$V_{CC}$ , $V_{CCBI}$	Supply voltage for Video sections		6	V
$V_{IN}$	Input Voltage at Pin (in reference to GND)	Audio pins Video pins Bus pins Slow Blanking pins	0, $V_{CCA}$ 0, $V_{CC}$ or $V_{CCBI}$ 0, 5.5 0, $V_{CC12}$	V
$V_{ESD}$	Maximum ESD Voltage allowed. (Human Body Model: 100 pF capacitor discharged through 1.5 kOhm serial resistor)		±4	kV
$T_{OPER}$	Ambient Operating Temperature		0 to +70	°C
$T_{STG}$	Storage Temperature		-20 to +150	°C

### 2.2 Thermal Data

Symbol	Parameter	Value	Unit
$R_{thJC}$	Junction-to-Case Thermal Resistance		°C/W
$R_{thJA}$	Junction-to-Ambient Thermal Resistance <sup>1</sup>	48	°C/W
$T_J$	Maximum Recommended Junction Temperature		°C

1. Measured on 4-layer application board.

### 2.3 Latch-up Data

At an ambient temperature of 25 °C, all pins meet the following specifications:

- $I_{trigger} = 200$  mA or  $I_{trigger} = -200$  mA.
- Pin 58 (IT\_OUT) does not meet this specification and the trigger current must be limited to 100 mA.



## 2.4 Electrical Characteristics

$T_{AMB} = 25^{\circ} C$ ,  $V_{CCA0} = 12 V$ ,  $V_{CC} = 5 V$ ,  $V_{CC12} = 12 V$ ,  $V_{DD} = 5 V$

$R_{GA} = 600 \Omega$ ,  $R_{GV} = 50 \Omega$ ,  $R_{LOUTA} = 10 k\Omega$ ,  $R_{LOUTV} = 150 \Omega$  (unless otherwise specified).

### Supply Section

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{DD}$	Digital Supply Voltage		4.75	5	5.25	V
$V_{CCA0}$	Audio Operating Supply Voltage	- Decoupling capacitor on $V_{CCA}$ - Connected to $V_{CCA}$	11.2 8.5	12 9	12.8 9.5	V
$V_{CC}$	Video Operating Supply Voltage		4.75	5	5.25	V
$V_{CC12}$	Slow Blanking Control Supply Voltage		11.2	12	12.8	V

### Active Mode (All channels ON)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{DD}$	Digital Supply Current	$V_{DD} = 5 V$		4.5	10	mA
$I_{CCA}$	Audio Supply Current	$V_{CCA0} = 12 V$ , No Load		9	15	mA
$I_{CCV}$	Total Video Supply Current ( $V_{CC} + V_{CCB1} + V_{CCB2} + V_{CCB3} + V_{CCB4} + V_{CCB5}$ )	$V_{CC} = 5 V$ , No Load		43	60	mA
$I_{CC12}$	12 V Supply Current	$V_{CC12} = 12 V$ SLB input mode SLB output mode, No Load		0 2.5	1 4	mA

### Standby Mode (All channels OFF)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{DD}$	Digital Supply Current	$V_{DD} = 5 V$		4.5	10	mA
$I_{CCASTD}$	Audio Supply Current	$V_{CCA0} = 12 V$ , No Load		3		mA
$I_{CCVSTD}$	Total Video Supply Current	$V_{CC} = 5 V$ , No Load		1		mA

### Audio Section

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SVR100	Supply Voltage Rejection	$V_{RIPPLE} = 500 mV_{RMS}$ at 100 Hz, Gain = 0 dB DECA filter cap = 47 $\mu F$ DECA filter cap = 220 $\mu F$	60	70 80		dB
SVR1K	Supply Voltage Rejection	$V_{RIPPLE} = 500 mV_{RMS}$ at 1 kHz, Gain = 0 dB	70	80		dB

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>INDC</sub>	Input DC Level	V <sub>CCA</sub> = 9 V		V <sub>CCA/2</sub>		V
V <sub>INAC</sub>	Input Signal Amplitude				2	V <sub>RMS</sub>
R <sub>IN</sub>	Input Resistance		30	50		kΩ
R <sub>INmatch</sub>	Input Resistance Matching			±2	±10	%
F <sub>RANGE</sub>	Bandwidth	-3 dB, 0.5 V <sub>RMS</sub> , R <sub>LOAD</sub> = 10 kΩ, Gain = 0 dB	50			kHz
Flatness	Spread of Gain in Audio Band	-0.5 V <sub>RMS</sub> , 20 Hz to 20 kHz, Gain = 0 dB			0.5	dB
CS	Channel Separation, from audio inputs Between L & R of TV outputs	V <sub>IN</sub> = 0.5 V <sub>RMS</sub> at 1 kHz on one input, R <sub>LOAD</sub> = 10 kΩ, Gain = 0 dB	80 70	90 74		dB dB
C <sub>i</sub>	Channel Isolation from video inputs	V <sub>IN</sub> = 1 V <sub>PP</sub> at 15 kHz on one point		85		dB
V <sub>OUT</sub>	Output DC Level	V <sub>CCA</sub> = 9 V		V <sub>CCA/2</sub>		V
V <sub>OFF</sub>	DC Offset Change	Switching between inputs		1	±15	mV
R <sub>OUT</sub>	Output Resistance			60	120	Ω
PHD	Phase Difference	1 V <sub>RMS</sub> input on each input channel at 1 kHz			3	° deg.
ASN	S/N Ratio	V <sub>IN</sub> = 1 V <sub>RMS</sub> at 1 kHz input weighted CCIR 468-4 quasi peak, Gain = 0 dB	80	90		dB
eNI	Equivalent RMS Input Voltage Noise	BW = 20 Hz, 20 kHz Flat, Gain = 0 dB		5		μV
G <sub>0</sub>	0 dB Gain	0.5 V <sub>RMS</sub> , R <sub>LOAD</sub> = 10 kΩ, Gain = 0 dB	-0.5		+0.5	dB
G <sub>STEP</sub>	Gain Step	-62 dB to +6 dB (see Figure 2)		2		dB
G <sub>MATCH1</sub>	Gain matching between different inputs of one output	V <sub>IN</sub> = 0.5 V <sub>RMS</sub> at 1 kHz, Gain = 0 dB	-0.5		0.5	dB
G <sub>MATCH2</sub>	Gain matching between Left/Right outputs of one input channel	V <sub>IN</sub> = 0.5 V <sub>RMS</sub> at 1 kHz, Gain = 0 dB	-0.5		0.5	dB
THD <sub>0</sub> THD <sub>6</sub> THD <sub>9</sub>	Total Harmonic Distortion ENC Input at 0 dB ENC Input at 6 dB ENC Input at 9 dB	V <sub>OUT</sub> = 0.5 V <sub>RMS</sub> at 1 kHz, LPF at 80 kHz, Volume Level Adjustment = 0 dB		0.01 0.01 0.01	0.05 0.05 0.05	%
V <sub>CL</sub>	Output Clipping Level	THD = 0.2%, 1 kHz	2.1	2.3		V <sub>RMS</sub>
R <sub>L</sub>	Output Load Resistance	V <sub>IN</sub> = 1 V <sub>RMS</sub> , THD = 0.3%, Gain = 0 dB	2	2.25		kΩ
Mute	Mute Suppression	V <sub>IN</sub> = 0.5 V <sub>RMS</sub> , on one point	90			dB

## Video Section

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{DCIN}$	DC Input Level	Bottom Sync Pulse		2		V
$I_{CLAMP}$	Clamping Current	at $V_{DCIN} - 400$ mV	1	2		mA
$I_{LEAK}$	Input Leakage Current	$V_{IN} = V_{DCIN} + 1$ V		1	10	$\mu$ A
$C_{IN}$	Input Capacitance			2		pF
$V_{IN}$	Max Input Signal	$V_{CC} = 5$ V		1.5		$V_{PP}$
DYN	Dynamic Output Signal	$V_{CC} = 5$ V		3		$V_{PP}$
BW	Bandwidth at -3 dB - Y/CVBS - RGB	$V_{IN} = 1 V_{PP}$ $V_{IN} = 1 V_{PP} V_{INC} = \text{muted}$	12 12	15 15		MHz
Flatness	Spread of Gain in Video Band (15 kHz - 5 MHz) - Y/CVBS - RGB	$V_{IN} = 1 V_{PP}$ $V_{IN} = 1 V_{PP} V_{INC} = \text{Muted}$			$\pm 0.5$ $\pm 0.5$	dB
CTi	Crosstalk Isolation between Input Channel	$V_{IN} = 1 V_{PP}$ at 4.43 MHz on one point		60		dB
CTo	Crosstalk Isolation between Output Channel	$V_{IN} = 1 V_{PP}$ at $f = 4.43$ MHz, on one point, $R_{LOAD} = 150\Omega$		50		dB
$R_{OUT}$	Output Resistance			5	10	$\Omega$
$G_{RGB}$	Gain at RGB outputs	$V_{IN} = 1 V_{pp}$ , Gain = 6 dB	5.5	6	6.5	dB
$G_{RGBM}$	Gain matching between R, G, B	$V_{IN} = 1 V_{pp}$ , Gain = 6 dB	-0.3	0	0.3	dB
$G_{RGBSTEP}$	Step of Gain	3 dB to 6 dB	0.75	1	1.25	dB
$G_{YCVBS}$	Gain on Y, CVBS channels	$V_{IN} = 1 V_{PP}$	5.5	6	6.5	dB
$G_{YCVBSM}$	Gain matching between Y, CVBS inputs	$V_{IN} = 1 V_{PP}$	-0.5	0	0.5	dB
$DC_{OUT}$	DC Output Voltage	Bottom sync pulse		0.6		V
DPHI	Differential Phase	$V_{IN} = 1 V_{PP}$ at 4.43 MHz		1	5	$^{\circ}$ deg.
DG	Differential Gain	$V_{IN} = 1 V_{PP}$ at 4.43 MHz		1	5	%
Mute	Mute Suppression	$V_{IN} = 1 V_{PP}$ at 5 MHz on one point	55			dB
LNL	Luminance non-linearity			0.3	3	%
VSN	Video S/N Ratio	Refer to <a href="#">Note 1</a>	65			dB

Note: 1  $S/N = 20 \log (V_{OUT} \text{ Black to White} = 0.7 V_{PP} / V_{Noise} (mV_{RMS}) \text{ weighted CCIR 567})$ .

## Chroma Section

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>DCIN</sub>	DC Input Level			3		V
R <sub>IN</sub>	Input Resistance		30	50		kΩ
C <sub>IN</sub>	Input Capacitance			2		pF
V <sub>IN</sub>	Max Input Signal			1.5		V <sub>PP</sub>
DYN	Dynamic Output Signal			3		V <sub>PP</sub>
DC <sub>OUT</sub>	DC Output VCR Voltage			2.2		V
CBW	Chroma Bandwidth	C <sub>IN</sub> = 1 V <sub>PP</sub> at -3 db	10			MHz
CTi	Crosstalk Isolation between Input Channel	V <sub>IN</sub> = 1 V <sub>PP</sub> at 4.43 MHz on one input		55		dB
CTo	Crosstalk Isolation between Output Channel	V <sub>IN</sub> = 1 V <sub>PP</sub> at 4.43 MHz on one input, R <sub>LOAD</sub> = 150 Ω		50		dB
R <sub>OUT</sub>	Output Resistance			5	10	Ω
G <sub>OUTC</sub>	Gain at OUTC	V <sub>IN</sub> = 1 V <sub>pp</sub>	5.5	6	6.5	dB
G <sub>CM</sub>	Gain Matching between C inputs	V <sub>IN</sub> = 1 V <sub>PP</sub>	-0.5	0	0.5	dB
Mute	Mute Suppression	V <sub>IN</sub> = 1 V <sub>PP</sub> at 4.43 MHz on one input	55			dB
CToYdel	Chroma to Luma Delay, Source Y/C	V <sub>PP</sub> at 4.43 MHz,			20	ns
CToYdel	Chroma to Luma Delay, Source Y/C				20	ns

## Slow Blanking Section

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
<b>Input Mode</b>						
SLBlow	Input Low Level Threshold		2.5	3.25	4	V
SLBhigh	Input High Level Threshold		7.5	8.25	9	V
I <sub>IN</sub>	Input Current			50	100	μA
<b>Output Mode</b>						
SLBlow	Output Low Level (Int. TV)		0	0.02	1.5	V
SLBmed	Output Medium Level (Ext. 16:9)		5	5.75	6.5	V
SLBhigh	Output High Level (Ext. 4:3)		10	11	12	V

## Fast Blanking Section

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
<b>Input Mode</b>						
FB <sub>low/high</sub>	Input Low/High Level Threshold		0.4	0.7	0.9	V
I <sub>IN</sub>	Input Current			2	10	μA
<b>Output Mode</b>						
FB <sub>LOW</sub>	Output Low Level	R <sub>LOAD</sub> = 150 Ω			0.5	V
FB <sub>HIGH</sub>	Output High Level		3.0	3.4	3.8	V
FB <sub>DEL</sub>	Fast Blanking RGB delay	At 50% on digital RGB transients, at 2 V on FB rise transient, at 1 V on FB fall, C <sub>LOAD</sub> = 10pF maximum		15		ns
FB <sub>TRANS</sub>	FB Transitions at FB output - Rise Time - Fall Time	C <sub>LOAD</sub> = 10 pF maximum between 10% and 90% between 90% and 10%		10 10		ns

## C\_Gate Function Output Section

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
C_GATE-H	Pull-up Resistor Value to V <sub>CCB1</sub>			20		kΩ
C_GATE-L	Output Low Level	I <sub>IN</sub> = 0 mA I <sub>IN</sub> = 1 mA			0.3 0.7	V

Interrupt Output Section<sup>1</sup>

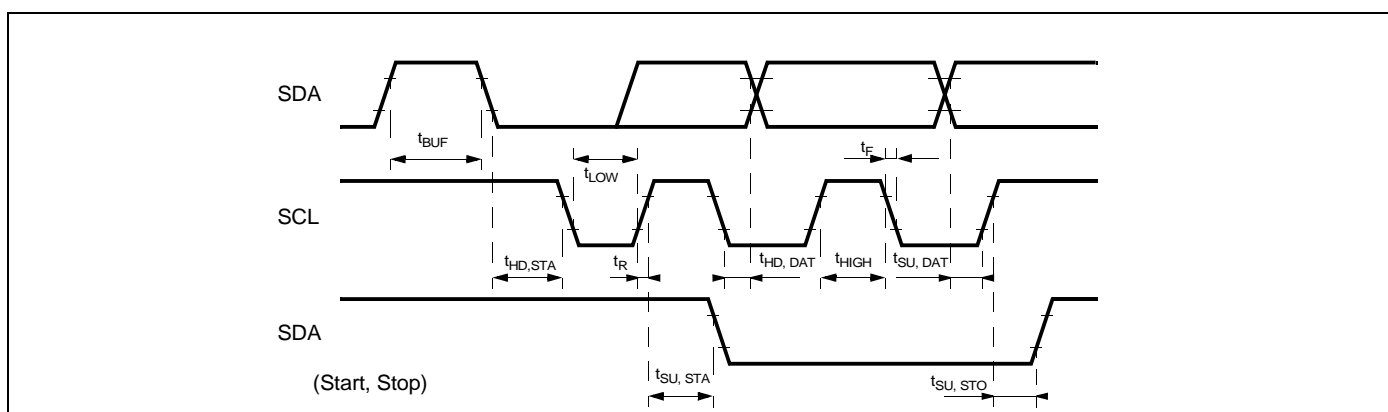
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
IT-Leak	High Level Leakage	External pull-up to 5 V			10	μA
IT-Low	Output Low Level (Active)	I <sub>IN</sub> = 0 mA I <sub>IN</sub> = 1 mA			0.3 0.7	V

1. When bit IT Enable is set, the interrupt is forced to a low level when a change is detected on slow blanking inputs. It can be used in standby mode to wake up the microprocessor. It is released when the I<sup>2</sup>C bus register is read.

I<sup>2</sup>C Bus Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
<b>SCL</b>						
V <sub>IL</sub>	Low Level Input Voltage		-0.3		1.5	V
V <sub>IH</sub>	High Level Input Voltage		2.3		5.5	V
I <sub>LI</sub>	Input Leakage Current	V <sub>IN</sub> = 0 to 5.5 V	-10	0	10	μA
<b>SDA</b>						
V <sub>IL</sub>	Low Level Input Voltage		-0.3		1.5	V
V <sub>IH</sub>	High Level Input Voltage		2.3		5.5	V
I <sub>LI</sub>	Input Leakage Current	V <sub>IN</sub> = 0 to 5.5 V	-10	0	10	μA
C <sub>I</sub>	Input Capacitance				10	pF
t <sub>R</sub>	Input Rise Time	1.5 V to 3 V			1	μs
t <sub>F</sub>	Input Fall Time	3 V to 1.5 V			300	ns
V <sub>OL</sub>	Low Level Output Voltage	I <sub>OL</sub> = 3 mA			0.4	V
t <sub>F</sub>	Output Fall Time	3 V to 1.5 V			250	ns
C <sub>L</sub>	Load Capacitance				400	pF
<b>Timing</b>						
t <sub>LOW</sub>	Clock Low Period		4.7			μs
t <sub>HIGH</sub>	Clock High Period		4			μs
t <sub>SU,DAT</sub>	Data Setup Time		250			ns
t <sub>HD,DAT</sub>	Data Hold Time		0		340	ns
t <sub>SU,STO</sub>	Setup Time from Clock High to Stop		4			μs
t <sub>BUF</sub>	Start Setup Time following a Stop		4.7			μs
t <sub>HD,STA</sub>	Start Hold Time		4			μs
t <sub>SU,STA</sub>	Start Setup Time following Clock Low to High Transition		4.7			μs

Figure 4: I<sup>2</sup>C Bus Timing



### 3 I<sup>2</sup>C Bus Selection

Data transfers follow the usual I<sup>2</sup>C format; i.e. after the start condition (S), a 7-bit slave address is sent, followed by an eight-bit data direction bit (W). An 8-bit sub-address is sent to select a register, followed by an 8-bit data word to be included in the register. The IC's I<sup>2</sup>C bus decoder enables the automatic incrementation mode in write mode.

#### String Format

Write only mode (S = Start condition, P = Stop condition, A = Acknowledge)

S	Slave Address	0	A	Sub-address	A	Data	A	P
---	---------------	---	---	-------------	---	------	---	---

Read only mode

S	Slave Address	1	A	Data	A	P
---	---------------	---	---	------	---	---

Slave Address

Address	A7	A6	A5	A4	A3	A2	A1
Value	1	0	0	1	0	1	1

Auto Increment Mode

S	Slave Address	0	A	Sub-address	A	Data0	A	Data1	A	...	Data n	A	P
						Sub-address		Sub-address + 1			Sub-address + N		

#### 3.1 I<sup>2</sup>C Bus Addresses

Write Address: 1001 0110 = 96(hex), Read Address: 1001 0111 = 97(hex)

**Table 2: Input Signal Summary (Write Mode)**

Reg. Add.	Data							
	d7	d6	d5	d4	d3	d2	d1	d0
<b>Audio</b>								
00h	TV Stereo Mono	TV 0/6 dB	TV Volume-62 dB to 0 dB - 2 dB steps					Soft Volume Mode
01h	VCR Stereo Mono	Not Used (See <a href="#">Note 1</a> )	VCR Audio Switch Control	CINCH Audio Gain	TV/CINCH Audio Switch Control			
<b>Video</b>								
02h	VCR Chroma muted	VCR Video and Chroma Switch Control			TV Chroma muted	TV Video and Chroma Switch Control		
03h	RGB and FB Tri-state	RGB Gain			RGB Switch Control		Fast Blanking Mode/Input Selection	

Table 2: Input Signal Summary (Write Mode)

Reg. Add.	Data							
	d7	d6	d5	d4	d3	d2	d1	d0
<b>Miscellaneous</b>								
04h	IT Enable	SLB Mode	Not Used (See Note 1)	VCR-C Output Control	VCR-C Gate Control	Not Used (See Note 1)	Not Used (See Note 1)	TV R or C Output Selection
05h	VCR Slow Blanking		TV Slow Blanking		ENC Audio Input Gain 0/6/9 dB		VCR R/C sub Clamp	ENC R/C sub Clamp
<b>Standby</b>								
06h	Not Used (See Note 1)	TV Outputs	CINCH Outputs	VCR Outputs	Not Used (See Note 1)	TV Inputs	VCR Inputs	ENC Inputs

Note: 1 At register address 06h, bits marked "Not Used" must be set to "1". All other bits marked "Not Used" must be set "0".

Table 3: TV Audio Output

Reg. Add.	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
00h	Soft Volume Change	1	X X	X X	X X	X X	X X	X X	X X	0 1	Active Disabled
	Level Adjustment	5	X X	X X	0 1	0 1	0 1	0 1	0 1	X X	0 dB -62 dB (-2 dB/step)
	6 dB Extra Gain	1	X X	0 1	X X	X X	X X	X X	X X	X X	0 dB +6 dB
	TV Stereo or Mono Mode	1	0 1	X X	X X	X X	X X	X X	X X	X X	0 = Stereo 1 = Mono



Table 4: Audio Selection &amp; VCR Audio Output

Reg. Add.	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
01h	TV & CINCH Audio Output Selection	3	X	X	X	X	X	0	0	0	Muted
			X	X	X	X	X	0	0	1	Encoder L/R selected
			X	X	X	X	X	0	1	0	VCR L/R selected
			X	X	X	X	X	0	1	1	Not allowed
X			X	X	X	X	1	0	0	TV L/R selected	
X			X	X	X	X	1	0	1	Not allowed	
X			X	X	X	X	1	1	0	Not allowed	
X	X	X	X	X	1	1	1	Not allowed			
01h	CINCH Audio Gain	1	X	X	X	X	0	X	X	X	0 dB
			X	X	X	X	1	X	X	X	Follow TV Gain
01h	VCR Audio Output Selection	2	X	X	0	0	X	X	X	X	Muted
			X	X	0	1	X	X	X	X	Encoder L/R selected
			X	X	1	0	X	X	X	X	TV L/R selected
01h	VCR Stereo or Mono Mode	1	0	X	X	X	X	X	X	X	0 = Stereo
			1	X	X	X	X	X	X	X	1 = Mono

Table 5: TV &amp; VCR Video Selection

Reg. Add.	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
02h	TV Video Output Selection	3	X	X	X	X	X	0	0	0	Y/CVBS muted & Chroma muted
			X	X	X	X	X	0	0	1	Y/CVBS_ENC & R/C_ENC
			X	X	X	X	X	0	1	0	Y_ENC & C_ENC
			X	X	X	X	X	0	1	1	Y/CVBS_VCR & R/C_VCR
			X	X	X	X	X	1	0	0	Not allowed
			X	X	X	X	X	1	0	1	Not allowed
			X	X	X	X	X	1	1	0	Not allowed
X	X	X	X	X	1	1	1	Not allowed			
02h	TV Chroma Output Control	1	X	X	X	X	0	X	X	X	Chroma defined by d2d1d0
			X	X	X	X	1	X	X	X	Chroma force to mute
02h	VCR Video Output Selection	3	X	0	0	0	X	X	X	X	Y/CVBS muted & Chroma muted
			X	0	0	1	X	X	X	X	Y/CVBS_ENC & R/C_ENC
			X	0	1	0	X	X	X	X	Y_ENC & C_ENC
			X	0	1	1	X	X	X	X	CVBS_TV & Chroma muted
			X	1	0	0	X	X	X	X	Not allowed
			X	1	0	1	X	X	X	X	Not allowed
			X	1	1	0	X	X	X	X	Not allowed
X	1	1	1	X	X	X	X	Not allowed			
02h	VCR Chroma Output Control	1	0	X	X	X	X	X	X	X	Chroma defined by d6d5d4
			1	X	X	X	X	X	X	X	Chroma force to mute

Table 6: RGB &amp; Fast Blanking Outputs

Reg. Add.	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
03h	Fast Blanking Control	2	X	X	X	X	X	X	0	0	FB forced to low level
			X	X	X	X	X	X	0	1	FB forced to high level
			X	X	X	X	X	X	1	0	FB from Encoder
			X	X	X	X	X	X	1	1	FB from VCR
	RGB Selection	2	X	X	X	X	0	0	X	X	Muted
			X	X	X	X	0	1	X	X	RGB_ENC selected
			X	X	X	X	1	0	X	X	RGB_VCR selected
			X	X	X	X	1	1	X	X	Not allowed
	RGB Gain	2	X	X	0	0	X	X	X	X	+6 dB gain
			X	X	0	1	X	X	X	X	+5 dB gain
			X	X	1	0	X	X	X	X	+4 dB gain
			X	X	1	1	X	X	X	X	+3 dB gain
		1	X	0	X	X	X	X	X	X	+0 dB extra gain
			X	1	X	X	X	X	X	X	X
	RGB and FB Control	1	0	X	X	X	X	X	X	X	RGB and FB outputs high impedance state
			1	X	X	X	X	X	X	X	X

Table 7: Miscellaneous Control

Reg. Add.	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
04h	R/C TV Output Selection	1	X	X	X	X	X	0	0	0	Red signal selected
			X	X	X	X	X	0	0	1	Chroma signal selected
	C_Gate Output Control	1	X	X	X	X	0	0	0	X	High level
			X	X	X	X	1	0	0	X	Low level
	C_VCR Output Control	1	X	X	X	0	X	0	0	X	Tri-state mode (high impedance)
X			X	X	1	X	0	0	X	Active	
Slow Blanking Mode	1	X	0	X	X	X	0	0	X	Normal Mode	
			X	1	X	X	X	0	0	X	SLB TV is driven by SLB VCR
IT Enable	1	0	X	X	X	X	0	0	X	No interrupt flag	
		1	X	X	X	X	0	0	X	IT enable	

Table 8: Slow Blanking &amp; Inputs Control

Reg. Add.	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
05h	Encoder R/Csub Clamp	1	X X	X X	X X	X X	X X	X X	X X	0 1	Bottom level clamp Average level clamp
	VCR R/Csub Clamp	1	X X	X X	X X	X X	X X	X X	0 1	X X	Bottom level clamp Average level clamp
	Encoder Input Level Adjustment	2	X X X	X X X	X X X	X X X	0 0 1	0 1 0	X X X	X X X	0 dB for normal audio inputs +6 dB for weak audio inputs +9 dB for weak audio inputs
	Slow Blanking TV SCART	2	X X X X	X X X X	0 0 1 1	0 1 0 1	X X X X	X X X X	X X X X	X X X X	Input mode only Output < 2 V Output 16/9 format Output 4/3 format
	Slow Blanking VCR SCART	2	0 0 1 1	0 1 0 1	X X X X	X X X X	X X X X	X X X X	X X X X	X X X X	Input mode only Output < 2 V Output 16/9 format Output 4/3 format

Table 9: Standby Modes

Reg. Add.	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
06h	ENC Inputs	1	1 1	X X	X X	X X	1 1	X X	X X	0 1	Inputs active Inputs disabled
	VCR Inputs	1	1 1	X X	X X	X X	1 1	X X	0 1	X X	Inputs active Inputs disabled
	TV Inputs	1	1 1	X X	X X	X X	1 1	0 1	X X	X X	Inputs active Inputs disabled
	VCR Outputs	1	1 1	X X	X X	0 1	1 1	X X	X X	X X	Audio & Video Outputs ON Audio & Video Outputs OFF
	CINCH Outputs	1	1 1	X X	0 1	X X	1 1	X X	X X	X X	Audio & Video Outputs ON Audio & Video Outputs OFF
	TV Outputs	1	1 1	0 1	X X	X X	1 1	X X	X X	X X	Audio & Video Outputs ON Audio & Video Outputs OFF
	Full Stop		1	1	1	1	1	1	1	1	1

Table 10: Output Signals (Read Mode)

Reg. Add.	Description	Bits	Data								Comments	
			d7	d6	d5	d4	d3	d2	d1	d0		
	Slow Blanking TV SCART	2	X	X	X	X	X	X	X	0	1	Input < 2 V Input 16/9 format Input 4/3 format
	Slow Blanking VCR SCART	2	X	X	X	X	0	1	X	X	X	Input < 2 V Input 16/9 format Input 4/3 format
	Interrupt Flag	1	X	X	X	0	X	X	X	X	X	No change since read One change has been detected (refer to <a href="#">Note 1</a> )

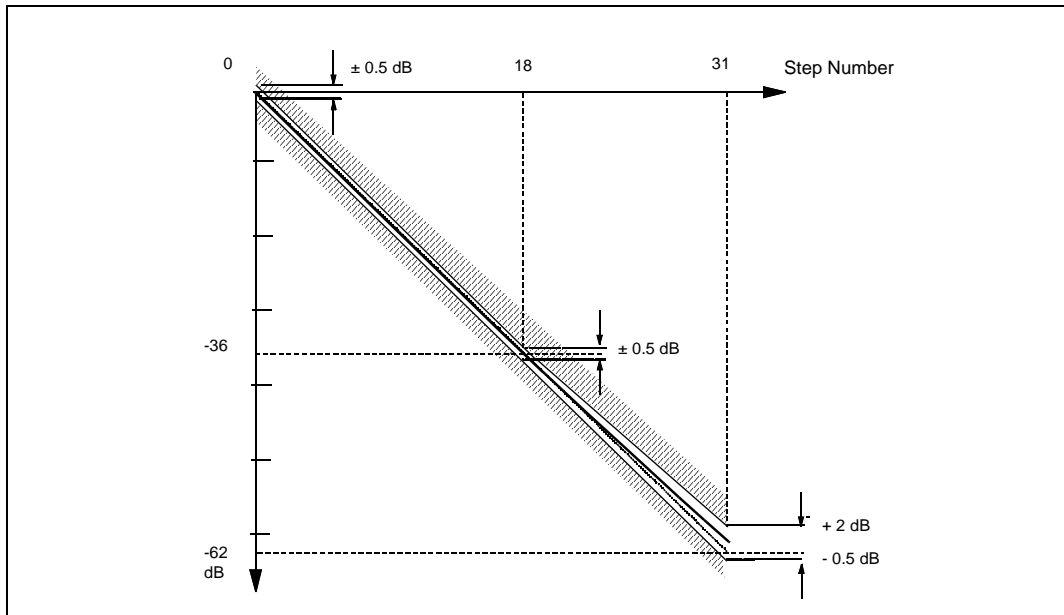
Note: 1 The Interrupt Flag will be cleared when this register is read. To prepare for a new interrupt, a “1” must be re-written in the IT Enable bit (Reg. 04, d7).

### 3.2 Power-on Reset — Bus Register Initial Conditions

Power-on Reset is active when the supply  $V_{DD}$  is less than 3.5 volts. Non-significant bits (X) are pre-set to “0”.

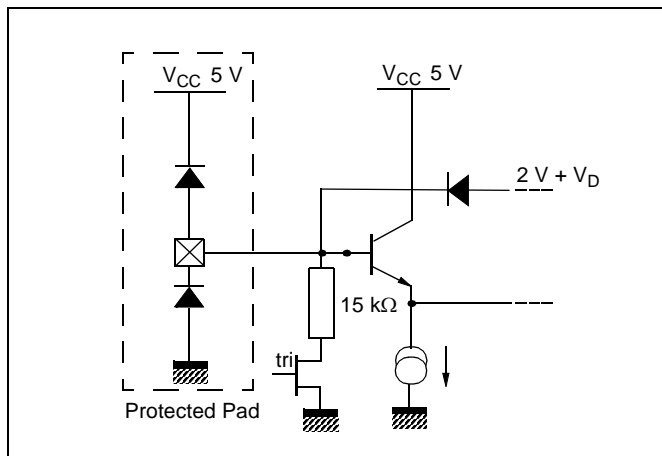
Reg. Add.	Data								Comments
	d7	d6	d5	d4	d3	d2	d1	d0	
00h	0	0	0	0	0	0	0	0	Audio TV and Cinch outputs are in Stereo Mode, 0 dB Gain Adjustment.
01h	0	0	0	0	0	0	0	0	TV, Cinch and VCR audio outputs are muted. VCR output is in Stereo Mode.
02h	0	0	0	0	0	0	0	0	VCR, TV video outputs are muted.
03h	0	0	0	0	0	0	0	0	Fast Blanking is forced to ‘0’. RGB outputs are muted and in high impedance.
04h	0	0	0	0	0	0	0	0	C_GATE is high. C_VCR is high impedance.
05h	0	0	0	0	0	0	0	0	Encoder and VCR R/Csub Bottom Level Clamp, RGB outputs 6 dB Gain, and Slow Blanking parts are in read mode.
06h	0	0	0	0	0	0	0	0	All internal blocks are ON.

Figure 5: Volume Control Characteristics

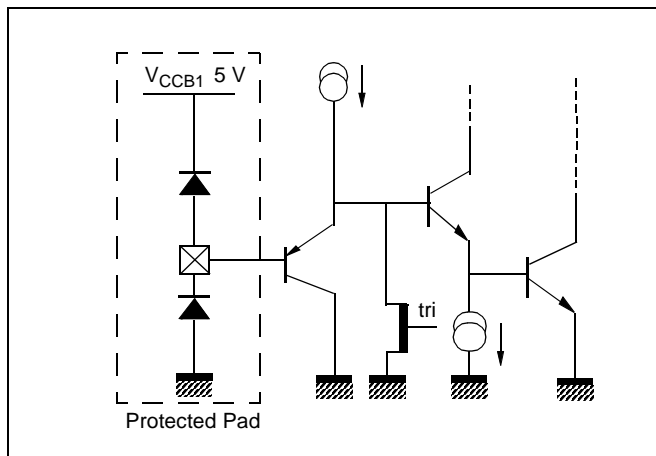


# 4 Input/Output Groups

**Figure 6: Bottom Clamped Video Inputs (Pins 4, 6, 12, 14, 18, 21, 62 and 64)**



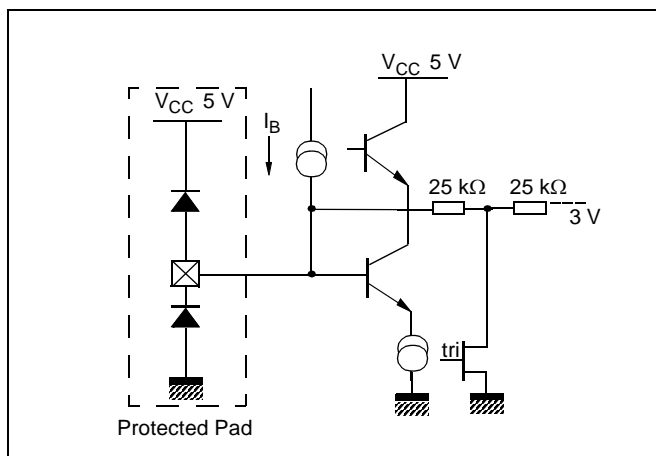
**Figure 9: Fast Blanking Inputs (Pins 50 and 51)**



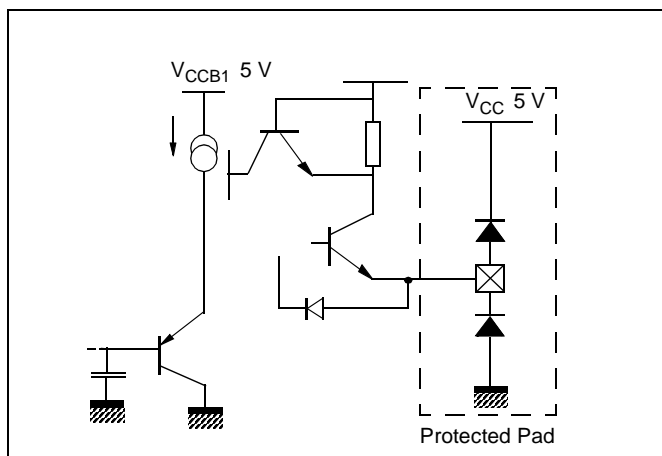
**Figure 7: R/C Clamped Video Inputs (Pins 10 and 60)**

R/C inputs may be configured either as a bottom clamped input or as an average clamped input. In either case, the simplified input schematic is very close to one of the graphics shown above.

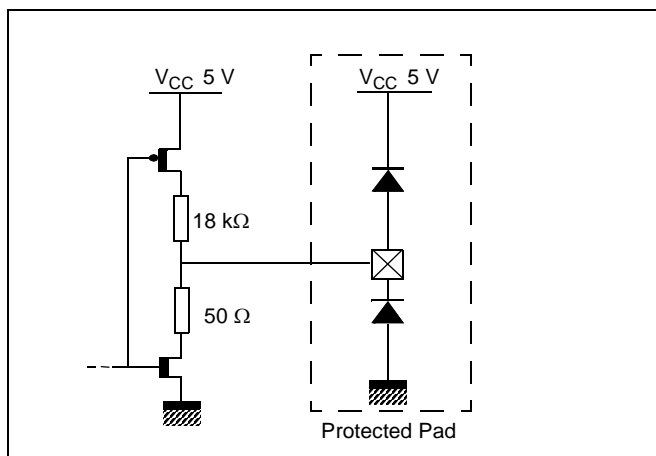
**Figure 10: Average Clamped Video Inputs (Pin 8)**



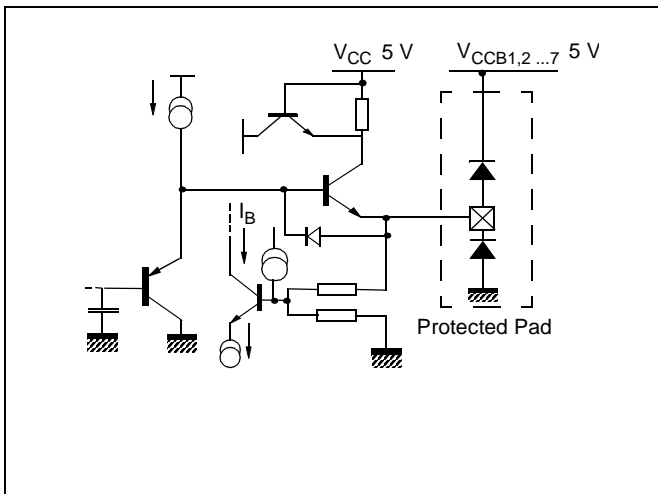
**Figure 8: Fast Blanking Output (Pin 49)**



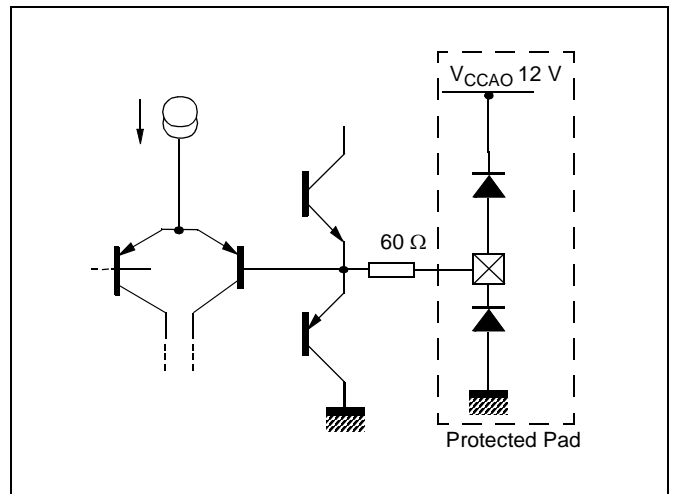
**Figure 11: Cgate Logical Output (Pin 52)**



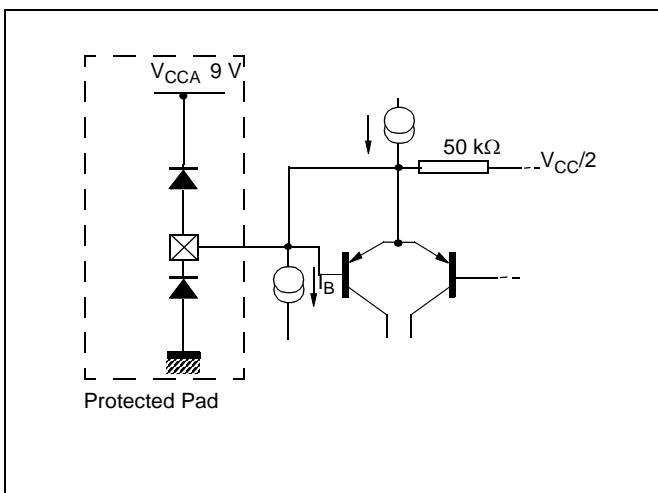
**Figure 12: Video Outputs**  
(Pins 38, 40, 42, 44, 46 and 48)



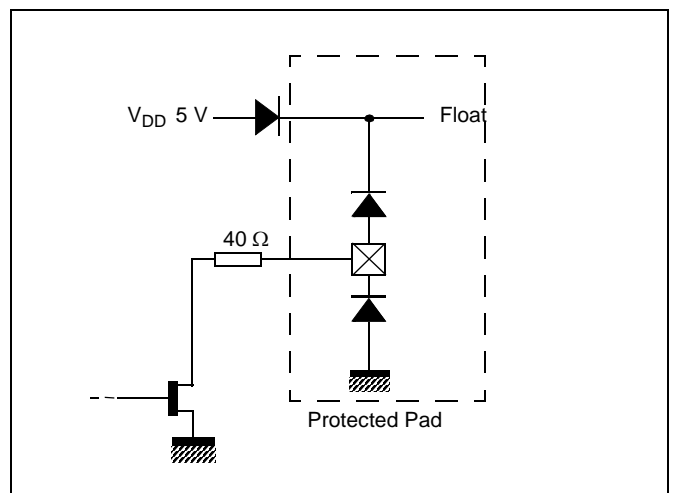
**Figure 15: Audio Outputs**  
(Pins 27, 28, 29, 30, 32 and 33)



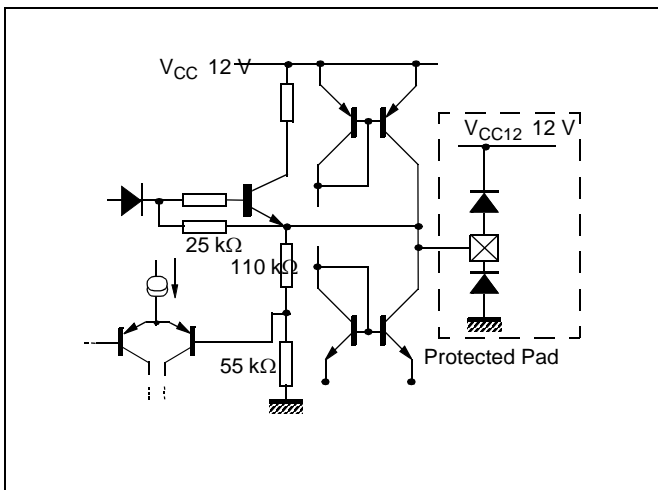
**Figure 13: Audio Inputs**  
(Pins 11, 13, 19, 20, 22 and 23)



**Figure 16: Interrupt Output**  
(Pin 58)



**Figure 14: Slow Blanking I/O** (Pins 59 and 61)



**Figure 17: I<sup>2</sup>C Bus (SDA) (Pin 56)**

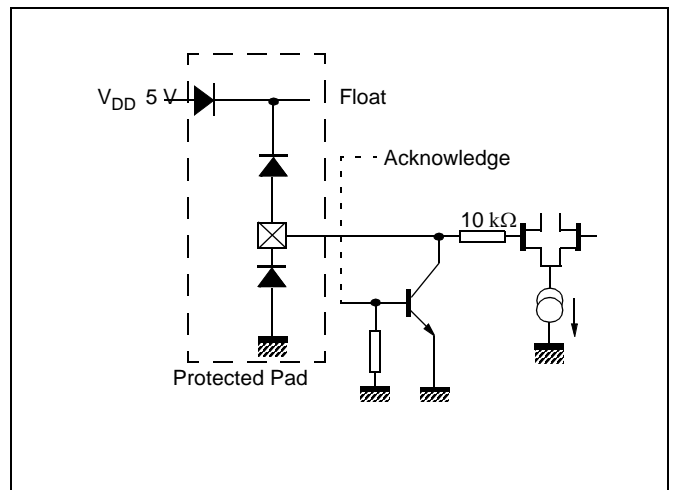


Figure 18: I<sup>2</sup>C Bus (SCL) (Pin 55)

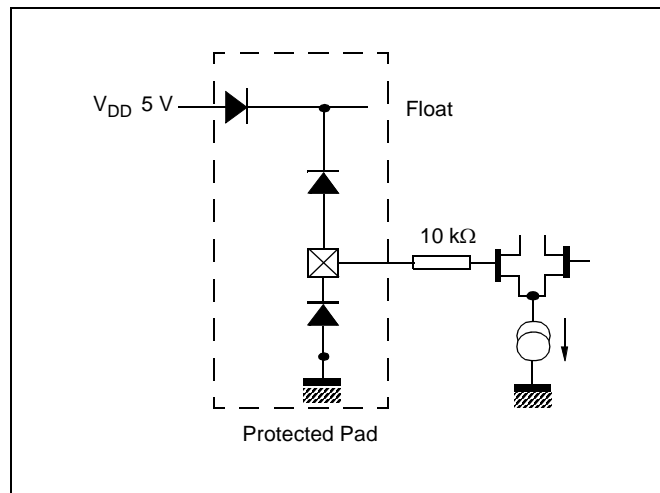
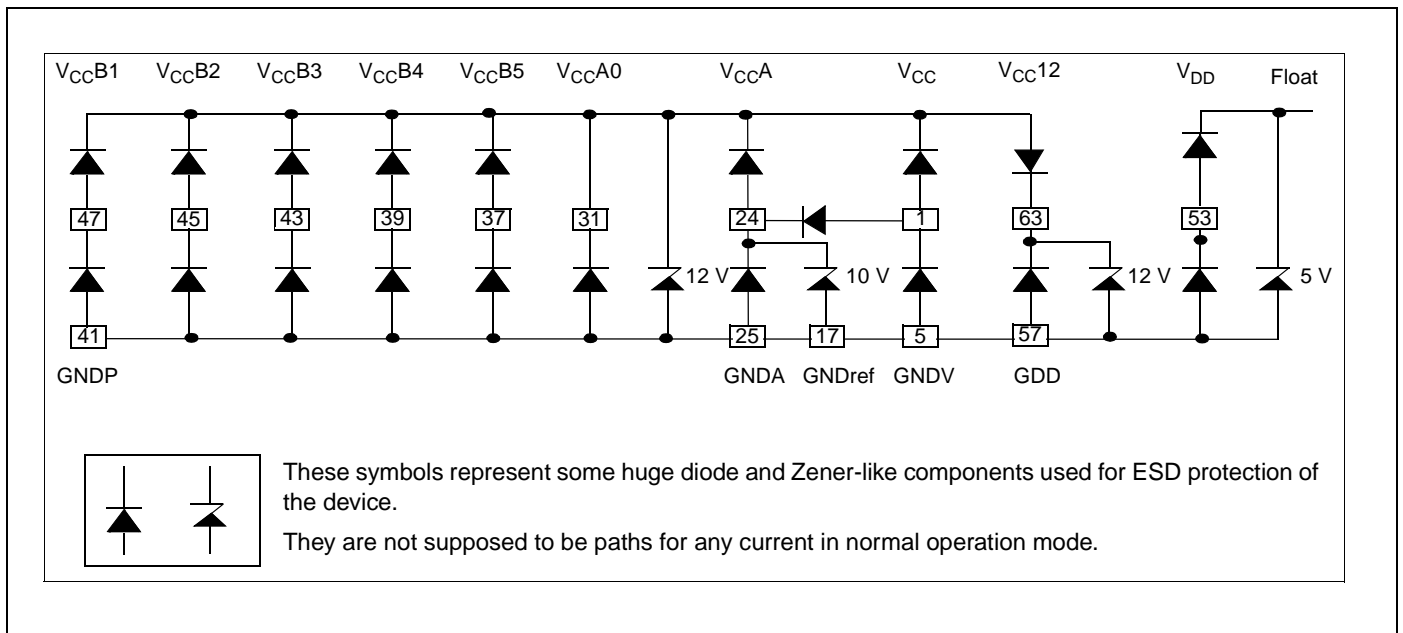


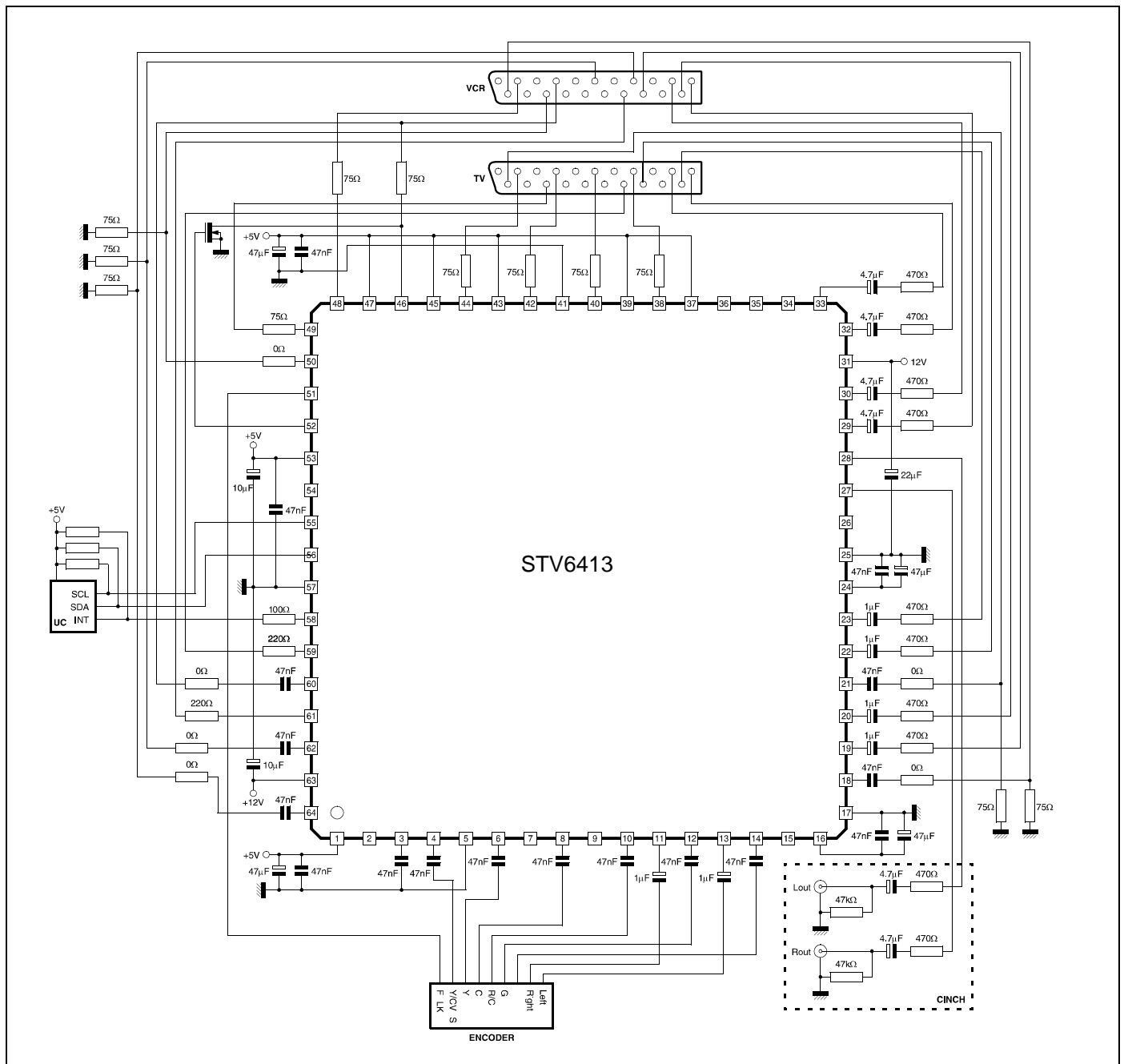
Figure 19: Power Supply Connection





# 5 Application Diagram

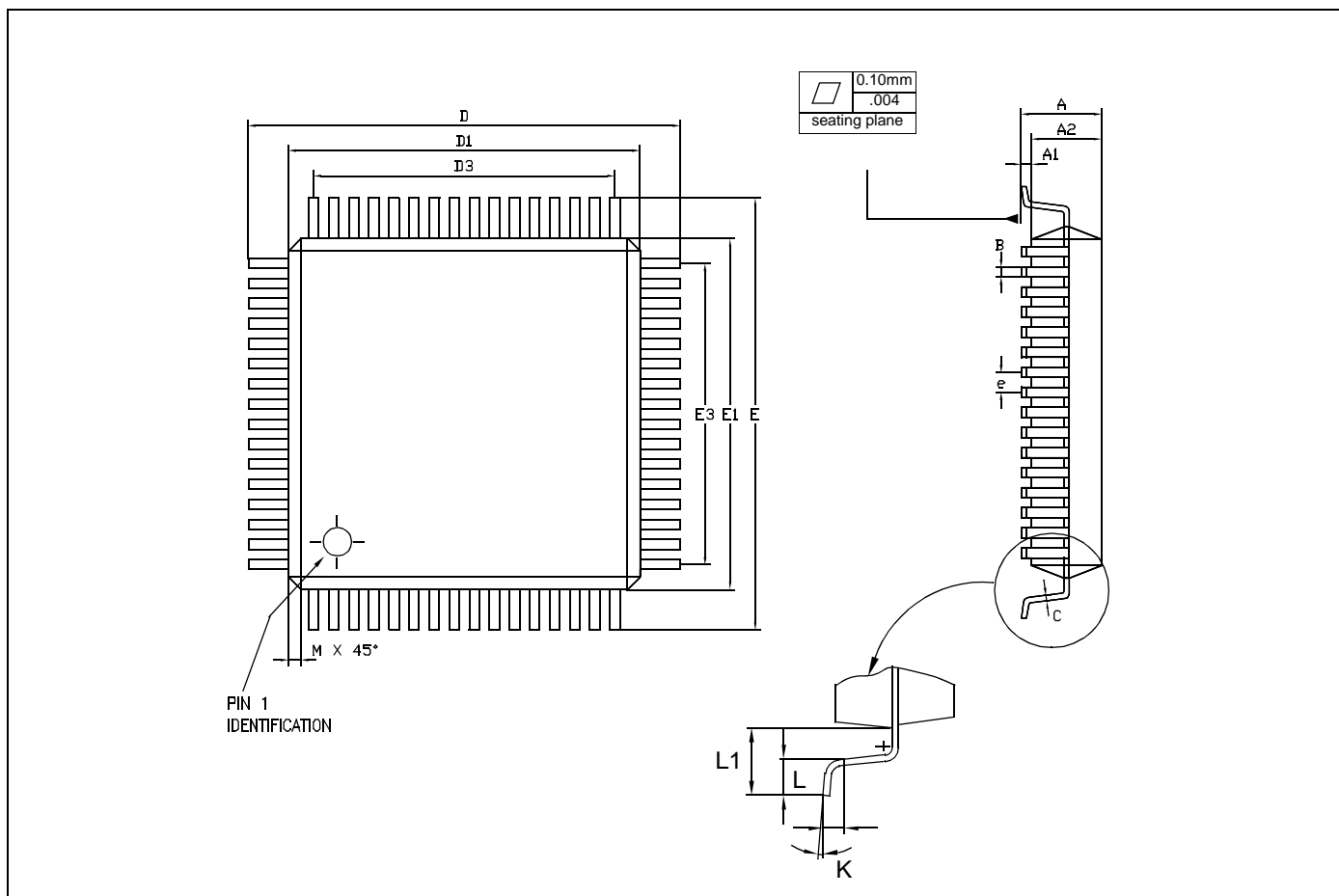
Figure 20: STV6413 Application Diagram



Note: For more details refer to STV6412A Application Note.

## 6 Package Mechanical Data

Figure 21: 64 Pin, Thin Full Plastic Quad Flat Pack (TQFP)



Dim.	mm			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
C	0.09		0.20	0.004		0.008
D		12.00			0.472	
D1		10.00			0.394	
E		12.00			0.472	
E1		10.00			0.394	
e		0.50			0.020	
K	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
	Number of Pins					
N	64		ND	16	NE	16

## 7 Revision History

Revision	Main Changes	Date
1.0	First Issue	Sept. 2001
1.1	Pin List updated.	Dec. 2001
1.2	STV6413 Product Preview updated to Datasheet. Order codes updated. Note added to <a href="#">Section 2.2: Thermal Data on page 8</a> . Test Conditions updated for Total Harmonic Distortion values in <a href="#">Section : Audio Section on page 9</a> .	March 2002
1.3	Modification of <a href="#">Note 1 on page 16</a> .	July 2002

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