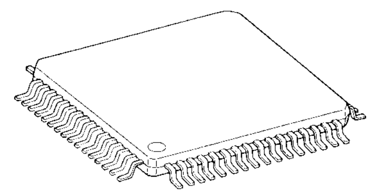
TOSHIBA Bi-CMOS Integrated Circuit Silicon Monolithic

TB62718AFG

Controller and Driver for Full-color LED Modules and Panels

The TB62718AFG is an LED driver which is suitable for driving full-color LED modules. This device has built-in 8 bit PWM grayscale and an output current adjustment functions. It can turn on to 16 LEDs. This device has a heat sink fitting side on the surface of the package. Then, a heat sink will dissipate heat generated in the device. In addition, this device incorporates built-in TSD (thermal Shutdown) and output-open detection functions to protect the device.



HQFP64-P-1010-0.50

Weight: 0.26 g (typ.)

Features

- Output current capability and number of outputs: 90 mA × 16 outputs
- Constant current range: 5 mA~75 mA
- Application output voltage: 0.7 V (output current 5 mA~90 mA)
- Adjustment function
  1. Standard current adjustment (8-bit serial data input)
     This function supports standard current adjustment using an external resistance connected to the REXT pin.
     2 high-order bits … Output current can be adjusted to any one of 4 levels in the range 25%~100%.
     6 low-order bits … Output current can be adjusted to any one of 64 levels in the range 40%~100%.
  2. Each dot adjustment (128-bit serial data input)
     This function allows adjustment of the current value for each output (dot).
     … Output current can be adjusted to any one of 64 levels in the range 20%~100%.
  3. All dot adjustment 1 (8-bit parallel data input)
     This function allows adjustment of brightness for each LED module.
     5 low-order bits … Output current can be adjusted to any one of 32 levels in the range 50%~100%.
  4. All dot adjustment 2 (8-bit parallel data input)
     This function allows changes to the frequency of the PWM clock and allows major brightness adjustment for the display.
     3 high-order bits … PWM clock frequency can be adjusted to any one of 8 levels in the range 1/1~1/8.
  5. 256-grayscale PWM function (8-bit parallel input)
     This function controls the pulse width for each output, yielding 256 grayscales.
     Maximum PWM clock frequency 10 MHz (for all temperature range), Minimum pulse width 2 ms
  - Accuracy of bits in constant-current output levels prior to adjustment
    ±6.0% max (for output current of 40 mA~80 mA)
    ±7.0% max (for output current of 20 mA~40 mA)
    ±12.0% max (for output current of 5 mA~20 mA)
- Protection functions
  1. Thermal shutdown function (TSD)
     This function monitors the rise in junction temperature.
     Connect a pull-up resistor to the ALARM1 pin in order to monitor the temperature.
  2. Output Pin Open Detection function
     This function detect when an output pin is open.
     Connect a pull-up resistor to the ALARM2 pin in order to monitor this.

- For anode-common LEDs
- Input signal voltage level: CMOS level (Schmitt trigger input)
- Power supply voltage range V_{DD} = 4.5 V~5.5 V
- Maximum output pin voltage: 26 V
- Serial and parallel data transfer rate: 20 MHz (max, cascade connection)
- Operating temperature range T_{opr} = −40°C~85°C
- Package: HQFP64-P-1010-0.50. A Heat sink can be fitted.

Warnings

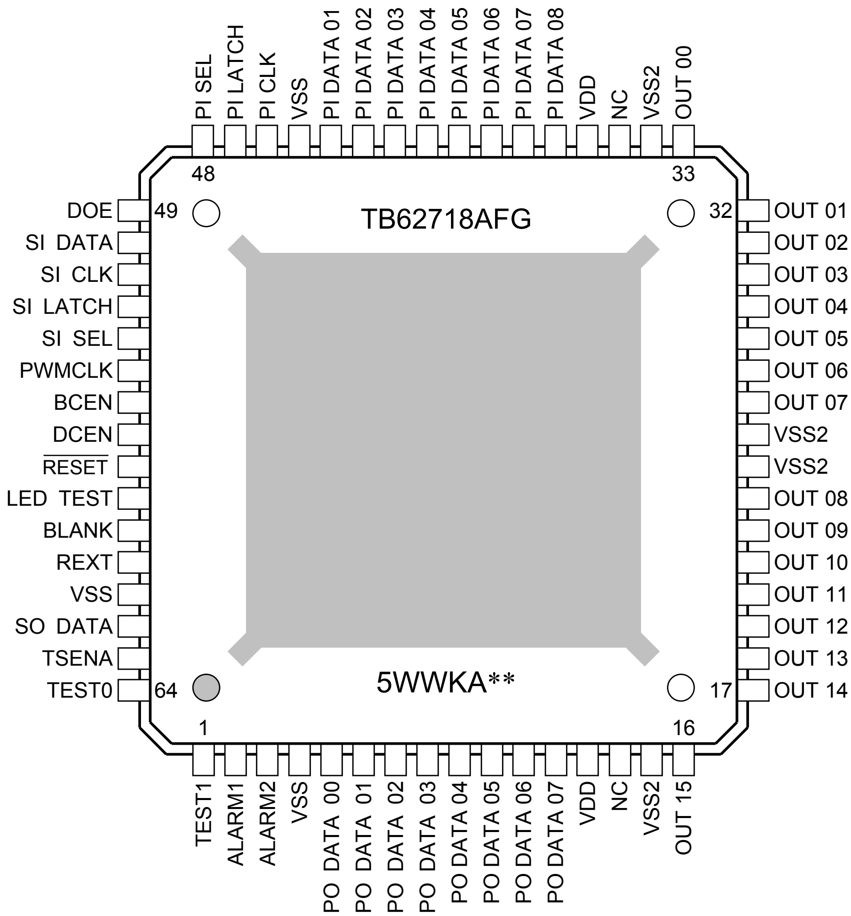
Short-circuiting an output pin to GND or to the power supply pin may destroy the device. Take care when wiring the output pins, the power supply pin and the GND pins (V_{SS}, V_{SS2}).

Do not apply either positive or negative voltages to the heat sink on the surface of the IC.

In addition, do not solder anything to the heat sink.

Pin Assignment (top view) and Markings

Package type: HQFP64-P-1010-0.50



Note: Indicates device name on the upper surface of the package.
Indicates weekly code on the lower surface of the package.

Details of weekly code on lower surface:

From left,

1st character = rightmost digit of year 0 for 2000, 1 for 2001

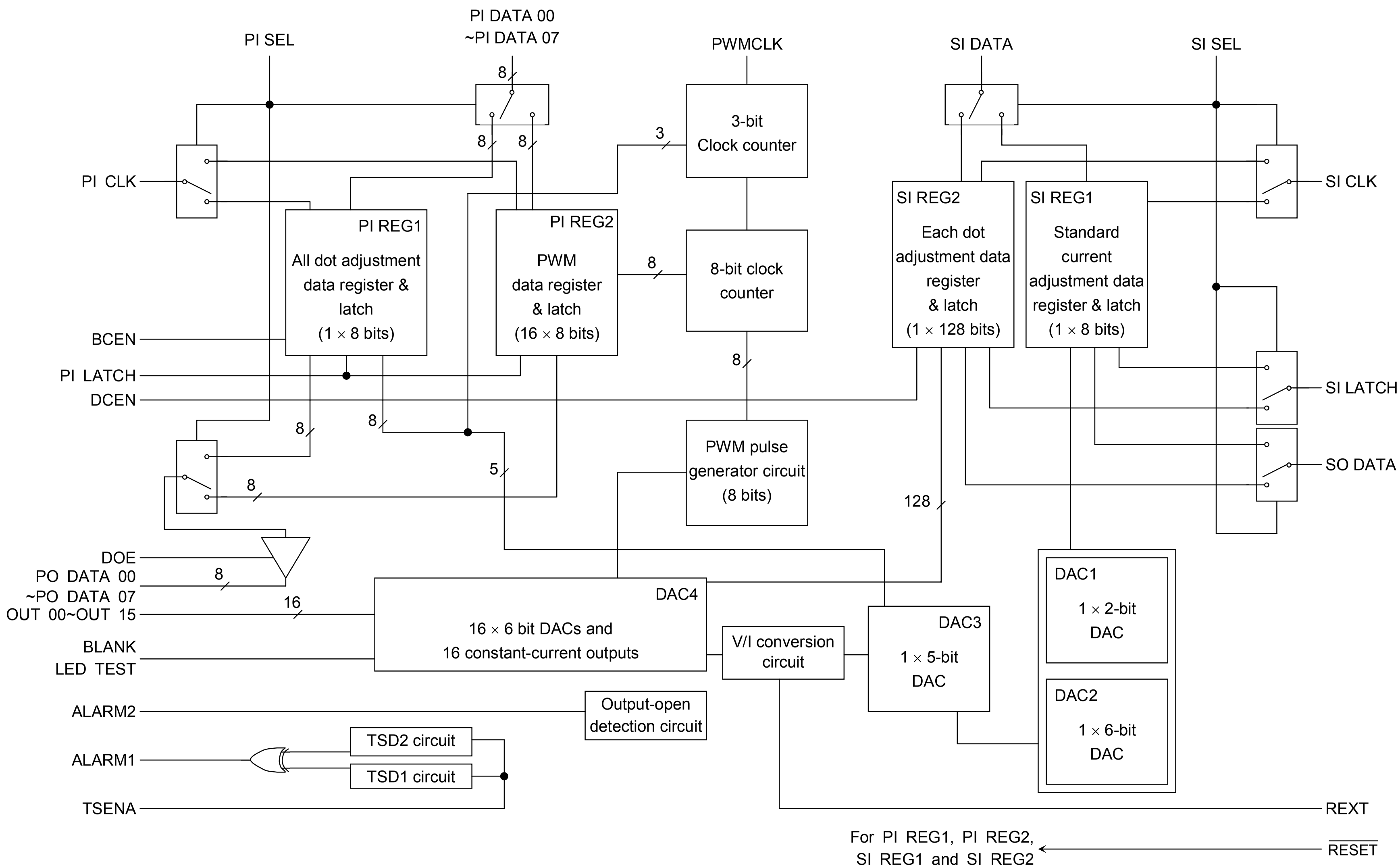
2nd and 3rd characters = week of manufacture during year: maximum value = 52.

4th characters = manufacturing factory (‘K’ means the Kita Kyushu factory.)

5th to 7th characters = lot number within week

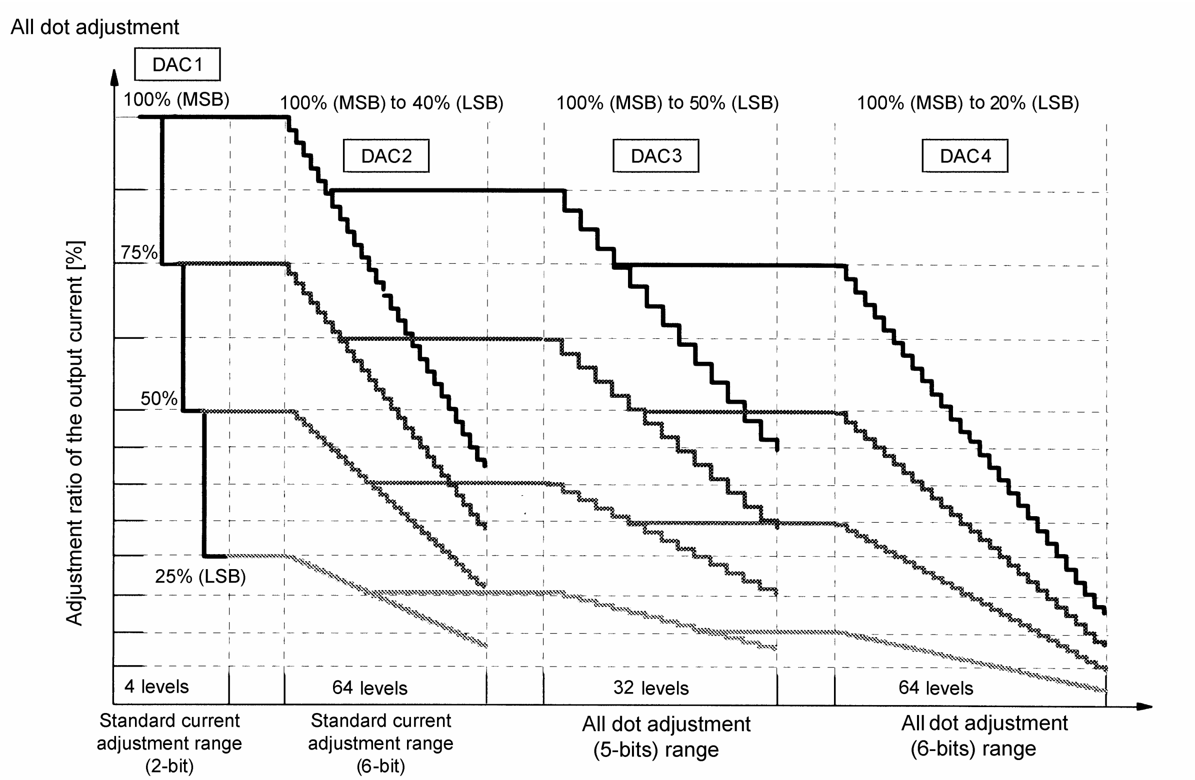
1st lot is A11, 2nd lot is A1 and 3rd lot is A.
4th lot is B11, 5th lot is B1 and 6th lot is B.
64th lot is Z11, 65th lot is Z1 and 66th lot is Z.
The four characters of ‘I’, ‘M’, ‘O’ and ‘W’ are not used.

Block Diagram (entire device)



Constant Current Adjustment Range (graph)

This graph shows how current may be adjusted to a fraction of its full-scale value.



Note 1: In each case, the value input to each DAC is the value output from the previous DAC.

Reference: Current adjustment functions

DAC1 to DAC3 are the current adjustment functions for all outputs.

The adjustment width of DAC1 is large and approximate (1 LSB ≃ 25%).

The adjustment width of DAC2 is the smallest and has a large error (1 LSB ≃ 0.9%).

The adjustment width of DAC3 is small. DAC3 is a high-performance DAC with a small error (1 LSB ≃ 1.61%).

Therefore,
It is recommended that DAC1 and DAC2 be used for adjusting the REXT resistance.
It is recommended that DAC3 be used for adjusting brightness between module.
(after it was set and it had DAC4 adjusted to the dot.)
The beginning is set in about 75% of the middle value, after that, it is effective to use ±25% of set width.

DAC4 is the current adjustment function for all outputs.
The adjustment width of DAC4 is small. But it is a high-performance DAC with a small error (1 LSB ≃ 1.27%).
And also, DAC4 has a very wide setting range.

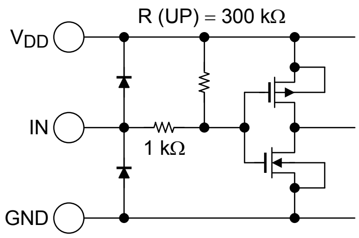
Therefore, DAC4 can be used to adjust the brightness of LEDs without a rank classification.
This method allows brightness to be adjusted with a degree of accuracy of 1.27% of full scale.

Note 2: Assuming precise linear correlation between output current and LED brightness

Equivalent Input and Output Circuits (resistance values are typical values.)

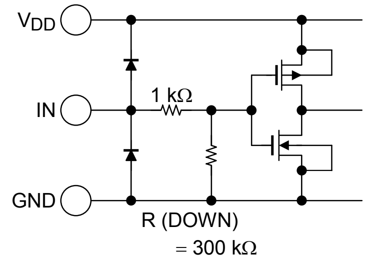
Input pins with pull-up resistor

TSENA, BLANK, BC/DCEN



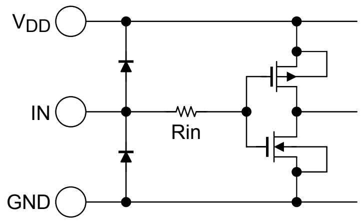
Input pins with pull-down resistor.

SI/PI LATCH, PI DATA 00~PI DATA 07, LED TEST



Input terminals

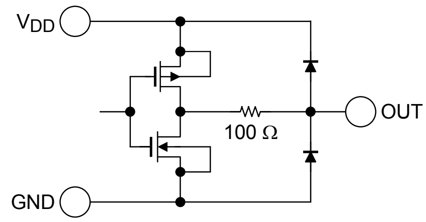
(A) SI DATA, SI CLK, PI CLK, PWMCLK
(B) $\overline{\text{RESET}}$, $\overline{\text{DOE}}$, PI SEL, SI SEL



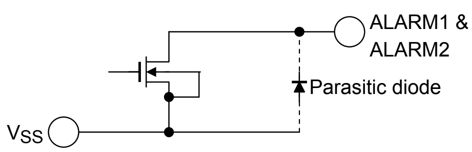
(A) Rin = 250 Ω
(B) Rin = 1 kΩ

Output terminals

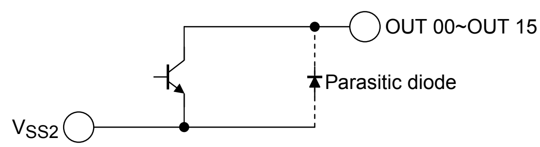
PO DATA 00~PO DATA 07, SO DATA



Protection circuit monitor terminals



Constant-current output terminals



Explanation of Pin Functions Table

No.	Name	I/O	Function Explanation	
4, 45	VSS	P	—	Logic ground pins. Be sure to use all.
35, 14	NC	—	—	Unused
63	TSENA	I	Pull-up	This pin is used to reset the IC's built-in temperature monitoring circuit (TSD). Rising edge of input signal re-enables outputs which had been forced to OFF. The latched data as the setting is not reset. Either in case of H- or L-level of this terminals can be operated TSD circuit.
15, 24, 25, 34	VSS2	P	—	Ground pin for output. Be sure to use all.
13, 36	VDD	P	—	Logic power supply input pins. Be sure to use all.
16~23, 26~33	OUT 00~ OUT 15	O	—	LED drive output pins. Connect to cathode of LED.
50	SI DATA	I	—	Serial data input pin. Used for input of standard current adjustment data and dot adjustment data
51	SI CLK	I	—	Serial data transfer clock input pin. Data is transferred positive edge.
52	SI LATCH	I	Pull-down	Serial data latch signal input pin. Data is held on positive edge.
53	SI SEL	I	—	Serial data selection pin. Either standard current adjustment data or dot adjustment data may be selected.
62	SO DATA	O	—	Serial data output pin. The output data type is selected using SI SEL.
37~44	PI DATA 00~ PI DATA 07	I	Pull-down	Input pins for parallel data. Inputs for all output adjustment data and PWM data
46	PI CLK	I	—	Input pin for parallel data transfer clock. Data is transferred on positive edge.
47	PI LATCH	I	Pull-down	Input pin for parallel data latch signal. Data is held on rising positive edge.
48	PI SEL	I	—	Parallel data selection pin. Either all output adjustment data or PWM data may be selected.
5~12	PO DATA 00~ PO DATA 07	O	—	Output pin for parallel data. The output data type is selected using PISEL.
49	DOE	I	—	Control pin for parallel data output PODATA. PIDATA is out on input of an H-level signal. PIDATA is set to High-impedance by input of an L-level signal.
59	BLANK	I	Pull-up	PWM circuit control signal input pin. Output is turn OFF by input of an H-level signal. PWM output is initiated by input of an L-level signal accordingly to the input data.
54	PWMCLK	I	—	Standard clock input pin for PWM circuit. One clock cycle is equivalent to the minimum pulse width of the PWM output.
55	BCEN	I	Pull-up	Selection signal input pin for all output adjustment functions. All output adjustment is fixed to 100% when this signal is Low. All bit adjustments become effective when it is High. It isn't influent anything to all output adjustment by PWMCLK.
56	DCEN	I	Pull-up	Selection signal input pin for dot adjustment function. Dot adjustment value is fixed to 100% when this signal is Low. Dot adjustment becomes effective when it is High.
57	$\overline{\text{RESET}}$	I	—	Reset signal input pin. Setting and registered data are reset when it is Low. A reset also releases TSD.
58	LED TEST	I	Pull-down	Connection confirmation signal input pin for an LED. When this signal is High, all outputs are ON. This signal should normally be kept Low.
60	REXT	P	—	Connection pin of resistor for setting for the current.
2	ALARM1	O	—	Open-drain monitor pin for TSD circuit. When the TSD circuit detects an abnormal temperature, this signal is turned ON. IO monitor the TSD circuit connect this pin to a pull-up resistor. ALARM1 is independent of the $\overline{\text{RESET}}$ signal.
3	ALARM2	O	—	Open-drain monitor pin for output-open detection circuit. When an open output is detected, this signal is turned ON.
1, 64	TEST 0, TEST 1	I	—	Pins for the device testing. Connect all these pins to ground.

Pin attributes P: power supply/ground/other, I: input pin, O: output pin

Note 3: It is recommended that pins with pull-up or pull-down resistors not be left open.
Ambient noise may cause malfunction of the device.

Absolute Maximum Ratings (T_{opr} = 25°C unless otherwise specified)

Characteristics		Symbol	Rating	Unit
Supply voltage		V_{DD}	−0.3~7	V
Constant-current output voltage		V_O	−0.3~26	V
Output current		I_{OUT}	90	mA/bit
Logic output voltage		V_{OUT}	−0.3~ V_{DD} + 0.3	V
Logic input voltage		V_{IN}	−0.3~V_{DD} + 0.3	V
Total V_{SS2} current (Note 5)		IV_{SS2}	1.44	A
Power dissipation	When device mounted on PCB (Note 6)	P_d (Note 4)	1.19	W
	When device mounted on PCB of any size		5.0	
Saturation heat resistance of package	When device mounted on PCB (Note 6)	$\theta_{(j-a)}$	102	°C/W
	When device mounted on PCB of any size	$\theta_{(j-c)}$	25	
Operating temperature		T_{opr}	−40~85	°C
Storage temperature		T_{stg}	−55~150	°C

Note 4: If the operating temperature exceeds 25°C, derate the power dissipation rating by 0.95 mW/°C.

Note 5: All four VSS2 pins must be connected. If not, device characteristics cannot be guaranteed.

Note 6: When device mounted on PCB with dimensions 100 mm × 100 mm × 1.6 mm

Recommended Operating Conditions
(V_{DD} = 4.5 V~5.5 V, T_{opr} = −40°C~85°C unless otherwise specified)

Characteristics	Symbol	Conditions & Pins	Min	Typ.	Max	Unit
Supply voltage	V_{DD}	—	4.5	5.0	5.5	V
High-level input voltage	V_{IH}	PI DATA, PI CLK, PI SEL, PI LATCH, SI DATA, SI CLK, SI SEL, SI LATCH, PWM CLK	0.7 V_{DD}	—	V_{DD}	V
Low-level input voltage	V_{IL}	BLANK, LED TEST, TSENA, DOE, DCEN, BCEN	V_{SS}	—	0.3 V_{DD}	V
High-level output current	I_{OH}	PO DATA 00~PO DATA 07, SO DATA	—	—	−1	mA
Low-level output current	I_{OL}	V_{DD} = 4.5 V, ALARM1, ALARM2	—	—	1	mA
Constant-current output	I_{OUT}	OUT 00~OUT 15	5	—	80	mA/bit
Output voltage	V_{OUT}	OUT 00~OUT 15 OFF	—	—	26	V
	V_{OH}	ALARM1, ALARM2 OFF	—	—	5	V
Operating temperature	T_{opr}	—	−40	—	85	°C

Recommended Operating Conditions (continue)
(V_{DD} = 4.5 V~5.5 V, T_{opr} = –40°C~85°C unless otherwise specified)

Characteristics	Symbol	Condition & Terminals	Min	Typ.	Max	Unit
Clock frequency	f_{PWM}	Ratio of High-level: Low level = 50%, PWM CLK	—	—	10	MHz
	f_{PI1}	PI CLK,	—	—	15	
	f_{PI2}	PI CLK, connected in cascade	—	—	10	
	f_{SI1}	SI CLK	—	—	15	
	f_{SI2}	SI CLK, connected in cascade	—	—	10	
Minimum pulse width	t_{wH}/t_{wL}	PWM CLK	30	—	—	ns
		PI CLK, SI CLK	30	—	—	
	t_{wltH}/t_{wltL}	PI LATCH, SI LATCH	50	—	—	
	t_{wrstH}/t_{wrstL}	$\overline{\text{RESET}}$	50	—	—	
	t_{wblkH}/t_{wblkL}	BLANK	400	—	—	
	t_{wledH}/t_{wledL}	LED TEST	400	—	—	
Set-up time	t_{setup}	PI DATA → PI CLK	10	—	—	ns
		PI LATCH → PI CLK	10	—	—	
		SI DATA → SI CLK	10	—	—	
		SI LATCH → SI CLK	10	—	—	
		SI LATCH → SI CEL	50	—	—	
Hold time	t_{hold}	PI DATA → PI CLK	5	—	—	ns
		PI LATCH → PI CLK	5	—	—	
		SI DATA → SI CLK	5	—	—	
		SI LATCH → SI CLK	5	—	—	
		SI LATCH → SI CEL	50	—	—	

Electrical Characteristics 1
(V_{DD} = 4.5 V~5.5 V, T_{opr} = –40°C~85°C, typ: V_{DD} = 5.0 V, T_{opr} = 25°C)

Parameter	Symbol	Test conditions & Terminals	Min	Typ.	Max	Unit
High-level output voltage	V_{OH}	I_{OH} = –1.0 mA, PO DATA 00~PO DATA 07, SO DATA	V_{DD} –0.4	—	—	V
Low-level output voltage	V_{OL}	I_{OL} = 1.0 mA, PO DATA 00~PO DATA 07, SO DATA	—	—	0.4	V
		I_{OL} = 1.0 mA, ALARM1, ALARM2	—	—	0.3	
Tri-state output leakage current	I_{OZ}	V_{OUT} = V_{DD} or V_{SS}, PO DATA 00~PO DATA 07	—	±0.5	±5	μA
Input current	I_I	All pins without pull-up/pull-down resistors	—	—	±1	μA
Supply current	I_{DD1}	PI DATA = 1/2 PI CLK SI DATA = 1/2 SI CLK PI CLK = SI CLK = 20 MHz PWMCLK = L, BLANK = H Settings: *1	—	20	30	mA
	I_{DD2}	PI DATA = SI DATA = L PI CLK = SI CLK = L PWMCLK = 20 MHz Settings: *5a	—	75	105	
	I_{DD3}	PI DATA = 1/2 PI CLK SI DATA = 1/2 SI CLK PI CLK = SI CLK = PWMCLK = 20 MHz Settings: *5a	—	80	115	
	I_{DD4}	PI DATA = SI DATA = L PI CLK = SI CLK = L PWMCLK = 20 MHz Settings: *6a	—	90	140	
	I_{DD5}	PI DATA = 1/2 PI CLK SI DATA = 1/2 SI CLK PI CLK = SI CLK = PWMCLK = 20 MHz Settings: *6a	—	95	150	

Electrical Characteristic Settings

(OUT 00~OUT 15 all on, V_{OUT} = 0.7 V and REXT = 2.7 kΩ unless otherwise specified)

No.	DAC Settings	Surface Brightness Adjustment (DAC3)	Constant Output Current (typ.)
*1	Outputs all OFF, V_{OUT} = 26 V, DAC1, 2, 4 = MSB, BLANK = H	DAC3 = 31	I_{OUT} = 0 mA
*2	DAC1 = 0, DAC2 = 0, DAC4 = 63, BLANK = L		I_{OUT} = 7.10 mA
*3a	DAC1 = 0, DAC2 = 17, DAC4 = 63, BLANK = L		I_{OUT} = 10.0 mA
*4a	DAC1 = 1, DAC2 = 17, DAC4 = 63, BLANK = L		I_{OUT} = 19.9 mA
*5a	DAC1 = 2, DAC2 = 37, DAC4 = 63, BLANK = L		I_{OUT} = 40.1 mA
*6a	DAC1 = 3, DAC2 = 51, DAC4 = 63, BLANK = L		I_{OUT} = 60.2 mA
*7	DAC1 = 3, DAC2 = 63, DAC4 = 63, BLANK = L		I_{OUT} = 71.0 mA
*3b	DAC1 = 0, DAC2 = 17, DAC4 = 63, BLANK = L	DAC3 = 00	I_{OUT} = 5.0 mA
*4b	DAC1 = 1, DAC2 = 17, DAC4 = 63, BLANK = L		I_{OUT} = 10.0 mA
*5b	DAC1 = 2, DAC2 = 37, DAC4 = 63, BLANK = L		I_{OUT} = 20.0 mA
*6b	DAC1 = 3, DAC2 = 51, DAC4 = 63, BLANK = L		I_{OUT} = 30.1 mA

Electrical Characteristics 2
(V_{DD} = 4.5 V~5.5 V, T_{opr} = –40°C~85°C, typ: V_{DD} = 5.0 V, T_{opr} = 25°C)

Parameter	Symbol	Test Conditions	Min	Typ.	Max	Unit
Constant-current output	I_{OUT1}	Settings *7	60.4	71.0	81.6	V
	I_{OUT2}	Settings *6a	51.2	60.2	69.2	
	I_{OUT3}	Settings *5a	34.1	40.1	46.1	
	I_{OUT4}	Settings *4a	16.5	19.9	23.2	
	I_{OUT5}	Settings *3a	7.8	10.0	12.2	
	I_{OUT6}	Settings *2	4.54	7.1	9.65	
Constant-current output Depends on temperature	$\%T_{OPR1}$	Settings *6a, V_{OUT} = 1.0 V, T_{opr} is varied in the range –40°C~85°C.	—	±50	±80	μA/°C
	$\%T_{OPR2}$	Settings *4a, V_{OUT} = 1.0 V, T_{opr} is varied in the range –40°C~85°C.	—	±25	±50	
Leakage current for constant-current output	I_{OLK}	Settings *1, V_{OUT} = 26 V	—	0.05	0.1	μA
Constant current accuracy between bits	ΔI_{OUT1}	Settings *6a, V_{OUT} = 0.7 V	—	±2.5	±6	%
	ΔI_{OUT2}	Settings *5a, V_{OUT} = 0.7 V	—	±3.5	±6	
	ΔI_{OUT3}	Settings *4a, V_{OUT} = 0.7 V	—	±5.5	±7	
	ΔI_{OUT4}	Settings *3a, V_{OUT} = 0.7 V	—	±7	±12	
Dot adjustment deviation between bits (when DAC3 data were changed from MSB to LSB.)	$\%I_{OUT1}$	Settings is changed from *6a to *6b.	—	±1	±3	%
	$\%I_{OUT2}$	Settings is changed from *5a to *5b.	—	±1.5	±3	
	$\%I_{OUT3}$	Settings is changed from *4a to *4b.	—	±3.5	±5	
	$\%I_{OUT4}$	Settings is changed from *3a to *3b.	—	±6	±12	
Constant-current output depends on output voltage	$\%V_{OUT}$	Settings *6a, V_{OUT} is varied in the range 0.7 V~3 V.	—	±5	±8	%
		Settings *4a, V_{OUT} is varied in the range 0.7 V~3 V.	—	±3	±6	
Constant-current output depends on supply voltage	$\%V_{DD}$	Settings *6a, V_{DD} is varied in the range 4.5 V~5.5 V.	—	±1	±2	%
TSD detection temperature	T_{sd1}	—	120	140	160	°C
	T_{sd2}	—	140	160	180	
Output-open detection voltage	V_{ARL}	ALARM2	—	0.04 V_{DD}	—	V
Pull-up/down resistor	R_{up}/R_{dw}	—	150	300	600	kΩ

Electrical Characteristic Settings

(OUT 00~OUT 15 all on, V_{OUT} = 0.7 V and REXT = 2.7 kΩ unless otherwise specified)

No.	DAC Settings	All Dot Adjustment (DAC3)	Constant Output Current (typ.)
*1	OUT00~15 OFF, V_{OUT} = 26 V, DAC1~4 = MSB, BLANK = H	DAC3 = 31	I_{OUT} = 0 mA
*2	DAC1 = 0, DAC2 = 0, DAC4 = 63, BLANK = L		I_{OUT} = 7.10 mA
*3a	DAC1 = 0, DAC2 = 17, DAC4 = 63, BLANK = L		I_{OUT} = 10.0 mA
*4a	DAC1 = 1, DAC2 = 17, DAC4 = 63, BLANK = L		I_{OUT} = 19.9 mA
*5a	DAC1 = 2, DAC2 = 37, DAC4 = 63, BLANK = L		I_{OUT} = 40.1 mA
*6a	DAC1 = 3, DAC2 = 51, DAC4 = 63, BLANK = L		I_{OUT} = 60.2 mA
*7	DAC1 = 3, DAC2 = 63, DAC4 = 63, BLANK = L		I_{OUT} = 71.0 mA
*3b	DAC1 = 0, DAC2 = 17, DAC4 = 63, BLANK = L	DAC3 = 00	I_{OUT} = 5.0 mA
*4b	DAC1 = 1, DAC2 = 17, DAC4 = 63, BLANK = L		I_{OUT} = 10.0 mA
*5b	DAC1 = 2, DAC2 = 37, DAC4 = 63, BLANK = L		I_{OUT} = 20.0 mA
*6b	DAC1 = 3, DAC2 = 51, DAC4 = 63, BLANK = L		I_{OUT} = 30.1 mA

Switching Characteristics
(V_{DD} = 4.5 V~5.5 V, T_{opr} = –40°C~85°C, C_L = 50 pF unless otherwise specified, typ: V_{DD} = 5.0 V, T_{opr} = 25°C, C_L = 50 pF)

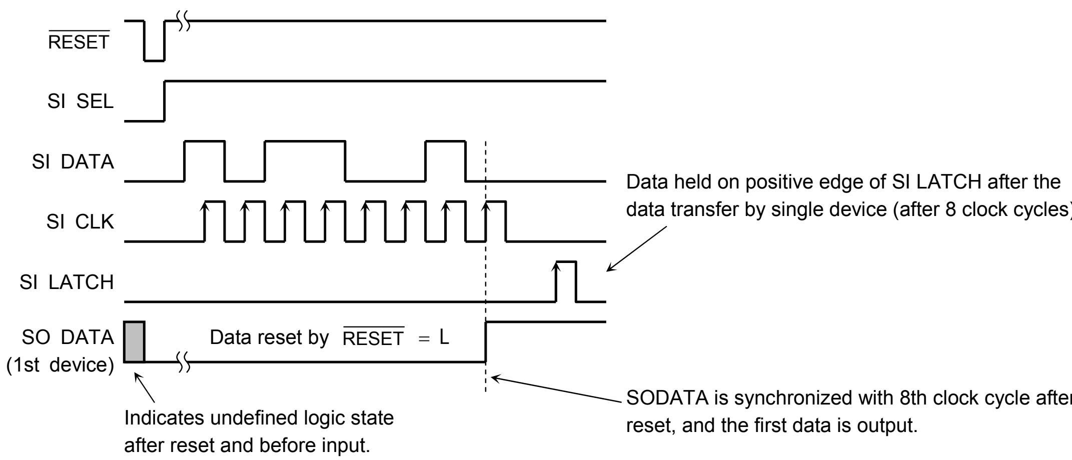
Parameter	Symbol	Test Conditions	Min	Typ.	Max	Unit
Tri-state output enable propagation delay	$t_{pZH/ZL}$	DOE → PO DATA0~ PO DATA 7	8	16	30	ns
Tri-state output disable propagation delay	$t_{pHZ/LZ}$	DOE → PO DATA0~ PO DATA 7	8	16	30	ns
Rise time	t_r	OUT00~ OUT 15	10	17	30	μs
		ALARM1, ALARM2	0.2	0.4	0.8	ns
Fall time	t_f	OUT00~ OUT 15	20	40	70	ns
		ALARM1, ALARM2	2	4	8	
Propagation delay	t_{pHL}	BLANK → OUT00~ OUT 15	30	60	120	ns
	t_{pLH}	PWM CLK → OUT00~ OUT 15	70	120	200	
	t_{pHL}	PWM CLK → OUT00~ OUT 15	40	70	140	
	t_{pLH}	LED TEST → OUT00~ OUT 15	60	110	190	
	t_{pHL}		30	60	130	
	t_{pHL}	$\overline{\text{RESET}}$ → OUT00~ OUT 15	30	60	130	
	t_{pd}	PI CLK → PO DATA0~ PO DATA 7	20	30	70	
		PI SEL → PO DATA0~ PO DATA 7	20	30	70	
		SI SEL → SO DATA	10	18	40	
		SI SEL → SO DATA	10	20	40	

Explanation of Operation and Truth Tables

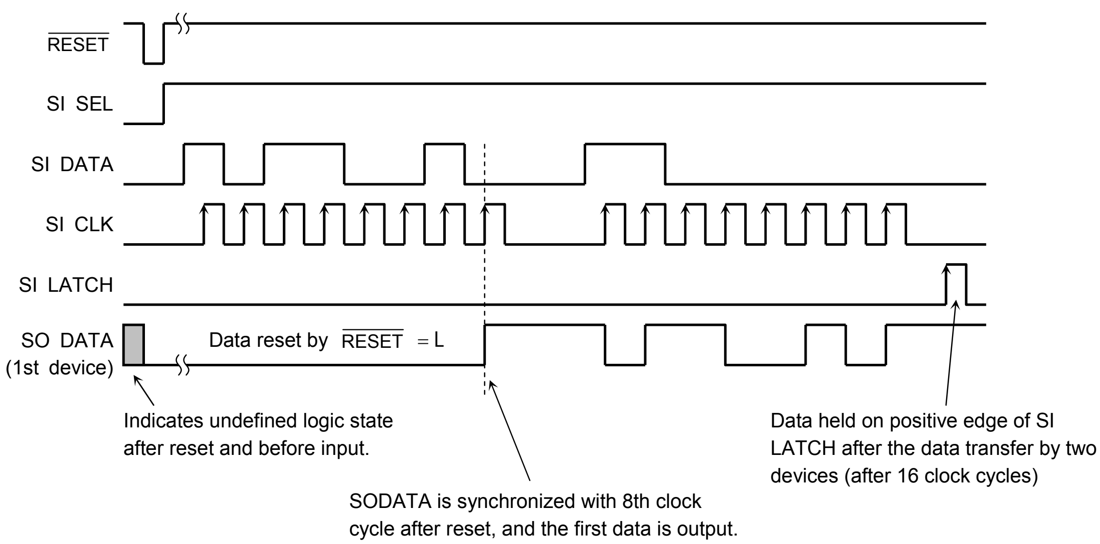
Serial data transfer: standard current adjustment using DAC1 and DAC2 (data register SI REG [7:0])

Process	SI DATA	SI CLK	SI LATCH	SI SEL	SO DATA	Operation and Function
1	H or L	↑ (×8)	L	H	H or L	Selects standard current adjustment (8 bits, 2 bits and 6 bits) for input data when SI SEL is high. Data is transferred to SI REG [1] on 8th positive edge of SI CLK input.
2	H or L	L	↑ (×1)	H	No change	Holds the data transferred to SI REG [1] on positive edge of SI LATCH. Set is reflected on standard current adjustment from the moment when it is held.

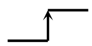
Serial data transfer timing (standard current adjustment, SI SEL = H, single device)



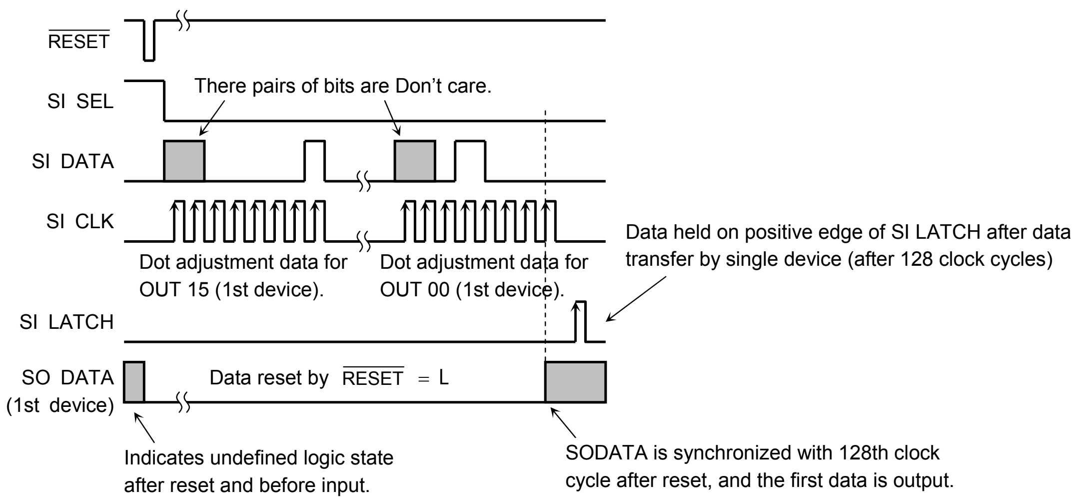
Serial data transfer timing (standard current adjustment, SI SEL = H, two devices connected in cascade)



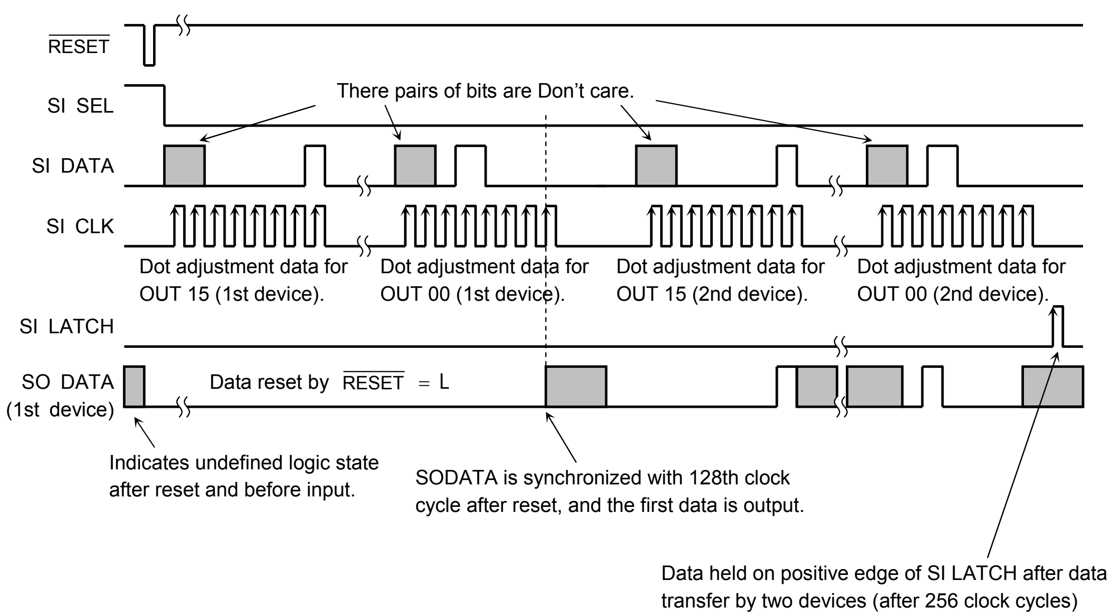
Serial data transfer: dot adjustment DAC4. (data register SI REG2 [127:0])

Process	SI DATA	SI CLK	SI LATCH	SI SEL	SO DATA	Operation and Function
1	H or L	 (×128)	L	L	H or L	Selects dot adjustment (128 bits) for input data. Data is transferred to SI REG2 on 128th positive edge of SI CLK.
2		L	 (×1)	L	No change	Holds the data transferred to SI REG2 on positive edge of SILATCH. Set is reflected on dot adjustment from the moment when it is held.

Serial data transfer timing (dot adjustment, SI SEL = L, single device)



Serial data transfer timing (dot adjustment, SI SEL = L, two devices connected in cascade)



DAC1: Standard current adjustment settings for DAC1 (SI REG1 [7:6])

RESET	SI SEL	SI REG (7:6)	SI REG (5:0)	Current Rate	Operation and Function	Notes
H	H	HH	XXXXXX	100% (1.0)	100% of base current setting as determined by R_{EXT} (Ω)	When SI SEL = H, 2 bits on MSB sides are corresponding to set of standard current adjustment DAC1. The output current can be set to one of 4 levels.
H	H	HL	XXXXXX	75% (0.75)	75% of base current setting as determined by R_{EXT} (Ω)	
H	H	LH	XXXXXX	50% (0.5)	50% of base current setting as determined by R_{EXT} (Ω)	
H	H	LL	XXXXXX	25% (0.25)	25% of base current setting as determined by R_{EXT} (Ω)	
	X	LL	LLLLLL	25% (0.25)	Initial state after input of reset signal: 25% of base current setting as determined by R_{EXT} (Ω) (as described above)	

DAC2: Standard current adjustment settings for DAC2 (SI REG1 [5:0])

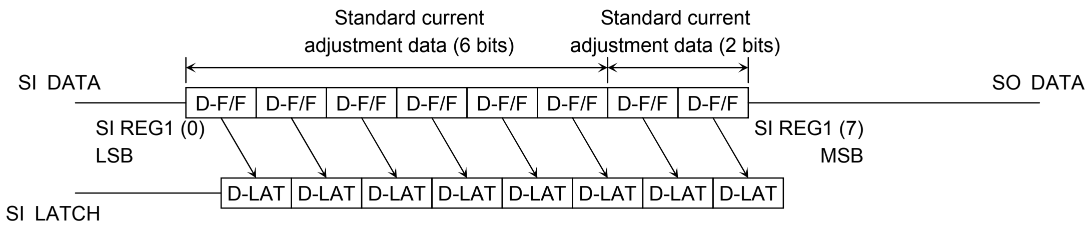
RESET	SI SEL	SI REG (7:6)	SI REG (5:0)	Current Rate	Operation and Function	Notes
H	H	XX	XXXXXX	100% (1.0)	100% of base current value as set using DAC1 base current adjustment	When SI SEL = H, 6 bits on MSB sides are corresponding to set of standard current adjustment DAC2. The output current can be set to one of 64 levels.
H	H	XX	HHHHHL ↑ ↓ LLLLLH	(0.9905) ↑ 1LSB = ±0.95% (±0.0095) ↓ (0.4095)	Any one or 64 levels in the range 40%~100% of the current can be set. (1 LSB = 0.95%) 6-bit DAC performance 1LSB variation: ±0.95% Non linearity error: ±1/2LSB Differential non linearity error: ±3/4LSB	
H	H	XX	LLLLLL	40% (0.4)	40% of base current value as set using DAC1 base current adjustment	
	X	LL	LLLLLL	40% (0.4)	Initial state after input of reset signal: 40% of base current value set as described above	

DAC4: Set details of dot adjustment DAC4 (SI REG2 [127:0])

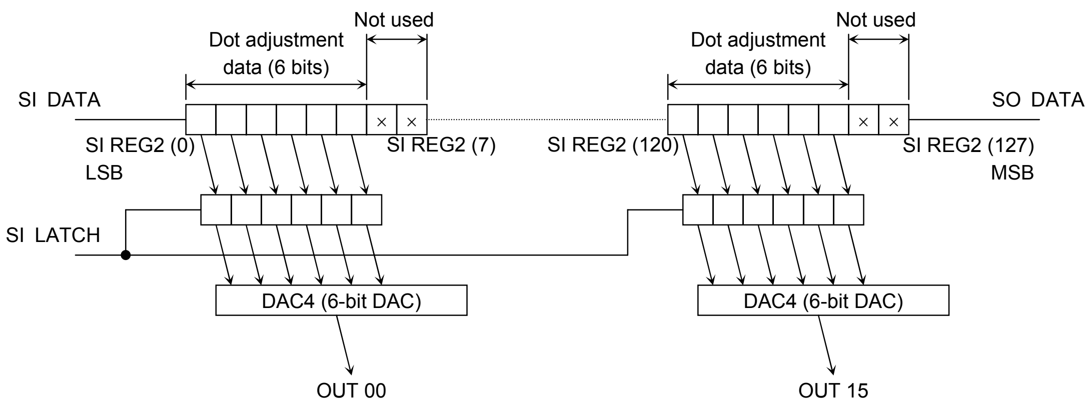
RESET	SI SEL	DCEN	About 8 bits Unit of SI REG2 [127:0]	Current Rate	Operation and Function	Notes
H	L	H	XXHHHHHH	100% (1.0)	Output current is 100% of base current value as set using DAC1 and DAC2 base current adjustment and DAC3 surface brightness adjustment	When SI SEL = L 8 bits out of 128 bits are corresponding to set of each output, and the 6 bits on MSB sides of 8 bits are data on dot adjustment. The output current can be set to one of 64 levels. SI REG2 [7:0] → adjustment data for OUT 00. SI REG2 [15:8] → adjustment data for OUT 01. SI REG2 [127:120] → adjustment data for OUT 15.
H	L	H	XXHHHHHL ↑ ↓ XXLLLLLH	(0.9874) ↑ 1LSB = ±1.269% (±0.0126) ↓ (20.0126)	Any one of 64 levels in the range 20%~100% of the current can be set. (1LSB ≃ 1.27%) 6-bit DAC performance 1LSB variation: ±1.269% Non linearity error: ±1/2LSB Differential non linearity error: ±1/2LSB	
H	L	H	XXLLLLLL	20% (0.2)	20% of base current value as set using DAC3 surface brightness adjustment	
	X	H	XXLLLLLL	20% (0.2)	Initial state after input of reset signal: 20% of base current value set as described above	
H	X	L	XXHHHHHH	100% (1.0)	Output current is 100% of base current value set as described above.	Data input is still enabled if DCEN = L. If DCEN = H, adjustment is performed at the same time.

Polarity of serial input data for standard current adjustment (SI REG1 [7:0]) and dot adjustment (SI REG2 [127:0])

Serial data transfer timing
(SI SEL = H, input of standard current adjustment data for DAC1 and DAC2)



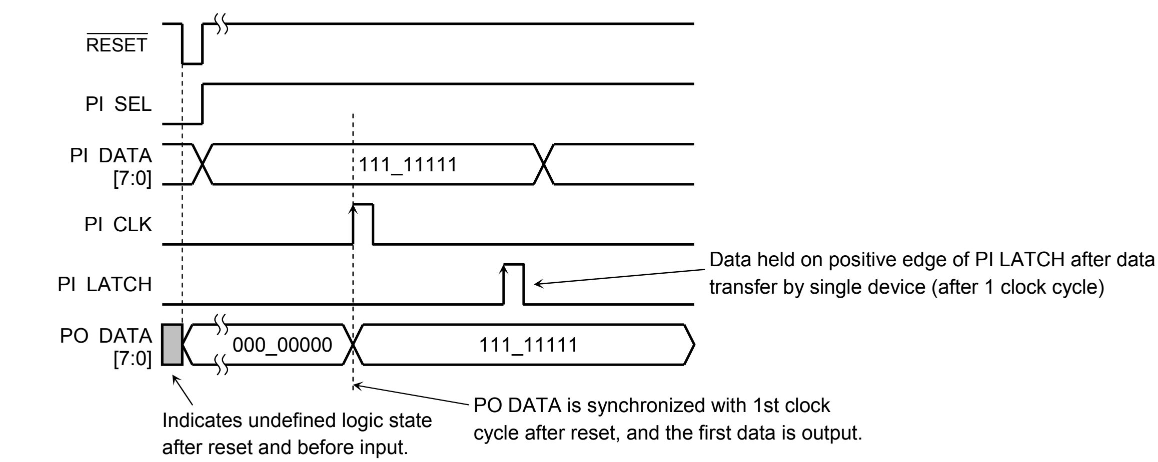
Serial data transfer timing
(SI SEL = L, input of dot adjustment data for DAC4)



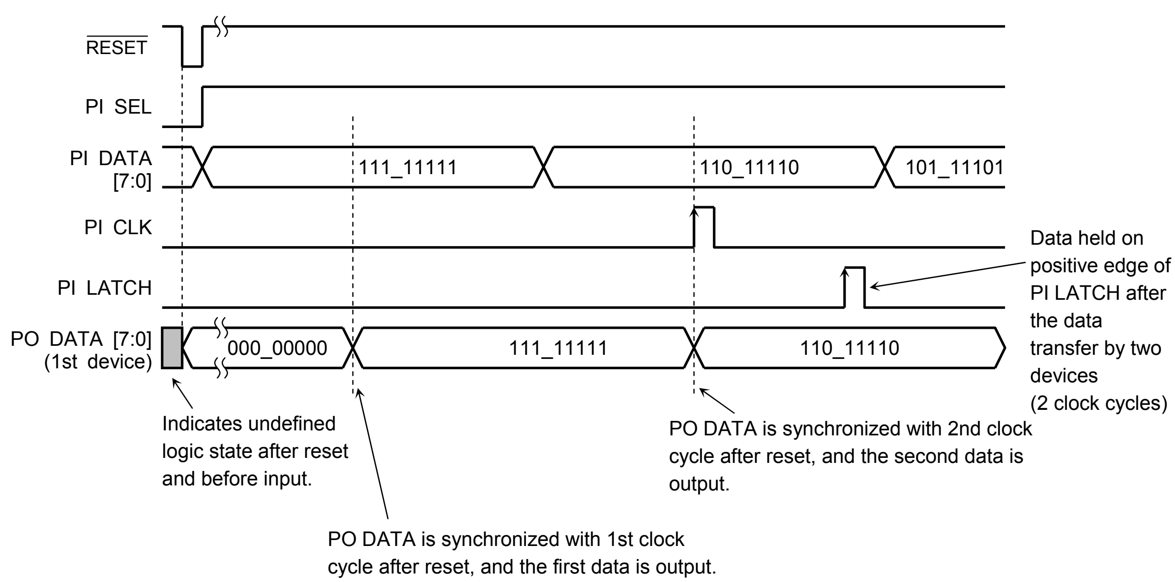
Parallel data transfer: All dot adjustment DAC3. (data register PI REG1 [7:0])

Process	PI DATA [7:0]	PI CLK	PI LATCH	PI SEL	PO DATA [7:0]	Operation and Function
1	H or L	↑ (×1)	L	H	H or L	Selects total dot adjustment (8-bit, 3-bit and 5-bit) for input data. Data is transferred to PI REG1 on 128th positive edge of PI CLK.
2	H or L	L	↑ (×1)	H	No change	Holds the data transferred to PI REG1. Set is reflected on all dot adjustment from the moment when it is held.

Parallel data transfer timing (all dot adjustment, PI SEL = H, single device)



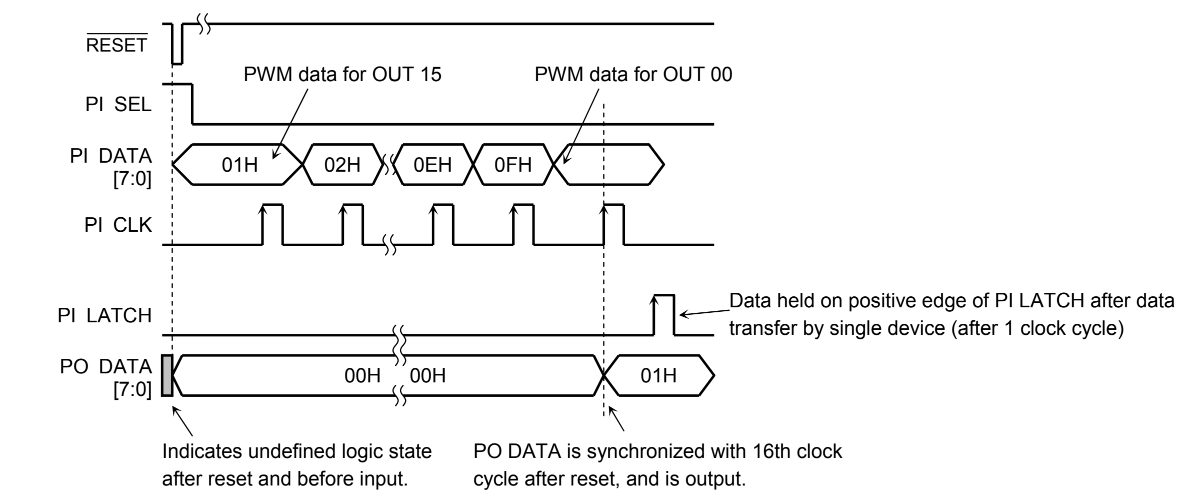
Parallel data transfer timing (all dot adjustment, PI SEL = H, two devices connected in cascade)



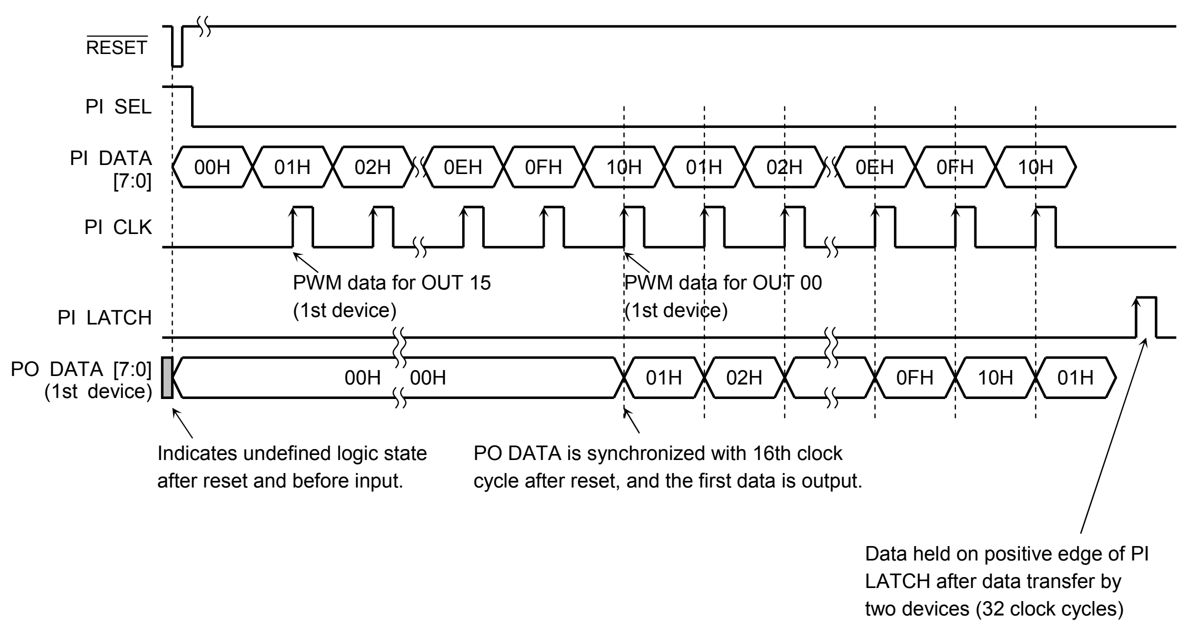
Parallel data transfer PMW display data (data register PI REG2 [127:0])

Process	PI DATA	PI CLK	PI LATCH	PI SEL	PO DATA	Operation and Function
1	H or L	↑ (×16)	L	L	H or L	Selects for input data of PWM display data (8 bit × 16). Data is transferred to PI REG2 on 16th positive edge of PI CLK.
2		L	↑ (×1)	L	No change	Holds the data transferred to PI REG2. Set is reflected on PWM 256 grayscales from the next BLANK = L when it is held.

Parallel data transfer timing (PWM data PI SEL = L, single device)



Parallel data transfer timing (PWM data PI SEL = L, two devices connected in cascade)



Details all dot adjustment setting using PWMCLK division (PI REG1 [7:5])

$\overline{RESET}$	PI SEL	BCEN	PI REG1 [7:5]	PWMCLK Divisor	Operation and Function	Notes
H	H	H	LLL	PWM CLK = 8/8 PWMCLK (Hz)	The period of PWMCLK is set to equal the change in the PWM pulse width data. 1LSB.	When PI SEL = H is selected, 3 bits on MSB sides are corresponding to set of standard current adjustment by PWM frequency dividing. PI REG [7:5] varies the pulse width of PWM data corresponding to 1 LSB for eight levels and adjusts brightness. This setting values affects pulse widths on all outputs.
H	H	H	LLH ↑ ↓ HHL	7/8 PWMCLK to 2/8 PWMCLK	Variable does the frequency of PWMCLK to 1/8 of the minimal. It is set in 8 levels. 6-bit DAC performance Maximum input: PWMCLK = 20 MHz	
H	H	H	HHH	PWMCLK = 1/8 PWMCLK (Hz)	The period of PWMCLK is set to one-eighth the change in the PWM pulse width data. 1 LSB.	
	X	H	LLL	PWMCLK = 8/8 PWMCLK (Hz)	The period of PWMCLK is set to equal the change in the PWM pulse width data. 1 LSB.	
H	H	L	XXX	Unchanged	BCEN signal does not affect PWMCLK frequency dividing.	Data input is still enabled if BCEN = L. Output current level reflects input settings.

DAC3: Details of all dot adjustment setting for DAC3 (PI REG2 [4:0])

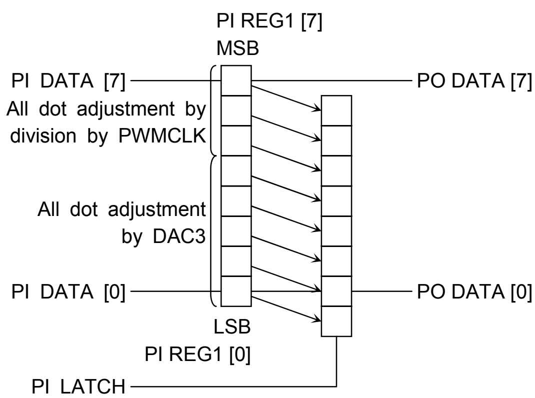
$\overline{RESET}$	PI SEL	PI REG1 [4:0]	BCEN	Current Rate	Operation and Function	Notes
H	H	HHHHH	H	100% (1.0)	100% of base current value as set using DAC1 and DAC2 current adjustment and DAC4 dot adjustment	When PI SEL = H is selected, 5 bits on LSB side are corresponding to set of surface brightness adjustment. The output current can be set to one of 32 levels.
H	H	HHHHL ↑ ↓ LLLLH	H	(0.9839) ↑ 1LSB = ±1.61% (±0.0161) ↓ (0.5161)	Any one of 32 levels in the range 50%~100% of the current can be set. (1 LSB = 1.61%) 5-bit DAC performance 1LSB variation: ±1.61% Non linearity error: ±1/2LSB Differential non linearity error: ±1/2LSB (No guarantee for monotonicity)	
H	H	LLLLL	H	50% (0.5)	50% of base current value as set using DAC1 and DAC2 current adjustment and DAC4 dot adjustment	
	X	HHHHH	H	100% (1.0)	Initial state after input of reset signal: 100% of base current value set as described above	
H	X	HHHHH	L	100% (1.0)	Initial state after input of DCEN signal: 100% of base current value set as described above	Data input is still enabled if BCEN = L. If BCEN = H, adjustment is performed at the same time.

Detailed PWM 256 grayscales setting (PI REG2 [127:0], 16 × 8 bits)

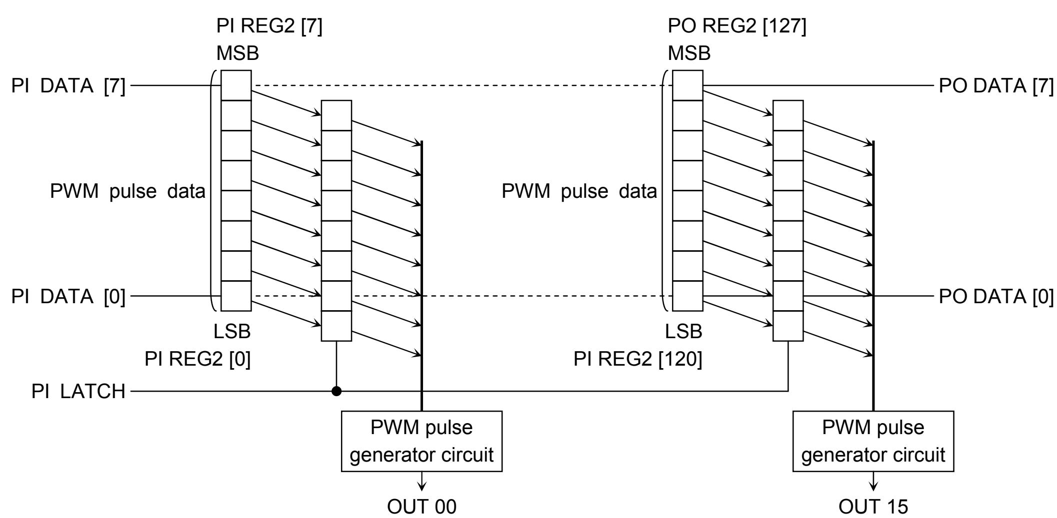
$\overline{RESET}$	PI SEL	1 word (8 bits) of PI REG2	Output Pulse Rate	Operation and Function	Notes
H	L	HHHHHHHH	255/255 100%	Output pulse width is at its maximum value when input data is FF.	When PI SEL = L, The PWM grayscale controls the output pulse width. 16 × 8-bit words are transferred in parallel. 1 word is the PWM data of each output pulse width is set in 256 step. PI REG2 [7:0] → PWM data for OUT 00. PI REG2 [15:8] → PWM data for OUT 01. PI REG2 [127:120] → PWM data for OUT 15. Minimum output pulse width is 1/PWMCLK.
H	L	HHHHHHHL ↑ ↓ LLLLLLLH	—	The input data can be used to control the PWM pulse width and hence generate 256 grayscales.	
H	L	LLLLLLLL	0/255 0%	Outputs are OFF when the input data is 00.	
	X	LLLLLLLL	0/255 0%	Early condition after the reset signal input is set in 0/256 (output off).	

Polarity of serial input data for all dot adjustment (PI REG [7:0]) and PWM 256 grayscales (PI REG2 [127:0])

Parallel data transfer timing
(PI SEL = H, selects data input for all dot adjustment for DAC3.)



(PI SEL = L, selects data input for PWM 256 grayscales.)



Reference table: output current setting vales (1)

DAC1 (2-bit)			DAC2 (6-bit)			DAC3 (5-bit)			DAC4 (6-bit)		
No.	Input Data	Current Rate1	No.	Input Data	Current Rate2	No.	Input Data	Current Rate3	No.	Input Data	Current Rate4
3	11	1.00	63	111111	1.000	31	**11111	**1.000	63	111111	63
2	10	0.75	62	111110	0.990	30	11110	0.984	62	111110	62
1	01	0.50	61	111101	0.981	29	11101	0.968	61	111101	61
0	**00	**0.25	60	111100	0.971	28	11100	0.952	60	111100	60
—	—	—	59	111011	0.962	27	11011	0.936	59	111011	59
—	—	—	58	111010	0.952	26	11010	0.919	58	111010	58
—	—	—	57	111001	0.943	25	11001	0.903	57	111001	57
—	—	—	56	111000	0.933	24	11000	0.887	56	111000	56
—	—	—	55	110111	0.924	23	10111	0.871	55	110111	55
—	—	—	54	110110	0.914	22	10110	0.855	54	110110	54
—	—	—	53	110101	0.905	21	10101	0.839	53	110101	53
—	—	—	52	110100	0.895	20	10100	0.823	52	110100	52
—	—	—	51	110011	0.886	19	10011	0.807	51	110011	51
—	—	—	50	110010	0.876	18	10010	0.790	50	110010	50
—	—	—	49	110001	0.867	17	10001	0.774	49	110001	49
—	—	—	48	110000	0.857	16	10000	0.758	48	110000	48
—	—	—	47	101111	0.848	15	01111	0.742	47	101111	47
—	—	—	46	101110	0.838	14	01110	0.726	46	101110	46
—	—	—	45	101101	0.829	13	01101	0.710	45	101101	45
—	—	—	44	101100	0.819	12	01100	0.694	44	101100	44
—	—	—	43	101011	0.820	11	01011	0.677	43	101011	43
—	—	—	42	101010	0.800	10	01010	0.661	42	101010	42
—	—	—	41	101001	0.791	9	01001	0.645	41	101001	41
—	—	—	40	101000	0.781	8	01000	0.629	40	101000	40
—	—	—	39	100111	0.771	7	00111	0.613	39	100111	39
—	—	—	38	100110	0.762	6	00110	0.597	38	100110	38
—	—	—	37	100101	0.752	5	00101	0.581	37	100101	37
—	—	—	36	100100	0.743	4	00100	0.565	36	100100	36
—	—	—	35	100011	0.733	3	00011	0.549	35	100011	35
—	—	—	34	100010	0.724	2	00010	0.532	34	100010	34
—	—	—	33	100001	0.714	1	00001	0.516	33	100001	33
—	—	—	32	100000	0.705	0	00000	0.500	32	100000	32
—	—	—	31	011111	0.695	—	—	—	31	011111	31
—	—	—	30	011110	0.686	—	—	—	30	011110	30
—	—	—	29	011101	0.676	—	—	—	29	011101	29
—	—	—	28	011100	0.667	—	—	—	28	011100	28
—	—	—	27	011011	0.657	—	—	—	27	011011	27
—	—	—	26	011010	0.648	—	—	—	26	011010	26
—	—	—	25	011001	0.638	—	—	—	25	011001	25
—	—	—	24	011000	0.629	—	—	—	24	011000	24
—	—	—	23	010111	0.619	—	—	—	23	010111	23
—	—	—	22	010110	0.610	—	—	—	22	010110	22
—	—	—	21	010101	0.600	—	—	—	21	010101	21
—	—	—	20	010100	0.591	—	—	—	20	010100	20
—	—	—	19	010011	0.581	—	—	—	19	010011	19
—	—	—	18	010010	0.571	—	—	—	18	010010	18
—	—	—	17	010001	0.562	—	—	—	17	010001	17
—	—	—	16	010000	0.552	—	—	—	16	010000	16
—	—	—	15	001111	0.543	—	—	—	15	001111	15
—	—	—	14	001110	0.533	—	—	—	14	001110	14
—	—	—	13	001101	0.524	—	—	—	13	001101	13
—	—	—	12	001100	0.514	—	—	—	12	001100	12
—	—	—	11	001011	0.505	—	—	—	11	001011	11
—	—	—	10	001010	0.495	—	—	—	10	001010	10
—	—	—	9	001001	0.486	—	—	—	9	001001	9
—	—	—	8	001000	0.476	—	—	—	8	001000	8
—	—	—	7	000111	0.467	—	—	—	7	000111	7
—	—	—	6	000110	0.457	—	—	—	6	000110	6
—	—	—	5	000101	0.448	—	—	—	5	000101	5
—	—	—	4	000100	0.438	—	—	—	4	000100	4
—	—	—	3	000011	0.429	—	—	—	3	000011	3
—	—	—	2	000010	0.419	—	—	—	2	000010	2
—	—	—	1	000001	0.410	—	—	—	1	000001	1
—	—	—	0	**000000	**0.4	—	—	—	0	**000000	0

Note 7: **: Indicates post-reset initialization value ($\overline{\text{RESET}}$ = L).

Note 8: The formula for calculating resistance settings is as follows: This value is theory value. Actual current value contains error and so on in this value.
REXT [kΩ] = (1.9 × current rate 1 × current rate 2 × current rate 3 / output current [mA]) × (1 + (7 × current rate 4 / 105)) × 19.4

Reference table: output current setting value (2)
Reference value for standard current adjustment under conditions:
R_{EXT} = 2.7 kΩ (fixed), all dot adjustment = MSB and dot adjustment = MSB

Unit: mA

		DAC2															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DAC1	0	7.1	7.3	7.4	7.6	7.8	7.9	8.1	8.3	8.5	8.6	8.8	9.0	9.1	9.3	9.5	9.6
	1	14.2	14.5	14.9	15.2	15.6	15.9	16.2	16.6	16.9	17.2	17.6	17.9	18.3	18.6	18.9	19.3
	2	21.3	21.8	22.3	22.8	23.3	23.8	24.3	24.9	25.4	25.9	26.4	26.9	27.4	27.9	28.4	28.9
	3	28.4	29.1	29.6	30.4	31.1	31.8	32.5	33.1	33.8	34.5	35.2	35.8	36.5	37.2	37.9	38.6

		DAC2															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DAC1	0	9.8	10.0	10.1	10.3	10.5	10.7	10.8	11.0	11.2	11.3	11.5	11.7	11.8	12.0	12.2	12.3
	1	19.6	19.9	20.3	20.6	21.0	21.3	21.6	22.0	22.3	22.7	23.0	23.3	23.7	24.0	24.3	24.7
	2	29.4	29.9	30.4	30.9	31.4	32.0	32.5	33.0	33.5	34.0	34.5	35.0	35.5	36.0	36.5	37.0
	3	39.2	39.9	40.6	41.2	41.9	42.6	43.3	44.0	44.6	45.3	46.0	46.7	47.3	48.0	48.7	49.4

		DAC2															
		32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
DAC1	0	12.5	12.7	12.9	13.0	13.2	13.4	13.5	13.7	13.9	14.0	14.2	14.4	14.5	14.7	14.9	15.0
	1	25.0	25.4	25.7	26.0	26.4	26.7	27.0	27.4	27.7	28.1	28.4	28.7	29.1	29.4	29.8	30.1
	2	37.5	38.0	38.6	39.0	39.6	40.1	40.6	41.1	41.6	42.1	42.6	43.1	43.6	44.1	44.6	45.1
	3	50.0	50.7	51.4	52.1	52.7	53.4	54.1	54.8	55.4	56.1	56.8	57.5	58.1	58.8	59.5	60.2

		DAC2															
		48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
DAC1	0	15.2	15.4	15.6	15.7	15.9	16.1	16.2	16.4	16.6	16.7	16.9	17.1	17.2	17.4	17.6	17.8
	1	30.4	30.8	31.1	31.4	31.8	32.1	32.5	32.8	33.1	33.5	33.8	34.1	34.5	34.8	35.2	35.5
	2	45.6	46.1	46.7	47.2	47.7	48.2	48.7	49.2	49.7	50.2	50.7	51.2	51.7	52.2	52.7	53.2
	3	60.9	61.5	62.2	62.9	63.6	64.2	64.9	65.6	66.3	66.9	67.6	68.3	69.0	69.6	70.3	71.0

Temperature detection function (can be monitored via the ALARM1 pin.)

Perform two-stage temperature detection as described in the table below (TSD1/TSD2).

Junction Temperature [°C]	ALARM1	OUT 00~OUT 15	Function
–40~120	OFF	Normal operation	—
120~	ON	Normal operation	When the chip temperature reaches the specified range the ALARM1 signal goes Low (TSD1), Other functions are not affected.
140~	ON	OFF	When the chip temperature reaches the specified range the ALARM1 signal goes Low and all output pins are turned OFF (TSD2). Outputs are re-enabled on the positive edge of TSENA or when the $\overline{\text{RESET}}$ signal goes Low. Neither of these causes the internal data to be reset. If $\overline{\text{RESET}}$ pin = L, all internal data is reset.

Output-open detection function (can be monitored via the ALARM2 pin.)

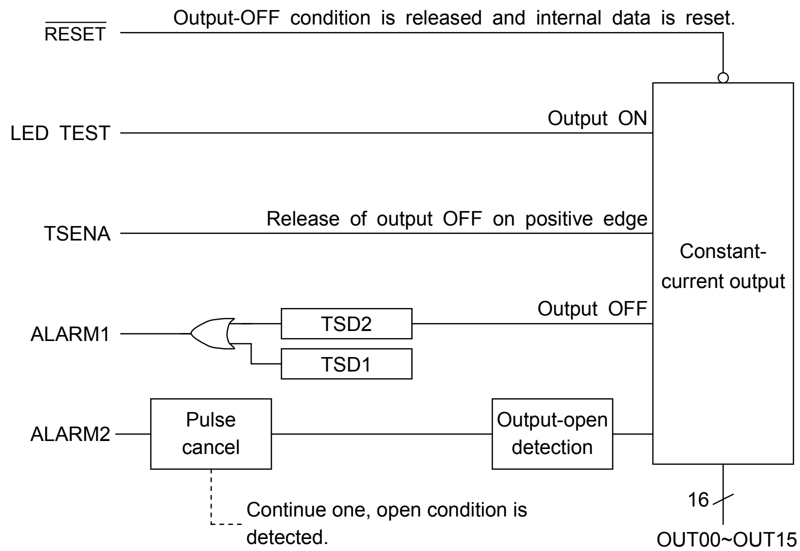
Reform output-open detection as described in the table below.

Output Voltage [V]	ALARM2	Function
$\geqq V_{DD} \times 0.04$	OFF	—
$\leqq V_{DD} \times 0.04$	ON	The output-open condition is detected when the ARARM2 pin signal is ON and the specified voltage level is detected. (it is also detected when the output voltage falls to near GND for some reason)

Pulse cancellation circuit (when monitored using output-open detection pin ARARM2.)

PWMCLK	ALARM2	Function
Input signal	Operating	
No input	Always OFF	The built-in pulse cancellation circuit is designed to prevent malfunction. However, if there is no input on PWMCLK, ALARM2 output will not be turned ON.

Block Diagram of Protection Circuit

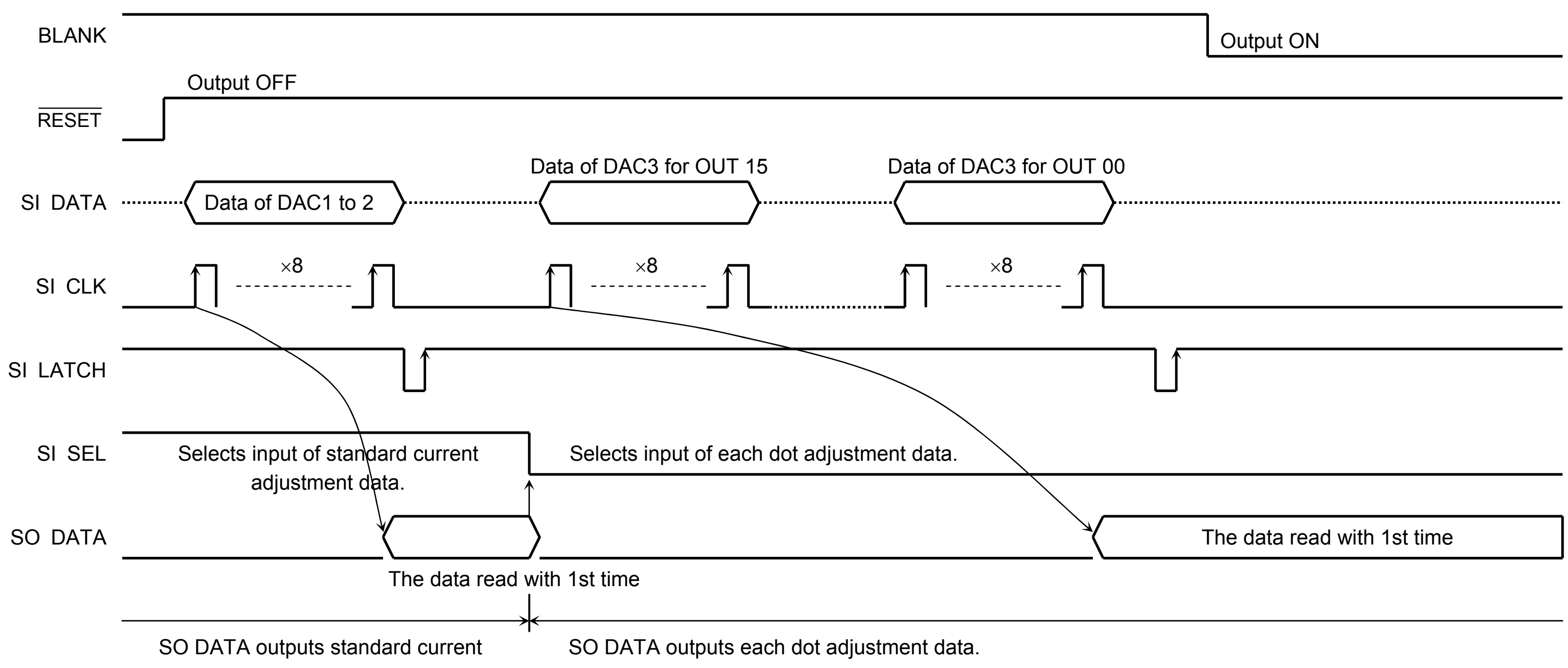


Protection circuit function
Operating chart (terminal for TESNA, ALARM1 and outputs OUT 00~OUT 15)

TSENA	$\overline{\text{RESET}}$	Junction Temperature (unit: °C)			ALARM1	OUT 00 ~ OUT 15	Function
		Tj ≦ 120°C	TSD1 120 ≦ Tj ≦ 160°C	TSD2 140 ≦ Tj ≦ 180°C			
X	L	○	—	—	OFF	ON	Device reset
X	H	○	—	—	OFF	ON	Outputs operate normally.
X	L	—	○	—	ON	ON	Device reset
X	H	—	○	—	ON	Normal operation	ALARM1 goes Low, indicating a rise in temperature. Outputs operate normally.
X	L	—	—	○	ON	OFF	Even after a reset, if the junction temperature is high, outputs are turned OFF.
X	H	—	—	○	ON	OFF	ALARM1 goes Low, indicating a rise in temperature. Outputs operate normally.

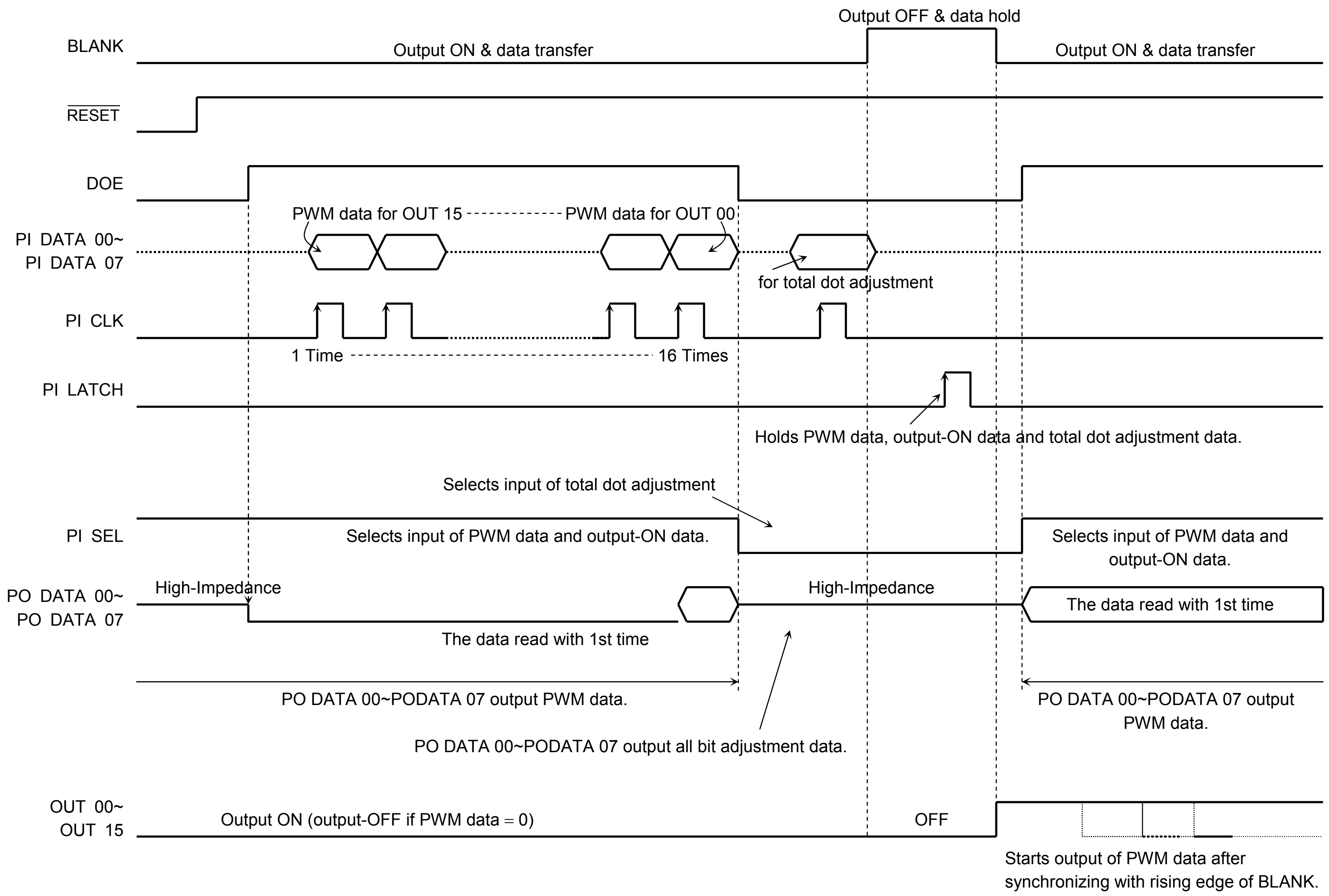
Note 9: The internal operation of the TSD circuit is independent of the TSENA and $\overline{\text{RESET}}$ pin voltage levels.

Serial Data Input Timing Chart



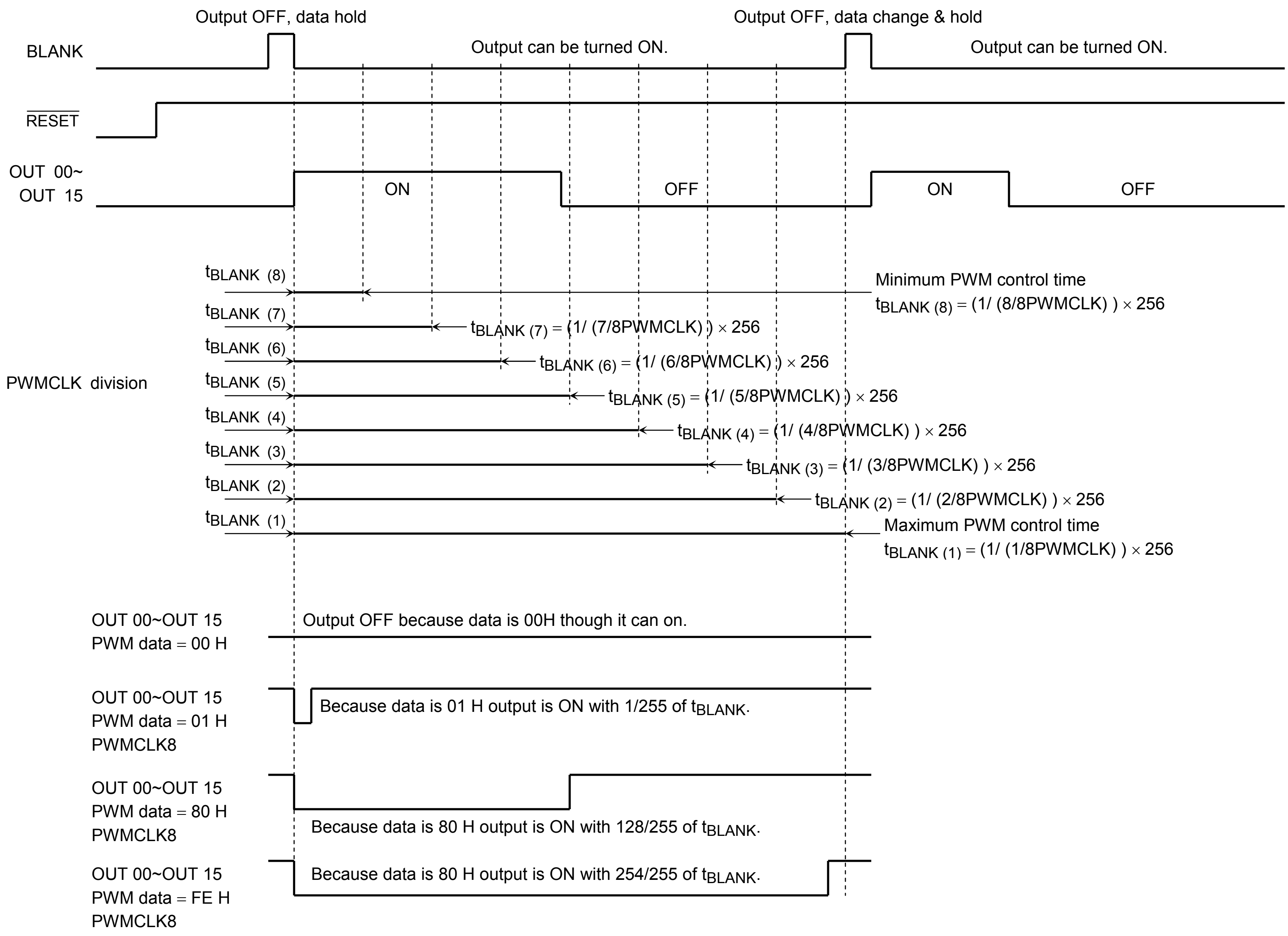
Note 10: Serial data input has no effect on the ON/OFF state of the outputs.
When the SI LATCH signal holds the serial data, the output current values and output pulse width are affected.

Parallel Data Input Timing Chart



Note 11: The BLANK signal has not effect on parallel data input. The PWM pulse can be controlled using the BLANK signal.
It is recommended that, on completion of data transfer, BLANK be set to High and outputs be turned OFF.

PWM Operating Timing Chart and All Bit Adjustment Using Division by PWMCLK



Note 12: PWM operation timing:

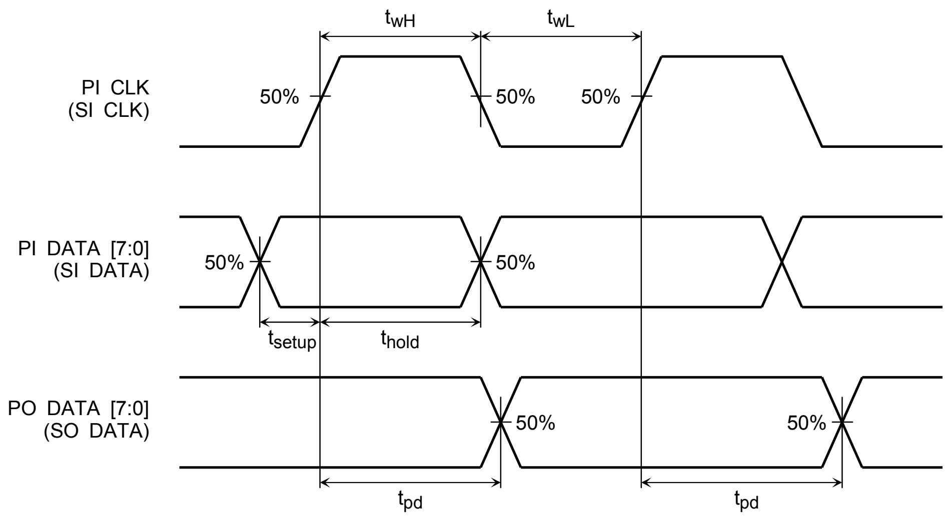
PWM pulse output on the output pins is initiated when BLANK goes Low. (there is simultaneous output on all 16 pins)
Output pulse only once toward BLANK signal's changing once in L from H.
Hence, if PWM data is to be re-used, BLANK must be pulled Low again.

PWMCLK division:

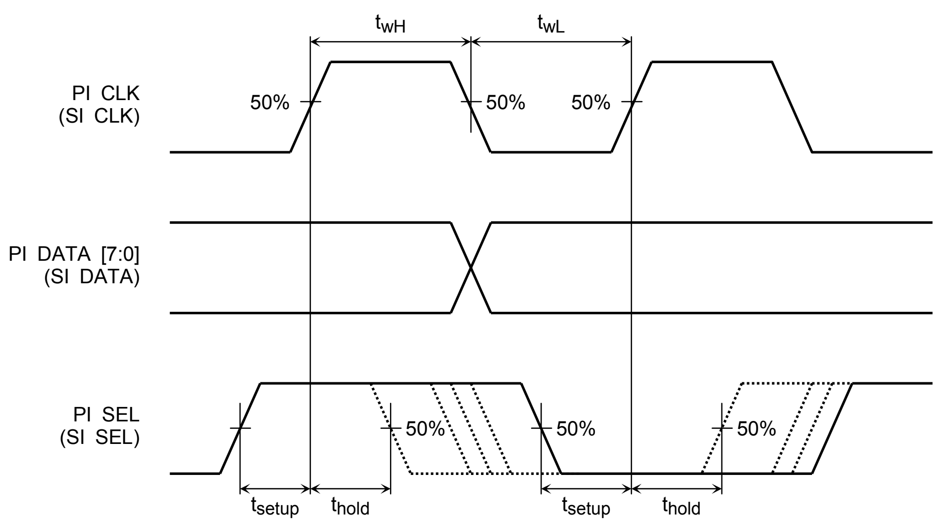
As shown in the central part of the upper figure, the brightness of the LED module can be set to any one of eight levels without adjusting the current value, simply by dividing by PWMCLK.
For large-scale brightness adjustment, division by PWMCLK is recommended.

Logic Input and Output Timing Waveforms

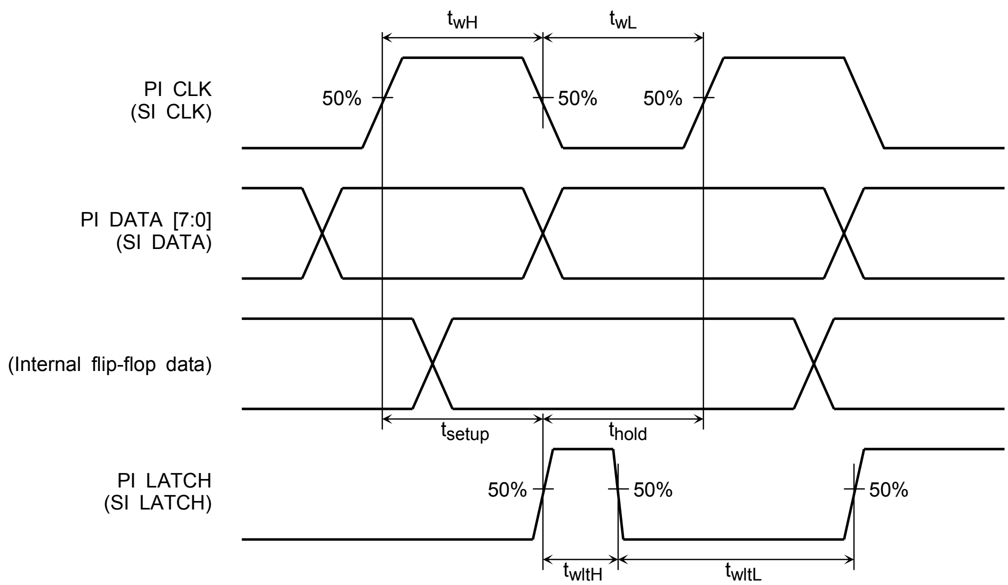
1. **PI CLK (SI CLK) vs. PI DATA [7:0] (SI DATA)**
   PI CLK (SI CLK) vs. PO DATA [7:0] (SO DATA)



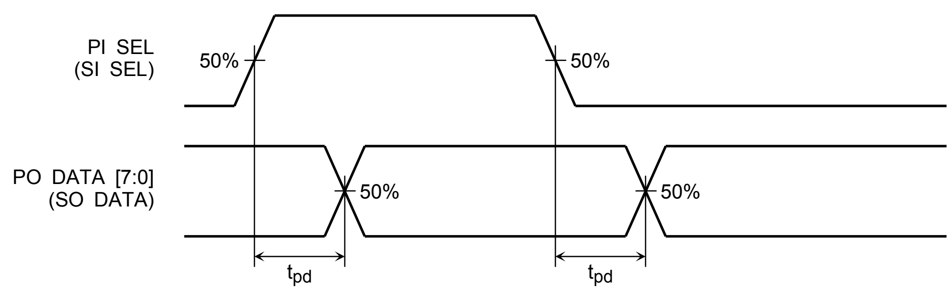
2. **PI SEL (SI SEL) vs. PI CLK (SI CLK)**



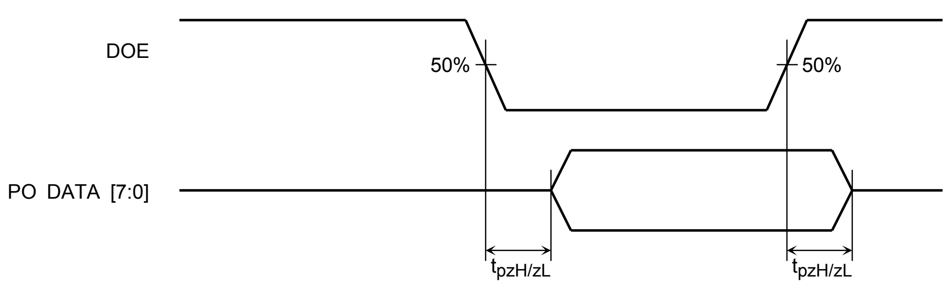
3. PI LATCH (SI LATCH) vs. PI CLK (SI CLK)



4. PI SEL (SI SEL) vs. PO DATA 00~PO DATA 07 (SO DATA)

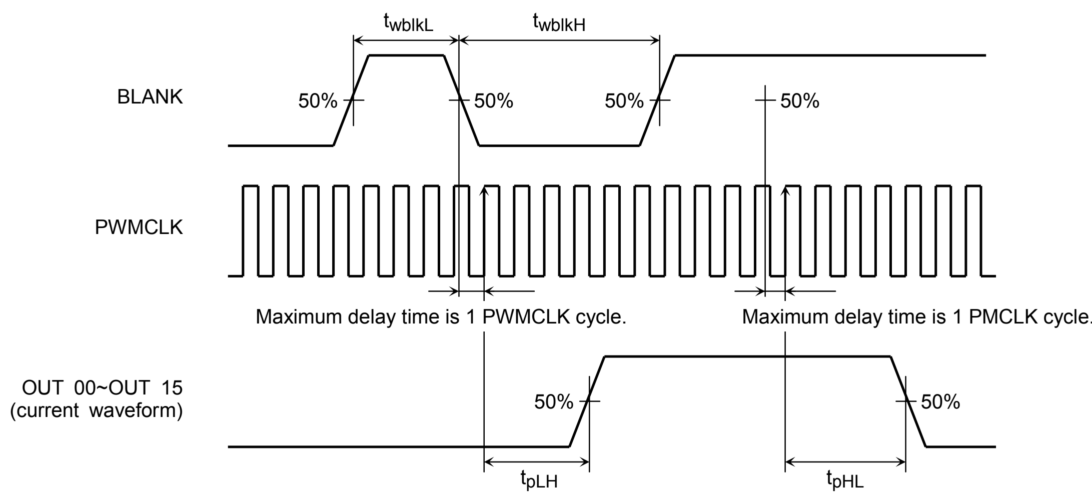


5. DOE vs. PO DATA 00~PO DATA 07

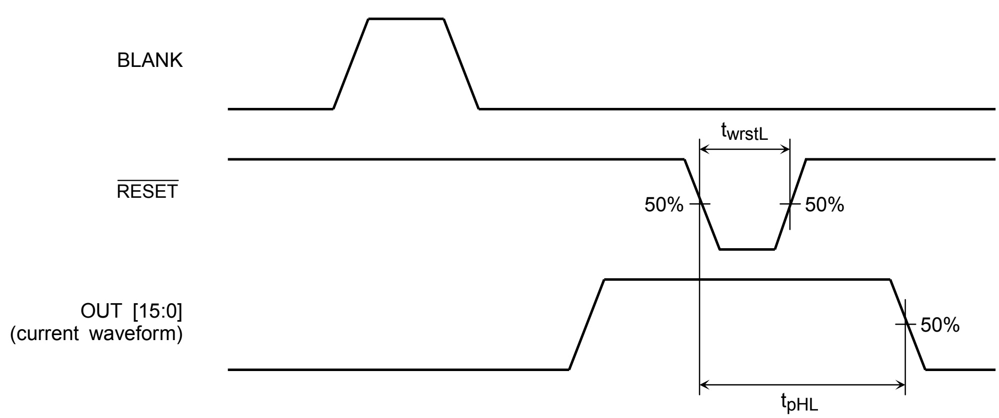


Logic Input and Constant-current Output Timing Waveforms

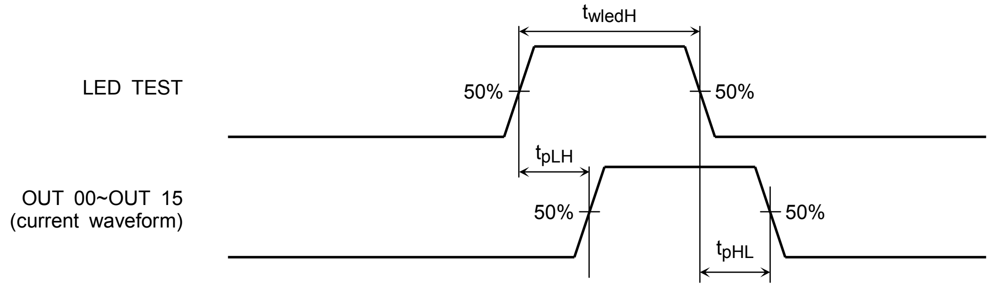
1. BLANK vs. OUT 00~OUT 15 with PWMCLK



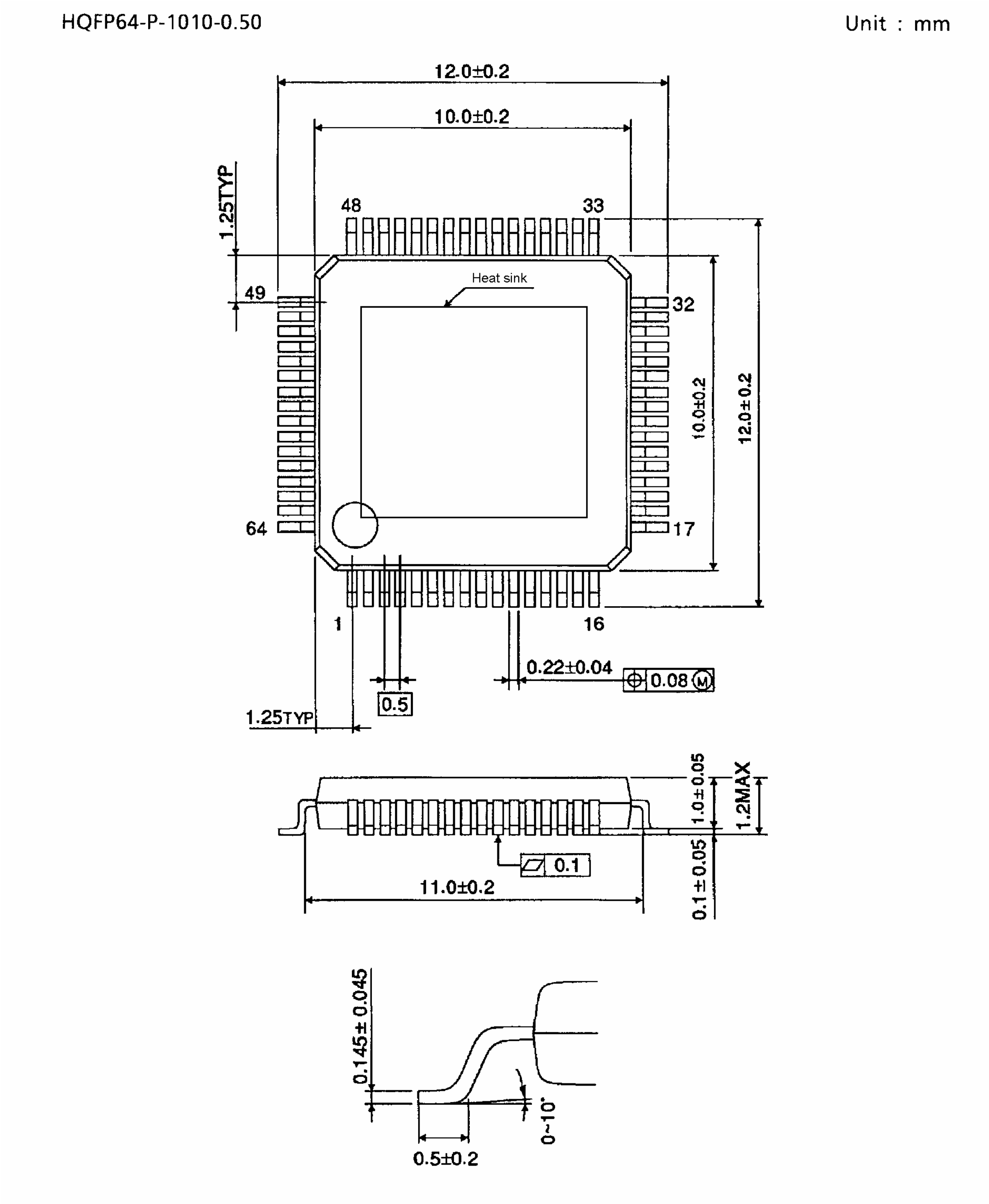
2. RESET vs. OUT 00~OUT 15



3. LED TEST vs. OUT 00~OUT 15



Package Dimensions



Weight: 0.26 g (typ.)

About solderability, following conditions were confirmed

- Solderability

  Use of Sn-63Pb solder Bath
  · solder bath temperature = 230°C
  · dipping time = 5 seconds
  · the number of times = once
  · use of R-type flux

  Use of Sn-3.0Ag-0.5Cu solder Bath
  · solder bath temperature = 245°C
  · dipping time = 5 seconds
  · the number of times = once
  · use of R-type flux