TC1043

Linear Building Block – Low Power Voltage Reference with Dual Op Amp, Dual Comparator, and Shutdown Mode

Features

- Combines Two Op Amps, Two Comparators and a Voltage Reference in a Single Package
- Optimized for Single-Supply Operation
- Small Package: 16-Pin QSOP
- Ultra Low Input Bias Current: Less than 100pA
- Low Quiescent Current: Operating 16µA (Typ.)
  Shutdown 6µA (Typ.)
- Rail-to-Rail Inputs and Outputs
- Operates Down to V_{DD} = 1.8V
- Reference and One Comparator Remain Active in Shutdown to Provide Supervisory Functions

Applications

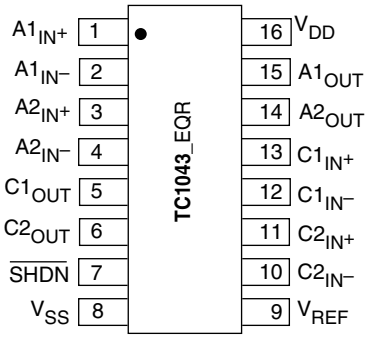
- Power Management Circuits
- Battery Operated Equipment
- Consumer Products
- Replacements for Discrete Components

Device Selection Table

Part Number	Package	Temperature Range
TC1043CEQR	16-Pin QSOP	-40°C to +85°C

Package Type

16-Pin QSOP



General Description

The TC1043 is a mixed-function device combining two general purpose op amps, two general purpose comparators, and a voltage reference in a single 16-Pin package.

This increased integration allows the user to replace two or three packages, saving space, lowering supply current, and increasing system performance. A shutdown input, $\overline{SHDN}$, disables the op amps and one of the comparators, placing their outputs in a high-impedance state. The reference and one comparator stay active in shutdown mode. Standby power consumption is typically 6µA. Both the op amps and comparators have rail-to-rail inputs and outputs which allows operation from low supply voltages with large input and output signal swings.

Packaged in a 16-Pin QSOP, the TC1043 is ideal for applications requiring high integration, small size and low power.

1.0 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage 6.0V
Voltage on Any Pin ..... (V_{SS} – 0.3V) to (V_{DD} +0.3V)
Junction Temperature.....+150°C
Operating Temperature Range.....-40°C to +85°C
Storage Temperature Range .....-55°C to +150°C

*Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods my affect device reliability.

TC1043 ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Typical values apply at 25°C and V_{DD} = 3V. Minimum and maximum values apply for T_A = -40° to + 85°C, and V_{DD} = 1.8V to 5.5V, unless otherwise specified.

Symbol	Parameter	Min.	Typ	Max	Units	Test Conditions
V_{DD}	Supply Voltage	1.8	—	5.5	V	
I_Q	Supply Current Operating	—	16	30	µA	All outputs unloaded, $\overline{SHDN}$ = V_{DD}
I_{SHDN}	Supply Current, Shutdown	—	6	10	µA	CMPTR2 and V_{REF} Outputs unloaded, $\overline{SHDN}$ = V_{SS}
Shutdown Input						
V_{IH}	Input High Threshold	80% V_{DD}	—	—	V	
V_{IL}	Input Low Threshold	—	—	20% V_{DD}	V	
I_{SI}	Shutdown Input Current	—	—	±100	nA	
Op Amps						
T_{SEL}	Select Time	—	15	—	µsec	(V_{OUT} from $\overline{SHDN}$ = V_{IH}) R_L = 10kΩ to V_{SS}
T_{DESEL}	Deselect Time	—	100	—	nsec	(V_{OUT} from $\overline{SHDN}$ = V_{IL}) R_L = 10kΩ to V_{SS}
R_{OUT}(SD)	Output Resistance in Shutdown	20	—	—	MΩ	$\overline{SHDN}$ = V_{SS}
C_{OUT}(SD)	Output Capacitance in Shutdown	—	—	6	pF	$\overline{SHDN}$ = V_{SS}
A_{VOL}	Large Signal Voltage Gain	—	100	—	V/mV	R_L = 10kΩ, V_{DD} = 5V
V_{ICMR}	Common Mode Input Voltage Range	V_{SS} - 0.2	—	V_{DD} + 0.2	V	
V_{OS}	Input Offset Voltage		±100 ±0.3	±500 ±1.5	µV mV	V_{DD} = 3V, V_{CM} = 1.5V, T_A = 25°C, T_A = -40°C to 85°C
I_B	Input Bias Current	-100	50	100	pA	T_A = 25°C, V_{CM} = V_{DD} to V_{SS}
$V_{OS(DRIFT)}$	Input Offset Voltage Drift	—	±4	—	µV/°C	V_{DD} = 3V, V_{CM} = 1.5V
GBWP	Gain-Bandwidth Product	—	90	—	kHz	V_{DD} = 1.8V to 5.5V V_O = V_{DD} to V_{SS}
SR	Slew Rate	—	35	—	mV/µsec	C_L = 100pF R_L = 1MΩ to GND Gain = 1 V_{IN} = V_{SS} to V_{DD}
V_{OUT}	Output Signal Swing	V_{SS} + 0.05	—	V_{SS} - 0.05	V	R_L = 10kΩ
CMRR	Common Mode Rejection Ratio	70	—	—	dB	T_A = 25°C, V_{DD} = 5V V_{CM} = V_{DD} to V_{SS}
PSRR	Power Supply Rejection Ratio	80	—	—	dB	T_A = 25°C, V_{CM} = V_{SS} V_{DD} = V_{DD} to V_{SS}
I_{SRC}	Output Source Current	3	—	—	mA	IN+ = V_{DD}, IN- = V_{SS} Output Shorted to V_{SS} V_{DD} = 1.8V, Gain = 1
I_{SINK}	Output Sink Current	4	—	—	mA	IN+ = V_{SS}, IN- = V_{DD} Output Shorted to V_{DD} V_{DD} = 1.8V, Gain = 1
En	Input Noise Voltage	—	10	—	μV_{PP}	0.1Hz to 10Hz
en	Input Noise Voltage Density	—	125	—	nV/$\sqrt{Hz}$	1kHz

TC1043 ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Typical values apply at 25°C and V_{DD} = 3V. Minimum and maximum values apply for T_A = - 40° to + 85°C, and V_{DD} = 1.8V to 5.5V, unless otherwise specified.

Symbol	Parameter	Min.	Typ	Max	Units	Test Conditions
Comparators						
R_{OUT}(SD)	Output Resistance in Shutdown	20	—	—	MΩ	$\overline{SHDN}$ = V_{SS}
C_{OUT}(SD)	Output Capacitance in Shutdown	—	—	5	pF	$\overline{SHDN}$ = V_{SS}
T_{SEL}	Select Time (For Valid Output)	—	20	—	µsec	V_{OUT} from $\overline{SHDN}$ = V_{IH} R_L =10kΩ to V_{SS}
T_{DESEL}	Deselect Time	—	500	—	nsec	V_{OUT} from $\overline{SHDN}$ = V_{IL} R_L =10kΩ to V_{SS}
V_{ICMR}	Common Mode Input Voltage Range	V_{SS} – 0.2	—	V_{DD} + 0.2	V	
V_{OS}	Input Offset Voltage	–5 –5	—	+5 +5	mV	V_{DD} = 3V, V_{CM} = 1.5V T_A = 25°C T_A = -40°C to 85°C
I_B	Input Bias Current	—	—	±100	pA	T_A = 25°C, IN+, IN- = V_{DD} to V_{SS}
V_{OH}	Output High Voltage	V_{DD} – 0.3	—	—	V	R_L = 10kΩ to V_{SS}
V_{OL}	Output Low Voltage	—	—	0.3	V	R_L = 10kΩ to V_{DD}
CMRR	Common Mode Rejection Ratio	66	—	—	dB	T_A = 25°C, V_{DD} = 5V V_{CM} = V_{DD} to V_{SS}
PSRR	Power Supply Rejection Ratio	60	—	—	dB	T_A = 25°C, V_{CM} = 1.2V V_{DD} = 1.8V to 5V
I_{SRC}	Output Source Current	1	—	—	mA	IN+ = V_{DD}, IN- = V_{SS} Output Shorted to V_{SS} V_{DD} = 1.8V
I_{SINK}	Output Sink Current	2	—	—	mA	IN+ = V_{SS}, IN- = V_{DD}, Output Shorted to V_{DD} V_{DD} = 1.8V
t_{PD1}	Response Time	—	4	—	µsec	100mV Overdrive, C_L = 100pF
t_{PD2}	Response Time	—	6	—	µsec	10mV Overdrive, C_L = 100pF
Voltage Reference						
V_{REF}	Reference Voltage	1.176	1.200	1.224	V	
$I_{REF(SOURCE)}$	Source Current	50	—	—	µA	
$I_{REF(SINK)}$	Sink Current	50	—	—	µA	
$C_{L(REF)}$	Load Capacitance	—	—	100	pF	
N_{VREF}	Voltage Noise	—	20	—	μV_{RMS}	100Hz to 100kHz
	Noise Density	—	1.0	—	$\mu V/\sqrt{Hz}$	1kHz

2.0 PIN DESCRIPTION

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Symbol	Description
1	$A1_{IN+}$	Op Amp Non-Inverting Input
2	$A1_{IN-}$	Op Amp Inverting Input
3	$A2_{IN+}$	Op Amp Non-Inverting Input
4	$A2_{IN-}$	Op Amp Inverting Input
5	$C1_{OUT}$	Comparator Output
6	$C2_{OUT}$	Comparator Output
7	$\overline{SHDN}$	Shutdown Input
8	V_{SS}	Negative Power Supply
9	V_{REF}	Voltage Reference Output
10	$C2_{IN-}$	Comparator Inverting Input
11	$C2_{IN+}$	Comparator Non-Inverting Input
12	$C1_{IN-}$	Comparator Inverting Input
13	$C1_{IN+}$	Comparator Non-Inverting Input
14	$A2_{OUT}$	Op Amp Output
15	$A1_{OUT}$	Op Amp Output
16	V_{DD}	Positive Power Supply

3.0 DETAILED DESCRIPTION

The TC1043 is one of a series of very low power, linear building block products targeted at low voltage, single supply applications. The TC1043 minimum operating voltage is 1.8V and typical supply current is only 20µA (fully enabled). It combines two comparators, two op amps and a voltage reference in a single package. A shutdown mode is incorporated for easy adaptation to system power management schemes. During shutdown, all but one comparator and the voltage reference are disabled (i.e. powered down with their respective outputs at high impedance). The “still awake” comparator and voltage reference can be used as a wake-up timer, power supply monitor, LDO controller or other continuous duty circuit function.

3.1 Comparators

The TC1043 contains two comparators. The comparators input range extends beyond both supply voltages by 200mV and the outputs will swing to within several millivolts of the supplies, depending on the load current being driven.

The comparators exhibit a propagation delay and supply current which are largely independent of supply voltage. The low input bias current and offset voltage make them suitable for high impedance precision applications.

Comparator CMPTR1 is disabled during shutdown and has a high impedance output. Comparator CMPTR2 remains active.

3.2 Operational Amplifiers

The TC1043 contains two rail-to-rail op amps. The amplifiers’ input range extends beyond both supplies by 200mV and the outputs will swing to within several millivolts of the supplies depending on the load current being driven.

The amplifier design is such that large signal gain, slew rate and bandwidth are largely independent of supply voltage. The low input bias current and offset voltage of the TC1043 make it suitable for precision applications. Both op amps are disabled during shutdown and have high output impedance.

3.3 Voltage Reference

A 2.0% tolerance, internally biased, 1.20V bandgap voltage reference is included in the TC1043. It has a push-pull output capable of sourcing and sinking at least 50µA. The voltage reference remains fully enabled during shutdown.

3.4 Shutdown Input

$\overline{SHDN}$ at V_{IL} disables both op amps and one comparator. The $\overline{SHDN}$ input cannot be allowed to float. When not used, connect it to V_{DD}. The disabled comparator’s output and the two disabled op amp outputs are in a high impedance state when shutdown is active. The disabled comparator’s inputs and the two disabled op amp inputs can be driven from rail-to-rail by an external voltage when the TC1043 is in shutdown. No latch-up will occur when the device is driven to its enabled state when $\overline{SHDN}$ is set to V_{IH}.

4.0 TYPICAL APPLICATIONS

The TC1043 lends itself to a wide variety of applications, particularly in battery powered systems. It typically finds application in power management, processor supervisory, and interface circuitry.

4.1 Wake-Up Timer

Many microcontrollers have a low power “sleep” mode that significantly reduces their supply current. Typically, the microcontroller is placed in this mode via a software instruction, and returns to a fully enabled state upon reception of an external signal (“wake-up”). The wake-up signal is usually supplied by a hardware timer. Most system applications demand that this timer have a long duration (typically seconds or minutes), and consume as little supply current as possible.

The circuit shown in Figure 4-1 is a wake-up timer made from comparator CMPTR2. (CMPTR2 is used because the wake-up timer must operate when SHDN is active.) Capacitor C1 charges through R1 until a voltage equal to V_R is reached, at which point the WAKE-UP is driven active. Upon wake-up, the microcontroller resets the timer by forcing a logic low on a dedicated, open drain I/O port pin. This discharges C1 through R4 (the value of R4 is chosen to limit the maximum current sunk by the I/O port pin). With a 3V supply, the circuit as shown consumes typically 6µA and furnishes a nominal timer duration of 25 seconds.

4.2 Precision Battery Monitor

Figure 4-2 is a precision battery low/battery dead monitoring circuit. Typically, the battery low output warns the user that a battery dead condition is imminent. Battery dead typically initiates a forced shutdown to prevent operation at low internal supply voltages (which can cause unstable system operation).

The circuit of Figure 4-2 uses a single TC1043 (one op amp is unused) and only six external resistors. AMP 1 is a simple buffer, while CMPTR1 and CMPTR2 provide precision voltage detection using V_R as a reference. Resistors R2 and R4 set the detection threshold for BATTLOW, while resistors R1 and R3 set the detection threshold for BATTFAIL. The component values shown assert BATTLOW at 2.2V (typical) and BATTFAIL at 2.0V (typical). Total current consumed by this circuit is typically 22µA at 3V. Resistors R5 and R6 provide hysteresis for comparators CMPTR1 and CMPTR2 respectively.

4.3 Dual LDO with Shutdown

Figure 4-3 shows a portion of a TC1043 configured as a dual low dropout regulator with shutdown. AMP1 and AMP2 are independent error amplifiers that use V_R as a reference. Resistors RA_1, RB_1, RA_2 and RB_2 set the feedback around the amplifiers and therefore determine the output voltage settings (please see equation in the figure). RA_1, RB_1, RA_2 and RB_2 can have large ohmic values (i.e. 100’s of kΩ) to minimize supply current.

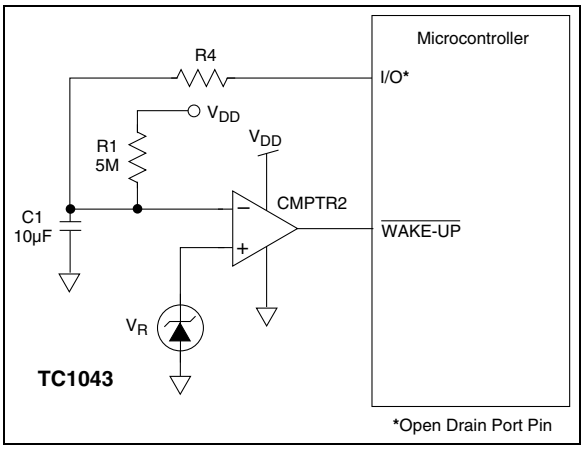
Using the 2N2222 output transistors as shown, these regulators exhibit low dropout operation. For example, with V_{OUT} = 3.0V, the typical dropout voltage is only 50mV at an output current of 50mA. The unused comparators can be used in conjunction with this circuit as power-on reset or low voltage detectors for a complete LDO solution at a very low installed cost.

4.4 External Hysteresis

Hysteresis can be set externally with two resistors using positive feedback techniques (see Figure 4-3). The design procedure for setting external comparator hysteresis is as follows:

1. Choose the feedback resistor R_C. Since the input bias current of the comparator is at most 100pA, the current through R_C can be set to 100nA (i.e. 1000 times the input bias current) and retain excellent accuracy. The current through R_C at the comparator’s trip point is V_R / R_C where V_R is a stable reference voltage.

FIGURE 4-1: WAKE-UP TIMER



2. Determine the hysteresis voltage (V_{HY}) between the upper and lower thresholds.
3. Calculate R_A as follows:

EQUATION 4-1:

$$R_A = R_C\left(\frac{V_{HY}}{V_{DD}}\right)$$

4. Choose the rising threshold voltage for V_{SRC} (V_{THR}).
5. Calculate R_B as follows:

EQUATION 4-2:

$$R_B = \frac{1}{\left[\left(\frac{V_{THR}}{V_R \times R_A}\right) - \frac{1}{R_A} - \frac{1}{R_C}\right]}$$

6. Verify the threshold voltages with these formulas:

   V_{SRC} rising:

EQUATION 4-3:

$$V_{THR} = (V_R)(R_A)\left[\left(\frac{1}{R_A}\right) + \left(\frac{1}{R_B}\right) + \left(\frac{1}{R_C}\right)\right]$$

   V_{SRC} falling:

EQUATION 4-4:

$$V_{THF} = V_{THR} - \left[\frac{(R_A \times V_{DD})}{R_C}\right]$$

4.5 32.768kHz 'Time Of Day Clock' Crystal Controlled Oscillator

A very stable oscillator driver can be designed by using a crystal resonator as the feedback element. Figure 4-5 shows a typical application circuit using this technique to develop a clock driver for a Time-Of-Day (TOD) clock chip. The value of R_A and R_B determines the DC voltage level at which the comparator trips; in this case one-half of V_{DD}. The RC time constant of R_C and C_A should be set several times greater than the crystal oscillator's period, which will ensure a 50% duty cycle by maintaining a DC voltage at the inverting comparator input equal to the absolute average of the output signal.

4.6 Non-Retriggerable One Shot Multivibrator

Using two comparators, a non-retriggerable, one shot multi-vibrator can be designed using the circuit configuration of Figure 4-6. A key feature of this design is that the pulse width is independent of the magnitude of the supply voltage because the charging voltage and the intercept voltage are a fixed percentage of V_{DD}. In addition, this one shot is capable of pulse width with as much as a 99% duty cycle and exhibits input lockout to ensure that the circuit will not re-trigger before the output pulse has completely timed out. The trigger level is the voltage required at the input to raise the voltage at node A higher than the voltage at node B, and is set by the resistive divider R4 and R10 and the impedance network composed of R1, R2 and R3. When the one shot has been triggered, the output of CMPTR2 is high, causing the reference voltage at the non-inverting input of CMPTR1 to go to V_{DD}. This prevents any additional input pulses from disturbing the circuit until the output pulse has timed out.

The value of the timing capacitor C1 must be small enough to allow CMPTR1 to discharge C1 to a diode voltage before the feedback signal from CMPTR2 (through R10) switches CMPTR1 to its high state and allows C1 to start an exponential charge through R5. Proper circuit action depends upon rapidly discharging C1 through the voltage set by R6, R9 and D2 to a final voltage of a small diode drop. Two propagation delays after the voltage on C1 drops below the level on the non-inverting input of CMPTR2, the output of CMPTR1 switches to the positive rail and begins to charge C1 through R5. The time delay which sets the output pulse width results from C1 charging to the reference voltage set by R6, R9 and D2, plus four comparator propagation delays. When the voltage across C1 charges beyond the reference, the output pulse returns to ground and the input is again ready to accept a trigger signal.

4.7 Oscillators and Pulse Width Modulators

Microchip's linear building block comparators adapt well to oscillator applications for low frequencies (less than 100kHz). Figure 4-7 shows a symmetrical square wave generator using a minimum number of components. The output is set by the RC time constant of R4 and C1, and the total hysteresis of the loop is set by R1, R2 and R3. The maximum frequency of the oscillator is limited only by the large signal propagation delay of the comparator in addition to any capacitive loading at the output which degrades the slew rate.

To analyze this circuit, assume that the output is initially high. For this to occur, the voltage at the inverting input must be less than the voltage at the non-inverting input. Therefore, capacitor C1 is discharged. The voltage at the non-inverting input (V_H) is:

EQUATION 4-5:

$$V_H = \frac{R2(V_{DD})}{[R2 + (R1 \parallel R3)]}$$

where, if R1 = R2 = R3, then:

EQUATION 4-6:

$$V_H = \frac{2(V_{DD})}{3}$$

Capacitor C1 will charge up through R4. When the voltage at the comparator's inverting input is equal to V_H, the comparator output will switch. With the output at ground potential, the value at the non-inverting input terminal (V_L) is reduced by the hysteresis network to a value given by:

EQUATION 4-7:

$$V_L = \frac{V_{DD}}{3}$$

Using the same resistors as before, capacitor C1 must now discharge through R4 toward ground. The output will return to a high state when the voltage across the capacitor has discharged to a value equal to V_L. The period of oscillation will be twice the time it takes for the RC circuit to charge up to one-half its final value. The period can be calculated from:

EQUATION 4-8:

$$\frac{1}{FREQ} = 2(0.694)(R4)(C1)$$

The frequency stability of this circuit should only be a function of the external component tolerances.

Figure 4-8 shows the circuit for a pulse width modulator circuit. It is essentially the same as in Figure 4-7 with the addition of an input control voltage. When the input control voltage is equal to one-half V_{DD}, operation is basically the same as described for the free-running oscillator. If the input control voltage is moved above or below one-half V_{DD}, the duty cycle of the output square wave will be altered. This is because the addition of the control voltage at the input has now altered the trip points. The equations for these trip points are shown in Figure 4-8 (see V_H and V_L).

Pulse width sensitivity to the input voltage variations can be increased by reducing the value of R6 from 10kΩ and conversely, sensitivity will be reduced by increasing the value of R6. The values of R1 and C1 can be varied to produce the desired center frequency.

4.8 Voice Band Receive Filter

The majority of spectral energy for human voices is found to be in a 2.7kHz frequency band from 300Hz to 3kHz. To properly recover a voice signal in applications such as radios, cellular phones, and voice pagers, a low power bandpass filter that is matched to the human voice spectrum can be implemented using MIcrochip's CMOS op amps. Figure 4-9 shows a unity gain multi-pole Butterworth filter with ripple less than 0.15dB in the human voice band. The lower 3dB cut-off frequency is 70Hz (single order response), while the upper cut-off frequency is 3.5kHz (fourth order response).

4.9 Supervisory Audio Tone (SAT) Filter for Cellular

Supervisory Audio Tones (SAT) provide a reliable transmission path between cellular subscriber units and base stations. The SAT tone functions much like the current/voltage used in land line telephone systems to indicate that a phone is off the hook. The SAT tone may be one of three frequencies: 5970, 6000 or 6030Hz. A loss of SAT implies that channel conditions are impaired and if SAT is interrupted for more than 5 seconds a cellular call is terminated.

Figure 4-10 shows a high Q (30) second order SAT detection bandpass filter using Microchip's CMOS op amp architecture. This circuit nulls all frequencies except the three SAT tones of interest.

FIGURE 4-2: PRECISION BATTERY MONITOR

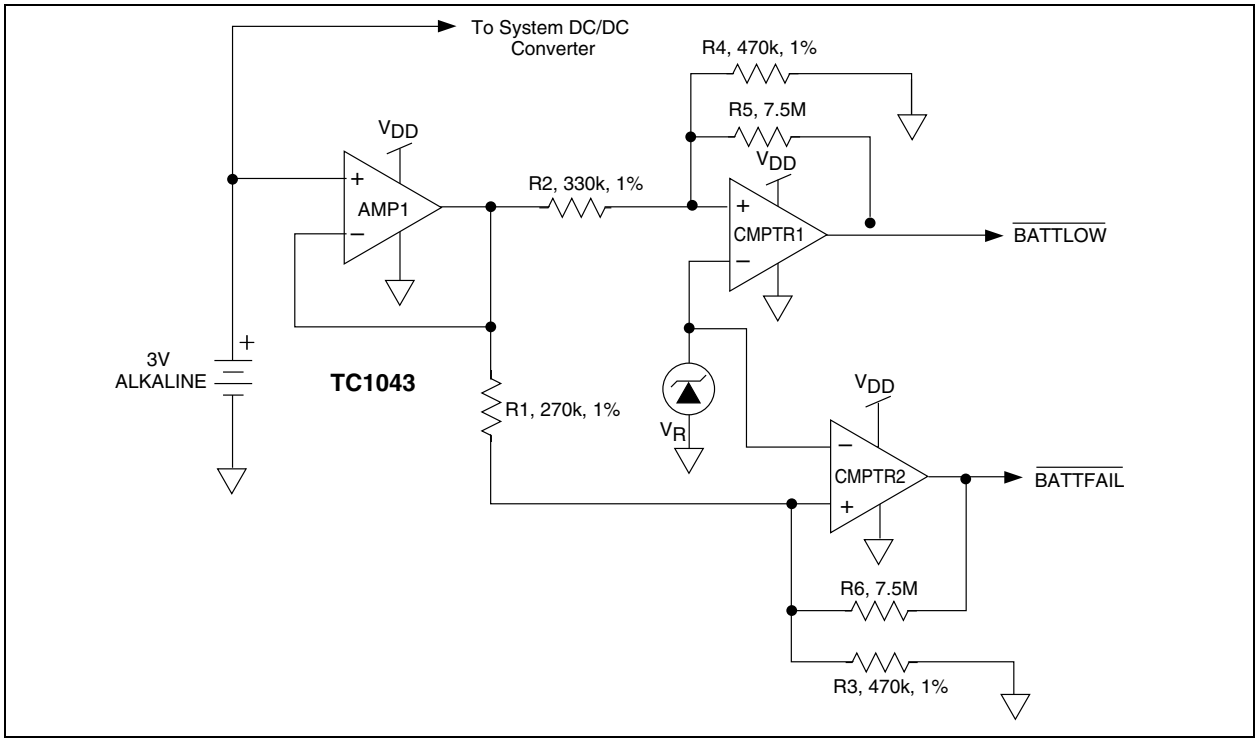


FIGURE 4-3: DUAL LOW DROPOUT REGULATOR

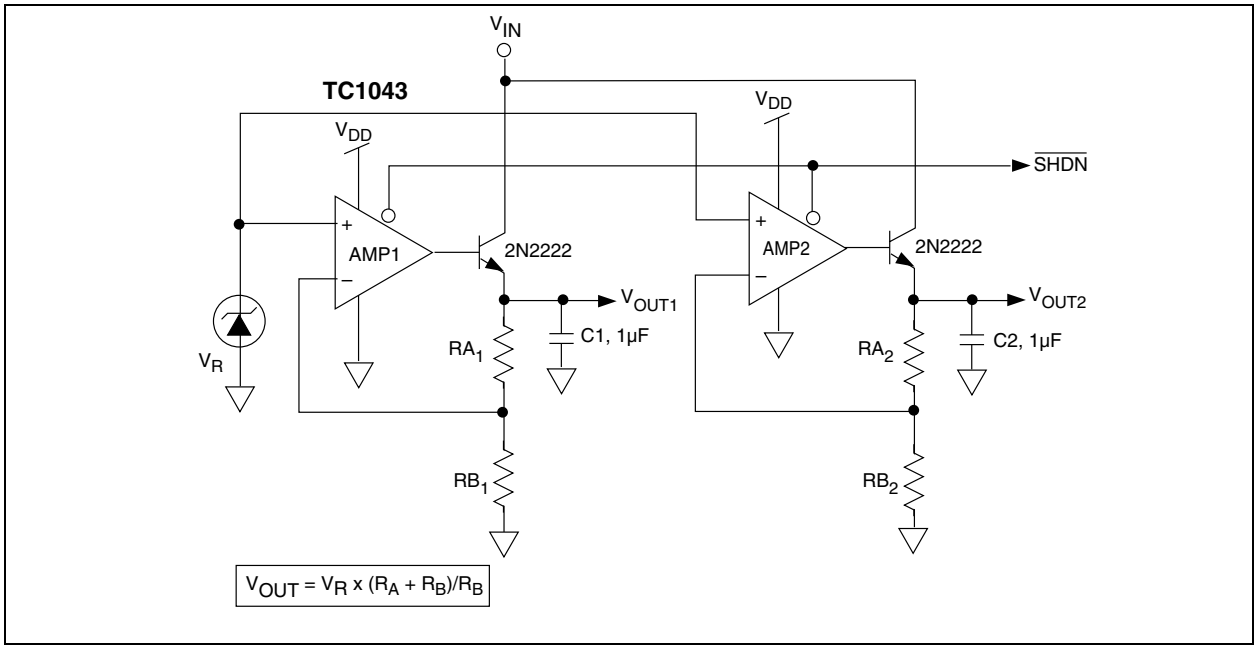


FIGURE 4-4: COMPARATOR EXTERNAL HYSTERESIS CONFIGURATION

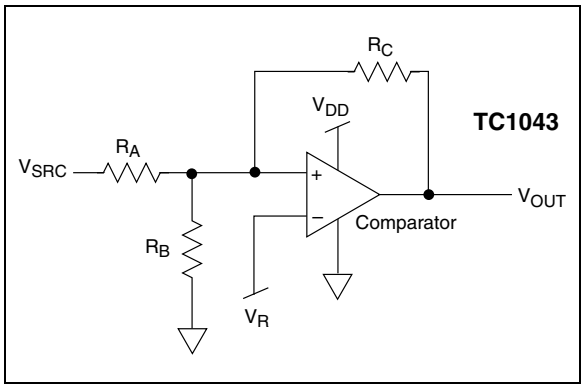


FIGURE 4-5: 32.768 KHZ "TIME-OF-DAY" CLOCK OSCILLATOR

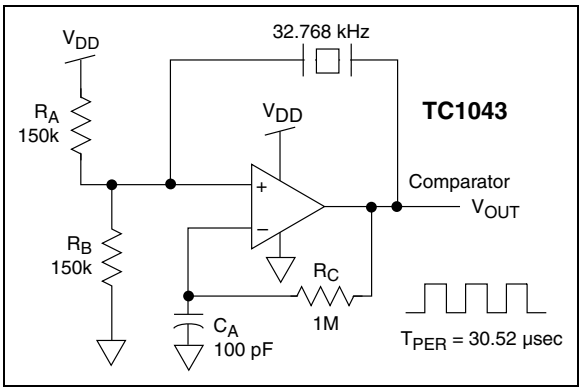


FIGURE 4-6: NON-RETRIGGERABLE MULTI-VIBRATOR

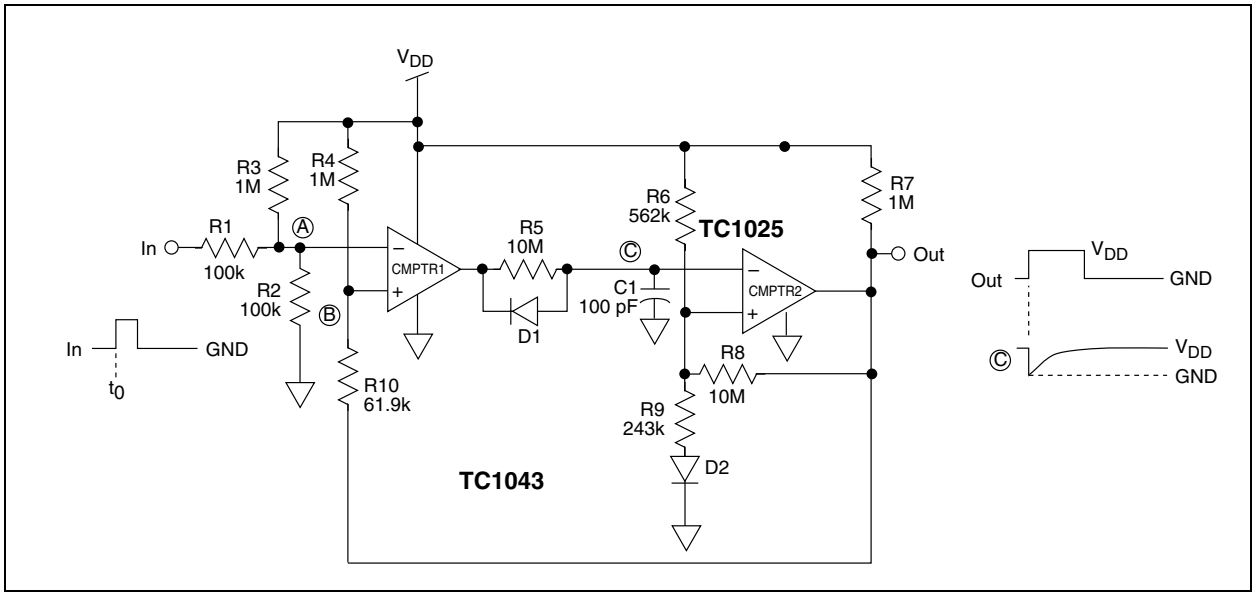


FIGURE 4-7: SQUARE WAVE GENERATOR

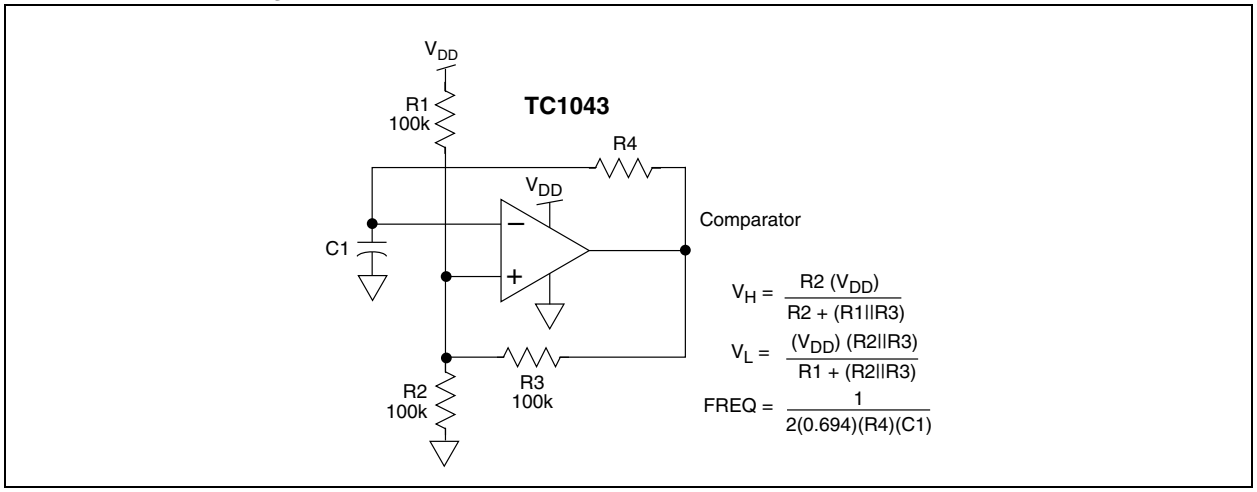
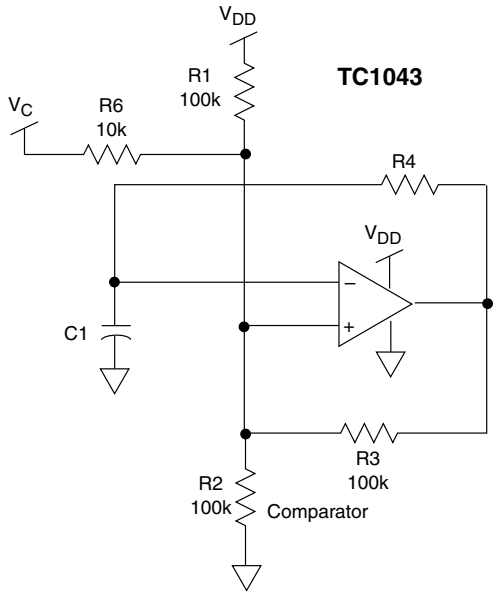


FIGURE 4-8: PULSE WIDTH MODULATOR



$$V_H = \frac{V_{DD}(R_1R_2R_6 + R_2R_3R_6) + V_C(R_1R_2R_3)}{R_1R_2R_6 + R_1R_3R_6 + R_2R_3R_6 + R_1R_2R_3}$$

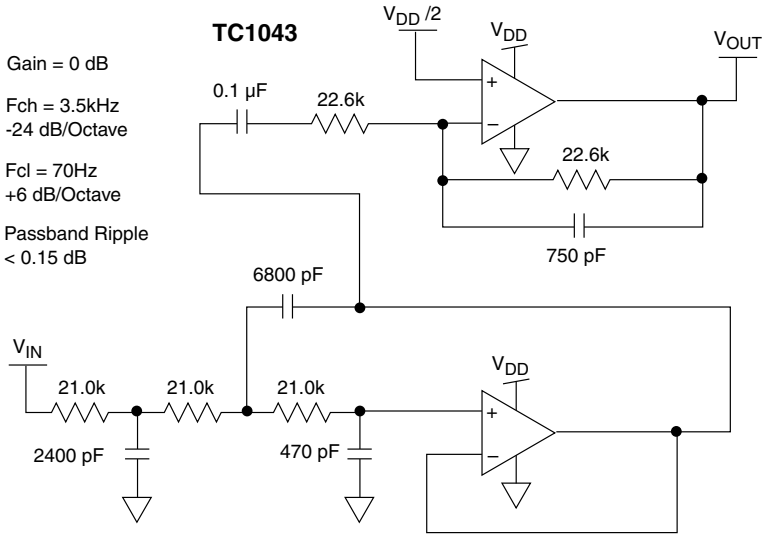
$$V_L = \frac{V_{DD}(R_2R_3R_6) + V_C(R_1R_2R_3)}{R_1R_2R_6 + R_1R_3R_6 + R_2R_3R_6 + R_1R_2R_3}$$

$$FREQ = \frac{1}{2\,(0.694)\,(R4)\,(C1)}$$

For Square Wave Generation,
Select R1 = R2 = R3

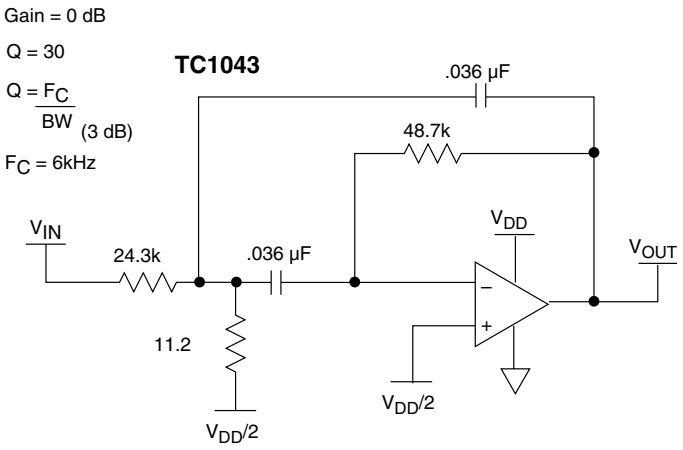
$$V_C = \frac{V_{DD}}{2}$$

FIGURE 4-9: MULTI-POLE BUTTERWORTH VOICE BAND RECEIVE FILTER



Two (2) **TC1043** Op Amps

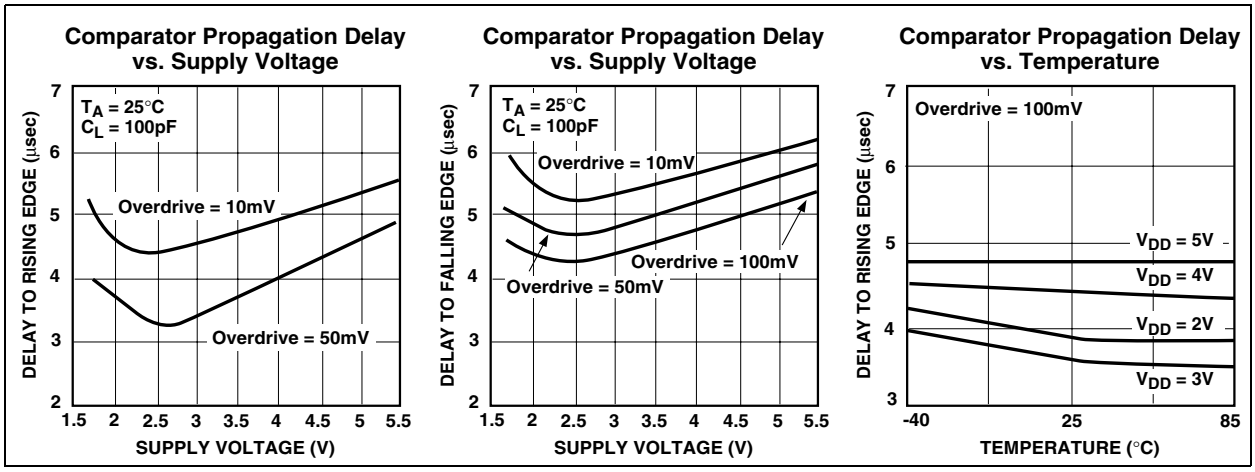
FIGURE 4-10: SECOND ORDER SAT BANDPASS FILTER

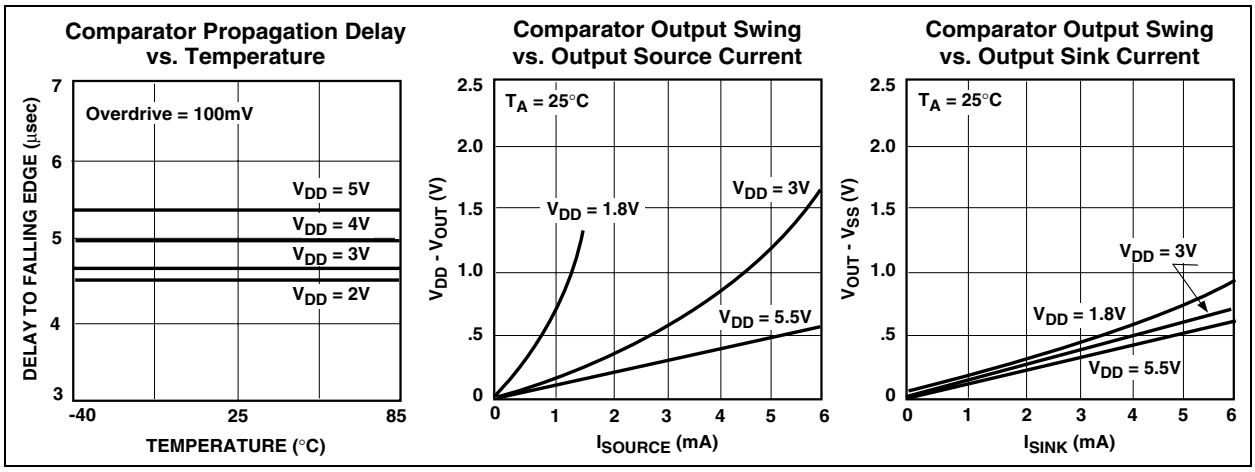


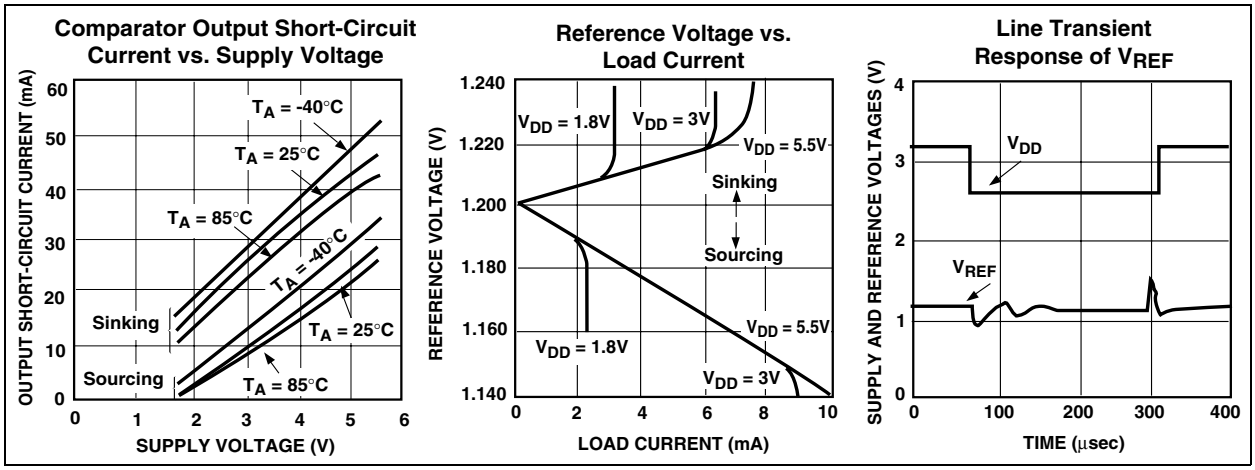
TC1043 Op Amp

5.0 TYPICAL CHARACTERISTICS

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

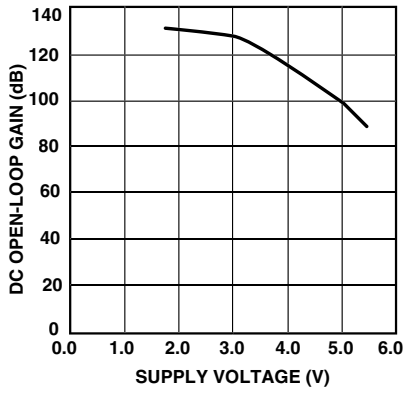




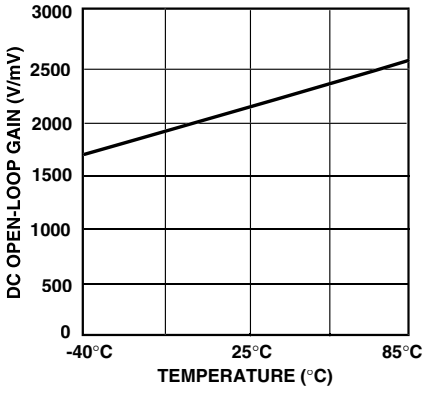


TYPICAL CHARACTERISTICS (CONTINUED)

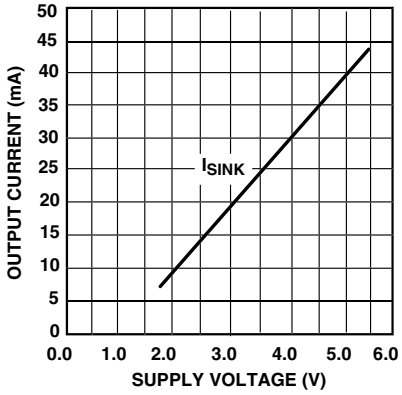
Op-Amp DC Open-Loop Gain vs. Supply Voltage



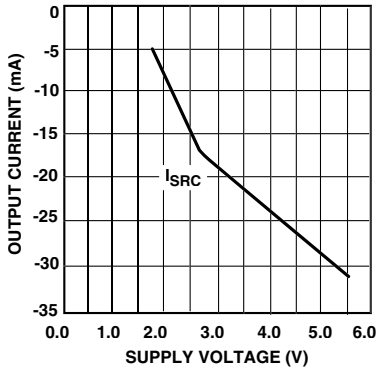
Op-Amp DC Open-Loop Gain vs. Temperature



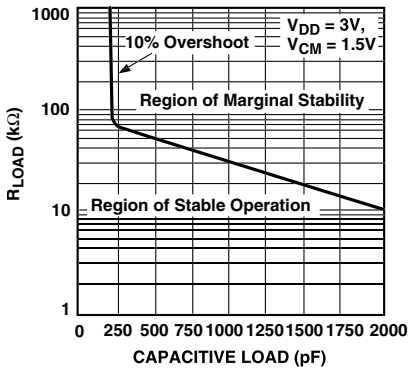
Op-Amp Short-Circuit Current vs. Supply Voltage



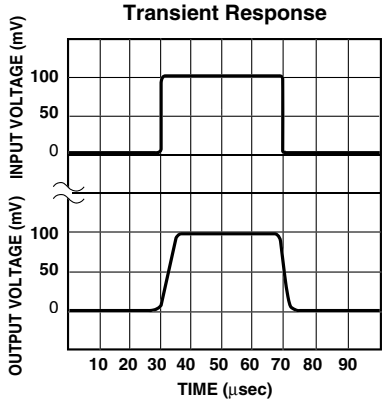
Op-Amp Short-Circuit Current vs. Supply Voltage



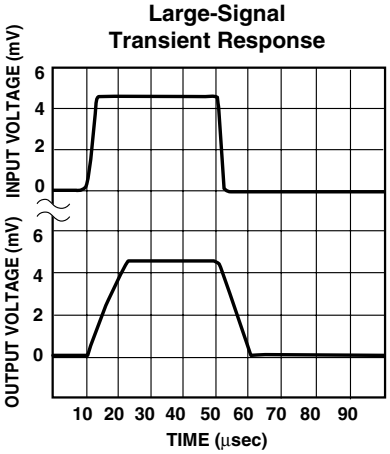
Op-Amp Load Resistance vs. Load Capacitance



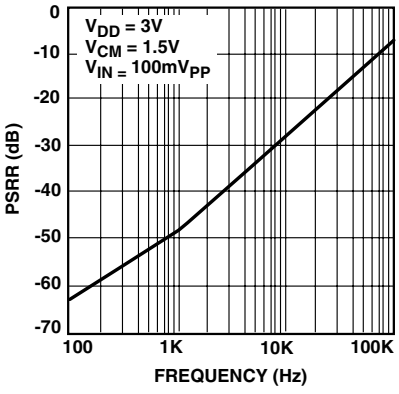
Op-Amp Small-Signal Transient Response



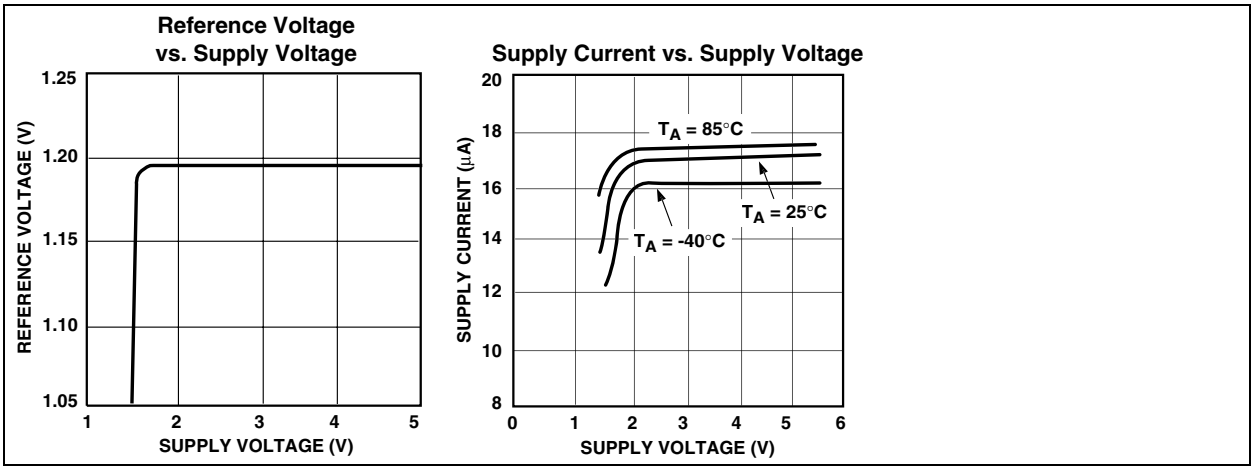
Large-Signal Transient Response



Op-Amp Power Supply Rejection Ratio (PSRR) vs. Frequency



TYPICAL CHARACTERISTICS (CONTINUED)



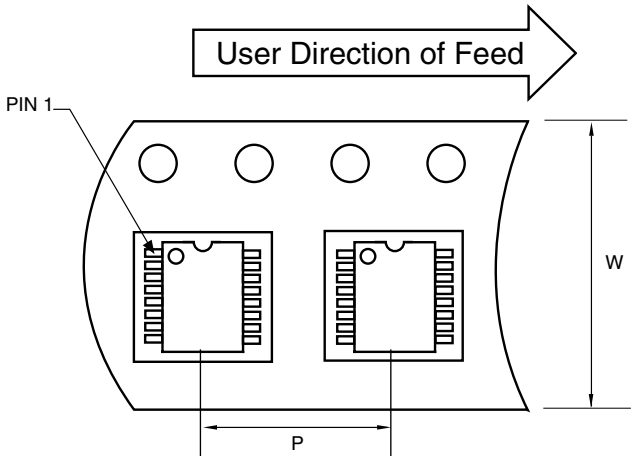
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

Package marking information not available at this time.

6.2 Taping Information

Component Taping Orientation for 16-Pin QSOP (Narrow) Devices



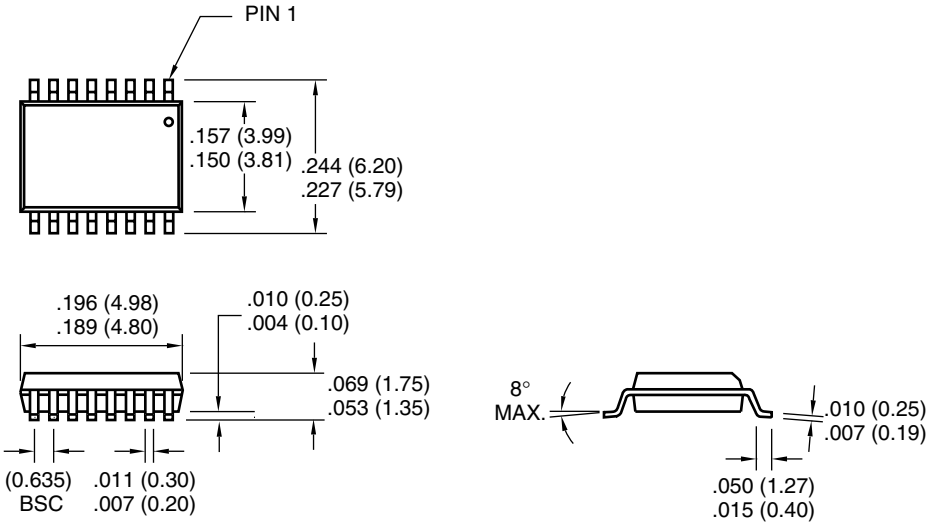
Standard Reel Component Orientation
for TR Suffix Device

Carrier Tape, Reel Size, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
16-Pin QSOP (N)	12 mm	8 mm	2500	13 in

6.3 Package Dimensions

16-Pin QSOP (Narrow)



Dimensions: inches (mm)

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Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
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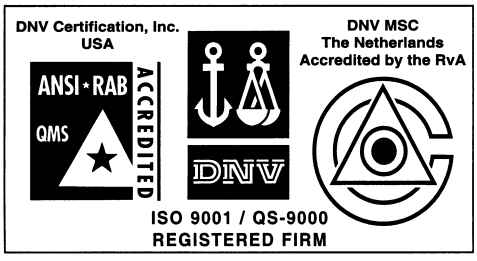
NOTES:



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