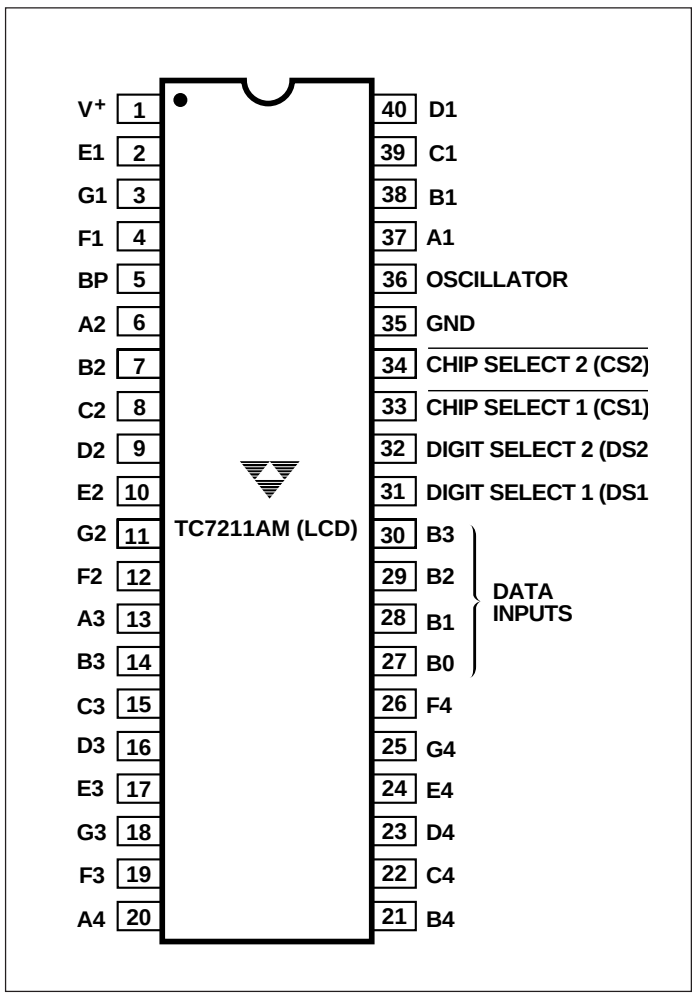
BUS COMPATIBLE 4-DIGIT CMOS DECODER/DRIVER

FEATURES

- **4-Digit Non-Multiplexed 7-Segment LCD Outputs With Backplane Driver**
- **Input and Digit Select Data Latches**
- **RC Oscillator On-Chip Generates Backplane Drive Signal**
- **Eliminates DC Bias Which Degrades LCD Life**
- **Backplane Input/Output Pin Permits Synchronization of Cascaded Slave Device to a Master Backplane Signal**
- **Binary and BCD Inputs Decoded to Code B (0 to 9, —, E, H, L, P, Blank)**
- **Pin Compatible and Functionally Equivalent to ICM7211AM**

PIN CONFIGURATIONS



GENERAL DESCRIPTION

The TC7211AM (LCD Decoder/driver) is a CMOS direct drive, 4-digit, 7-segment display decoder and driver.

The TC7211AM drives conventional LCDs. An RC oscillator, divider chain, backplane driver, and 28-segment outputs are provided on a single CMOS chip. The segment drivers supply square waves of the same frequency as the backplane, but in-phase for an OFF segment and out-of-phase for an ON segment. The net DC voltage applied between driver segment and backplane is near zero maximizing display lifetime.

The four bit binary input is decoded into the seven segment alphanumeric code known as "Code B". The "Code B" output format results in a 0 to 9,—, E, H, L, P or blank display. True BCD or binary inputs will be correctly decoded to the seven segment display format.

ORDERING INFORMATION

Part No.	Driver Type	Package	Input Code	Output Config.
TC7211AMIPL	LCD	40-Pin Plastic DIP	Code B	Data and Digit Select Latches

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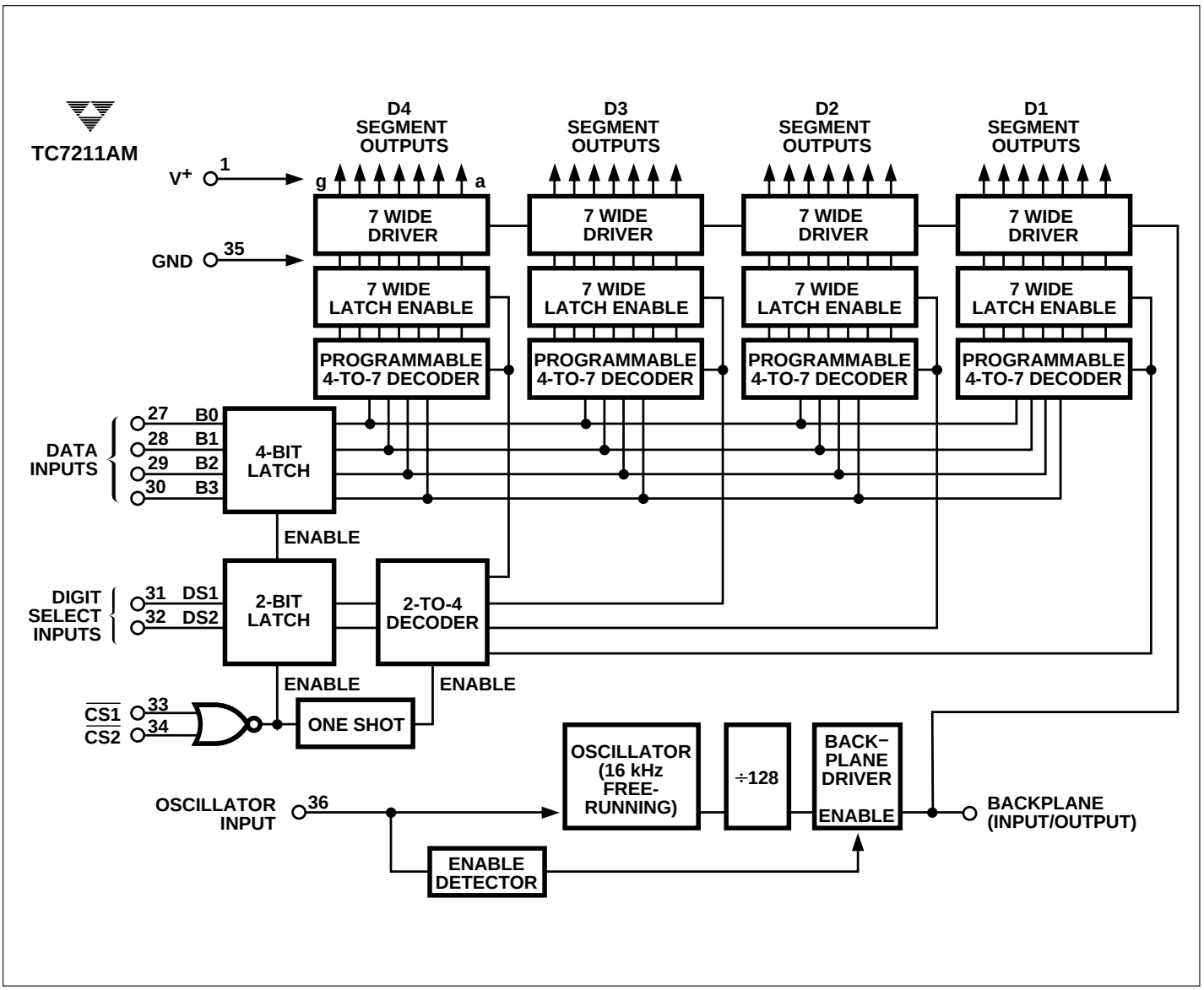
FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Supply Voltage ..... +6.5V
Input Voltage, Any Terminal
(Note 2) ..... V^+ +0.3V, GND –0.3V
Power Dissipation $T_A \leq 70°C$ (Note 1) 1.23W
Operating Temperature Range ..... –20°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTES: 1. This limit refers to that of the package and will not be realized during normal operation.
2. Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V^+ or less than GND may cause destructive latch-up. For this reason, it is recommended that inputs from external sources not operating on the same power supply not be applied to the device before its supply is established, and, in multiple supply systems, the supply to the TC7211AM be turned on first.

TYPICAL CHARACTERISTICS: All parameters measured with V+ = 5V, $T_A = 25°C$

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{SUP}	Operating Voltage Range		3	5	6	V
I_{OP}	Operating Current	Display Blank	—	10	50	µA
I_{OSCI}	Oscillator Input Current	Pin 36	—	±2	±10	µA
t_{RFS}	Segment Rise/Fall Time	C_L = 200 pF	—	0.5	—	µsec
t_{RFB}	Backplane Rise/Fall Time	C_L = 5000 pF	—	1.5	—	µsec
f_{OSC}	Oscillator Frequency	Pin 36 Floating	—	16	—	kHz
f_{BP}	Backplane Frequency	Pin 36 Floating	—	125	—	Hz
Input Characteristics						
V_{IH}	Logic “1” High Input Voltage		3	—	—	V
V_{IL}	Logic “0” Low Input Voltage		—	—	1	V
I_{ILK}	Input Leakage Current	Pins 27–34	—	±0.01	±1	µA
C_{IN}	Input Capacitance	Pins 27–34	—	5	—	pF
I_{BPLK}	BP Input Current Leakage	Measured at Pin 5 With Pin 36 at GND	—	±0.01	±1	µA
C_{BPI}	BP Input Capacitance	All Devices	—	200	—	pF

AC Characteristics						
Symbol	**Parameter**	**Test Conditions**				
t_{CSA}	Chip Select Active Pulse Width	(Note 1)	200	—	—	nsec
t_{DS}	Data Setup Time		100	—	—	nsec
t_{DH}	Data Hold Time		10	0	—	nsec
t_{ICS}	Inter-Chip Select Time		2	—	—	µsec

NOTE: 1. Other chip select (CS) is either held at logic zero or both CS1 and CS2 driven together.

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TIMING DIAGRAMS

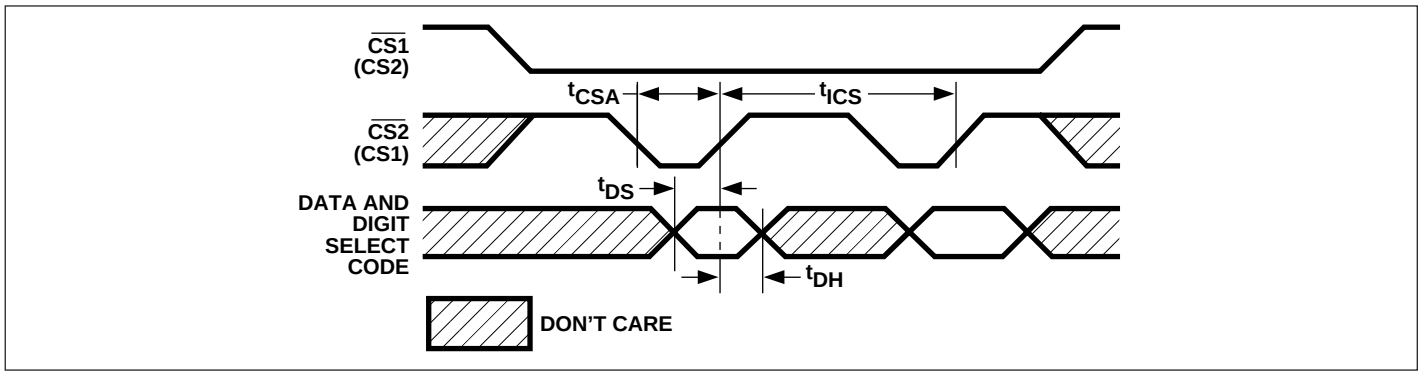


Figure 1: BUS Interface Timing Diagram

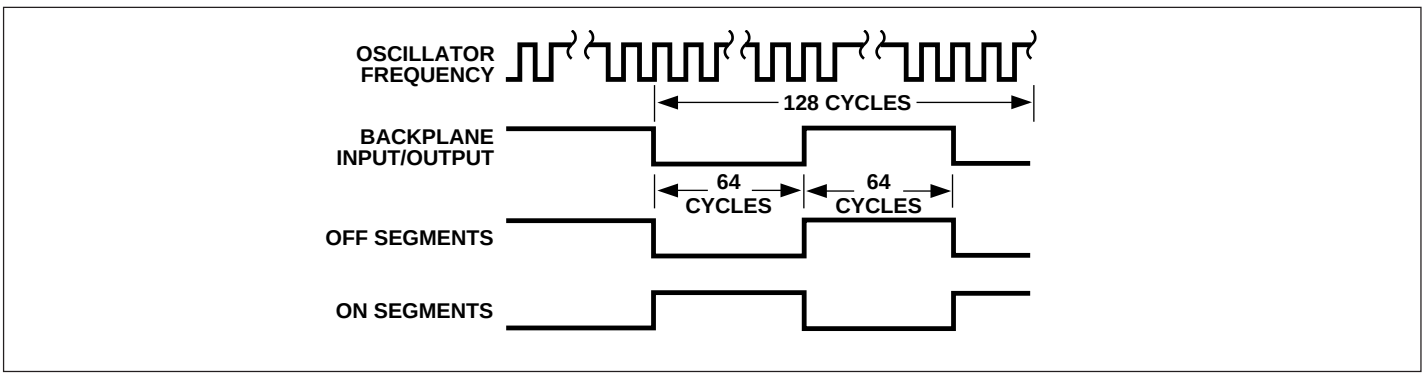


Figure 2: LCD Display Waveforms

INPUT DEFINITIONS

In this table, V^+ and GND are considered to be normal operating input logic levels. For lowest power consumption, input signals should swing over the full supply.

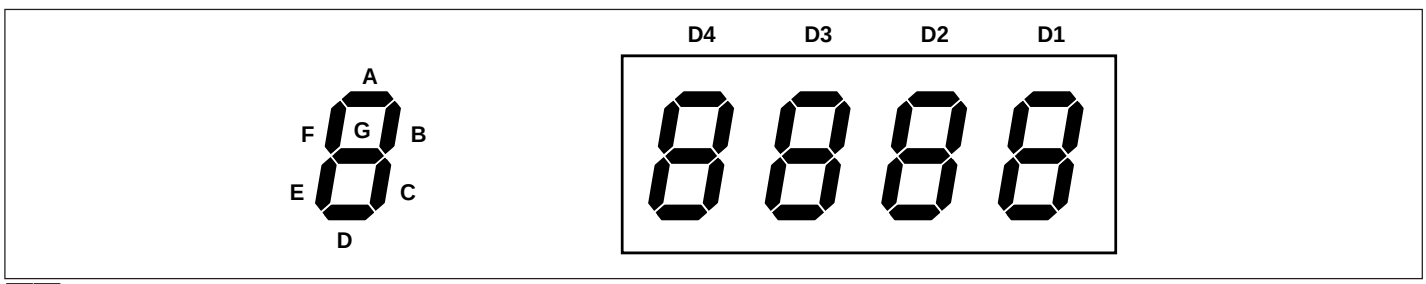
Input	Pin No.	Condition	Function	
B0	27	V^+ = Logic "1" GND = Logic "0"	Ones (Least Significant)	Data Input Bits
B1	28	V^+ = Logic "1" GND = Logic "0"	Twos	
B2	29	V^+ = Logic "1" GND = Logic "0"	Fours	
B3	30	V^+ = Logic "1" GND = Logic "0"	Eights (Most Significant)	
OSC	36	Floating or with external capacitor GND	Oscillator input. Disables BP output devices, allowing segments to be synchronized to an external signal input at the BP terminal (pin 5)	
$\overline{DS1}$	31	V^+ = Logical One	DS2, DS1 = 00 Selects D4 DS2, DS1 = 01 Selects D3 DS2, DS1 = 10 Selects D2 DS2, DS1 = 11 Selects D1	Digit Select Inputs
DS2	32	GND = Logical Zero		
$\overline{CS1}$	33	V^+ = Inactive	When both $\overline{CS1}$ and $\overline{CS2}$ are LOW, the data and digit select input latches are open or enabled. On the rising of $\overline{CS1}$ or $\overline{CS2}$, data is latched, decoded and stored in the output drive latches.	
CS2	34	GND = Active		

OUTPUT DEFINITIONS

Output pins are defined by the alphabetical segment assignment and numerical digital assignment.

Output	Pin No.		Function			Output	Pin No.		Function		
A1	37	A	Segment Drive	Digit 1	(LSD)	A3	13	A	Segment Drive	Digit 3	
B1	38	B	↓	↓	↓	B3	14	B	↓	↓	
C1	39	C				C3	15	C			
D1	40	D				D3	16	D			
E1	2	E				E3	17	E			
F1	4	F				F3	19	F			
G1	3	G	↓	↓	↓	G3	18	G	↓	↓	
A2	6	A	Segment Drive	Digit 2		A4	20	A	Segment Drive	Digit 4	(MSD)
B2	7	B	↓	↓		B4	21	B	↓	↓	↓
C2	8	C				C4	22	C			
D2	9	D				D4	23	D			
E2	10	E				E4	24	E			
F2	12	F				F4	26	F			
G2	11	G	↓	↓		G4	25	G	↓	↓	↓

DIGIT ASSIGNMENT



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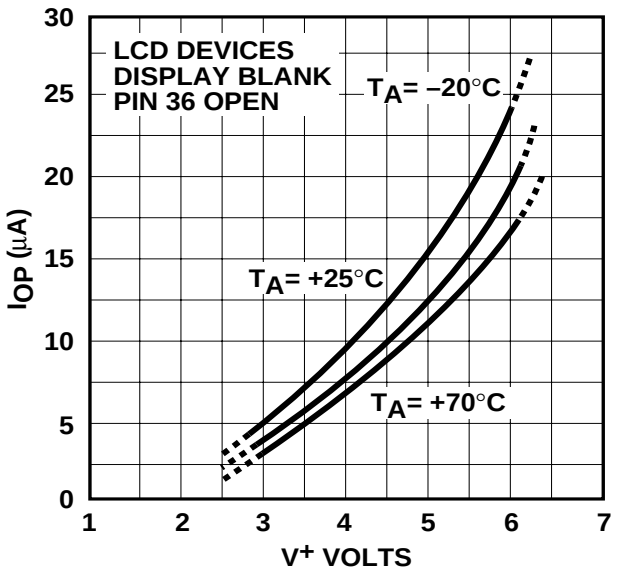
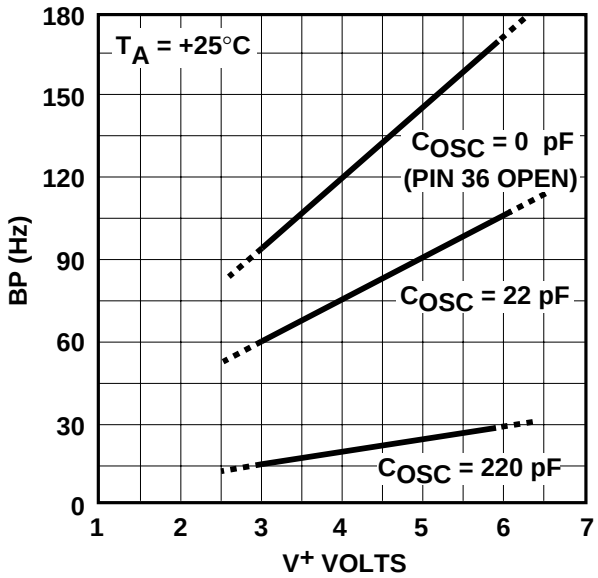
TYPICAL CHARACTERISTICS

Operating Supply Current vs Supply Voltage



Backplane Frequency vs Supply Voltage



BASIC OPERATION

The TC7211AM drives 4-digit, 7-segment LCDs. This device contains 28 individual segment drivers, a backplane driver, a self-contained oscillator, and a divider chain to generate the backplane signal.

The 28 CMOS segment drivers and backplane driver contain ratioed N- and P-channel transistors for identical ON resistance. The equal resistances eliminate the DC output driver component resulting from unequal rise and fall times. This ensures maximum LCD life.

The backplane output driver can be disabled by grounding the OSCILLATOR input (pin 36). The 28 output segment drivers can therefore be synchronized directly to an input signal at the backplane (BP) terminal (pin 5). Several slave devices may be cascaded to the backplane output of a master device. The backplane signal may also be derived from an external source. These features permit interfacing to single backplane LCDs with characters in multiples of four.

Each slave's backplane input represents a 200pF capacitive load to the master backplane driver (comparable to one additional segment). The number of slave devices drivable by a master device is therefore set by the larger display backplane capacitive load. The master backplane output will drive the display backplane of 16 one-half-inch characters with rise and fall times under 5 µsec. This represents a system with three slave devices and a fourth master device driving the backplane.

If more than four devices are slaved together, the backplane signal should be derived externally and all TC7211AM devices slaved to it. The external drive signal must drive a high capacitive load with 1µsec to 2 µsec rise and fall times. The backplane frequency is normally 125 Hz. At lower display ambient temperatures, the frequency may be reduced to compensate for display response time.

The on-chip RC oscillator free-runs at approximately 16 kHz. A divide-by 128 circuit provides the 125 Hz backplane frequency. The oscillator frequency may be reduced by connecting an external capacitor between the oscillator terminal and V^+. (See typical operating characteristics curves.)

The free-running oscillator may be overridden (if desired) by an external clock. The backplane driver, however, must not be disabled during the external clock's negative or lOW portion, as this will result in a DC drive component being applied to the LCD, limiting the LCD's life. To prevent backplane driver disabling, the oscillator input should be driven from the positive supply to no less than one-fifth the supply voltage above ground. A backplane disable signal will not be sensed if the driving signal remains above ground by one-fifth the supply voltage. An alternate method for externally driving the oscillator permits the oscillator input to swing the full supply voltage range. The oscillator input signal duty cycle is skewed so the LOW

portion duration is less than 1 µsec. The backplane disable sensing circuit will not respond to such a short signal.

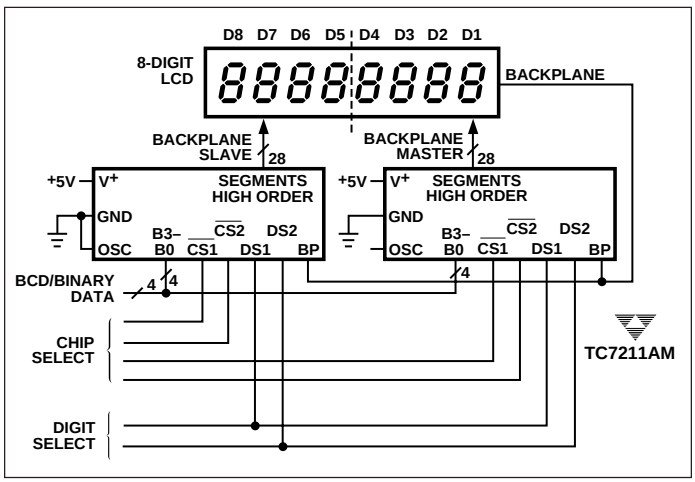


Figure 3. TC7211AM Driving an 8-Digit LCD Display in Master/Slave Configuration

Input Configuration and Output Codes

The TC7211AM accepts a 4-bit, true binary (positive level = logic "1") input at pin 27 (LSB) through pin 30 (MSB). The binary input is decoded to the 7-segment output known as Code B. The output display format is 0 to 9, —, E, H, L, P and blank display (see Table 1). Segment assignments are shown in Figure 4. The TC7211AM will correctly decode binary and BCD true codes to a 7-segment output.

The TC7211AM is designed to interface with a data bus and display data under microprocessor control. Four data inputs (pins 27–30) and two digit select input bits (pins 31 and 32) are written into input buffer latches. The rising edge of either chip select causes data to be latched, decoded and stored in the selected digit output data latch. The 2-bit digit code selects the appropriate output digit latch. The 4-bit display data word is decoded to the "Code B" 7-segment output format.

For applications where bus compatibility is not required, refer to the TC7211AM (LCD) 4-digit decoder driver data sheet. This device is designed to accept multiplexed BCD/binary input data for display under the control of four separate digit select control signals.

Table 1. Binary Codes Versus Character Displayed

Binary Input				Character Displayed
B3	B2	B1	B0	(Code B)
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	—
1	0	1	1	E
1	1	0	0	H
1	1	0	1	L
1	1	1	0	P
1	1	1	1	Blank

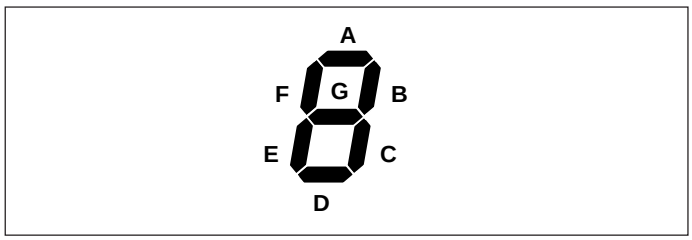


Figure 4. Segment Assignment

Special Order Decoder Option

The TC7211AM is mask programmed to give the 16 combinations of 7-segment output codes. For large volume orders (50K pieces minimum), custom decoder options are available. Contact TelCom Semiconductor for details.

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