DATA SHEET

TDA5147K

12 V Voice Coil Motor (VCM) driver and spindle motor drive combination chip

Product specification
File under Integrated Circuits, IC11

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Philips
Semiconductors

PHILIPS

12 V Voice Coil Motor (VCM) driver and spindle motor drive combination chip

TDA5147K

FEATURES

Spindle motor driver

- Internal 1 A peak current power drivers
- Low $R_{ds(on)}$ 1 Ω max total for high, low and isolation drivers
- Induction sense start-up option
- External current sense resistor
- Soft switching on both upper and lower drivers
- Programmable linear or PWM spindle mode
- Provide spindle active dynamic braking mode.

Voice coil motor driver

- 0.8 Amp VCM power driver
- Maximum of 1 V drop across the power driver at 0.8 A
- External current sense resistor, with sense amplifier
- External current control loop compensation
- 15 kHz (typ.) VCM current control loop bandwidth
- Three mode operation: enable VCM, retract, and disable.

Power monitor and retract circuit

- +5 and +12 V power monitor threshold accuracy ±2%
- Hysteresis on both power monitor comparators
- Precision internal voltage generator ±2%
- Buffered reference voltage output pin
- Retract circuit operates down to 2 V
- Internal thermal sense circuitry with an over temperature shut down option
- Internal boost voltage generator
- Sleep mode.

APPLICATIONS

- Hard disk drive for PC products.

GENERAL DESCRIPTION

The TDA5147K is an ASIC combination chip that includes the following functions; spindle motor drive, voice coil motor drive, retract, and power-on. The circuit is contained in a 52-pin PLCC package.

The TDA5147K (see Fig.1) is controlled by a custom digital ASIC. The custom ASIC provides the necessary commutation sequences for the spindle drivers via the SCNTL1, SCNTL2 and SCNTL3 inputs. Spindle speed is monitored by comparator outputs SENU, SENV and SENWIS. Motor speed control is accomplished by a PWM signal (input at the SIPWM pin).

Control of the VCM circuits is via the V_{IPWMH} and V_{IPWML} input signals. These two inputs provide control of the coil current. The $V_{ISENSE2}$ output signal can be used to monitor the voice coil current.

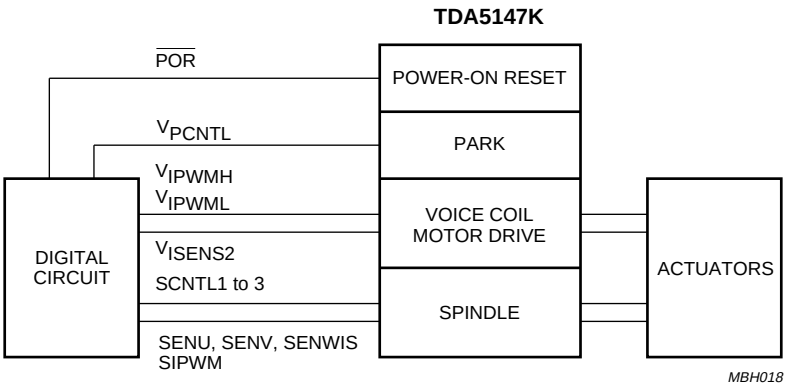
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Supply voltage					
V_{CCA1}	analog supply voltage 1	4.5	5.0	5.5	V
V_{CCA2}	analog supply voltage 2	10.8	12.0	13.2	V
Drivers					
$I_{spin(max)}$	maximum spindle current	–	1	–	A
$I_{VCM(max)}$	maximum voice coil motor current	–	0.8	–	A

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA5147K	PLCC52	plastic leaded chip carrier; 52 leads	SOT238-2

BLOCK DIAGRAMS



Overview

No external power drivers; dynamic braking for non-power down situations; 1 A spindle current; 0.8 A VCM power driver; full-wave spindle mode, $\overline{POR}$ monitors for both 5 and 12 V supplies; auto-park in the event of power-down.

Fig.1 System block diagram.

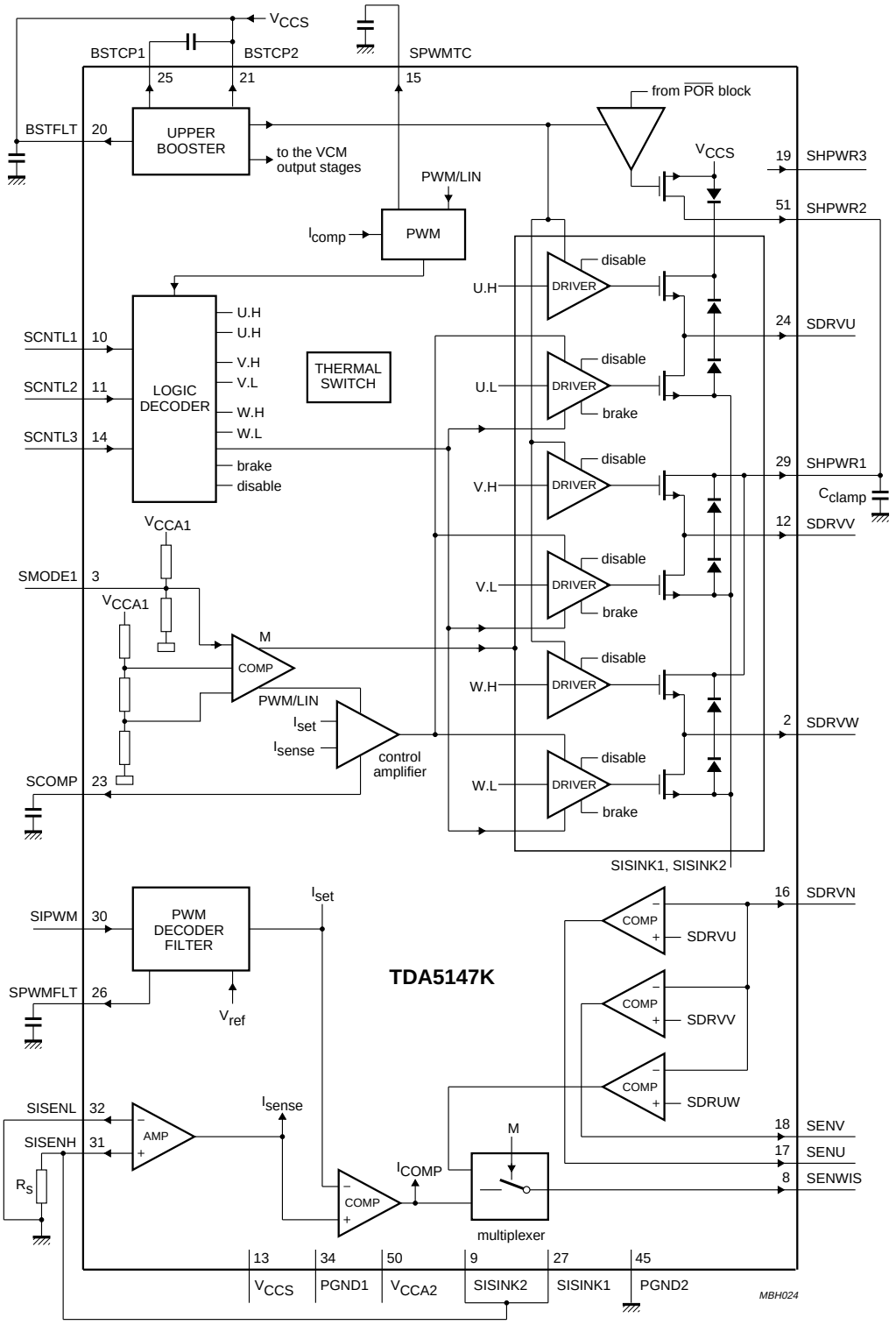


Fig.2 Block diagram of spindle motor drivers.

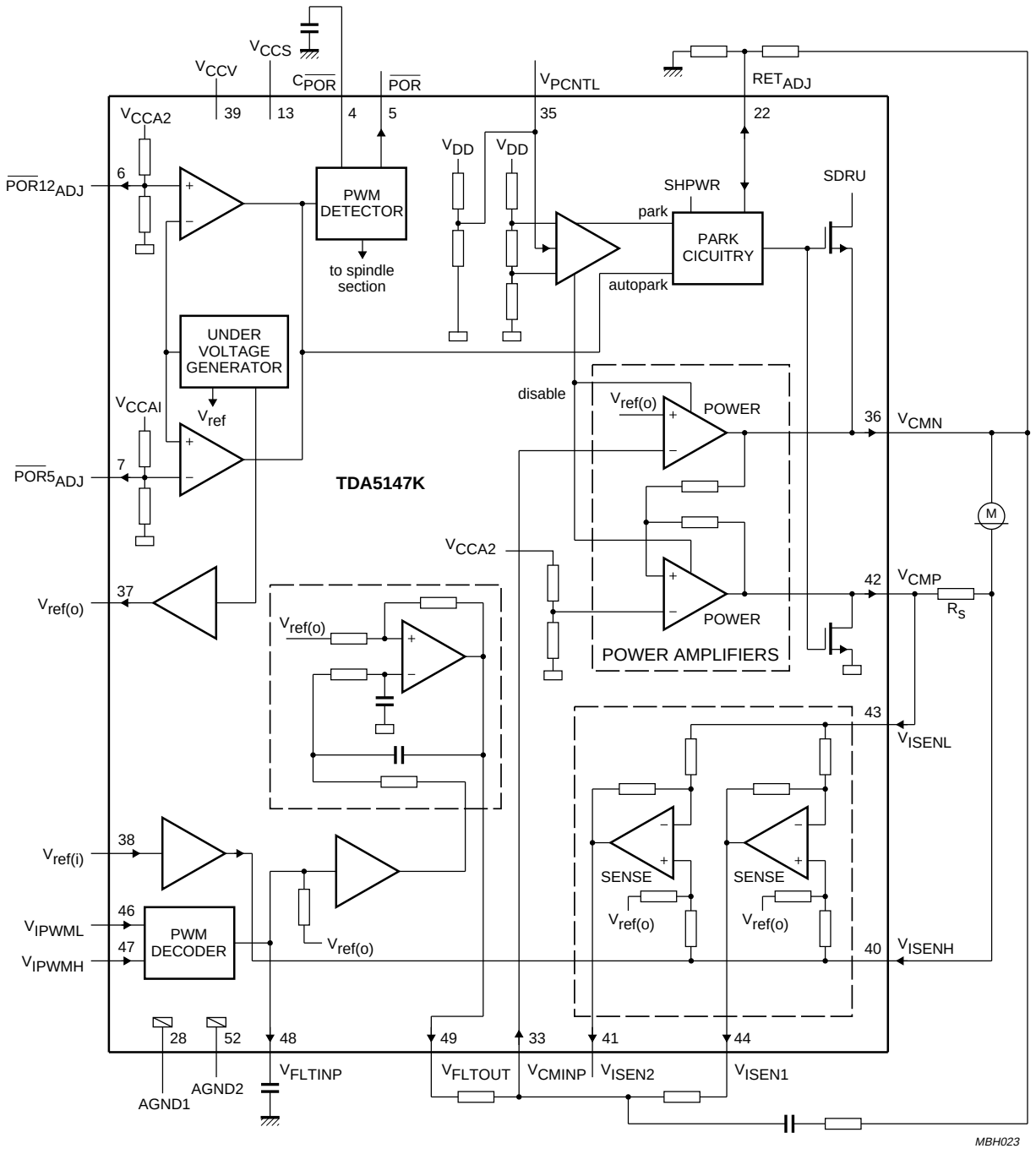


Fig.3 Block diagram of voice coil motor driver.

PINNING

SYMBOL	PIN	I/O	DESCRIPTION
V_{CCA1}	1	–	analog supply voltage 1 (+5 V)
SDRVW	2	O	phase 3 output for spindle motor
SMODE1	3	I	3-state level input for spindle mode
$C_{\overline{POR}}$	4	I/O	power-on reset delay capacitor
$\overline{POR}$	5	O	power-on reset digital output (active LOW)
$\overline{POR}12_{ADJ}$	6	O	adjustment of $\overline{POR}$ threshold (for +12 V)
$\overline{POR}5_{ADJ}$	7	O	adjustment of $\overline{POR}$ threshold (for +5 V)
SENWIS	8	O	digital output of back EMF sense 3/inductive sense
SISINK2	9	–	connection 2 to the sense resistor
SCNTL1	10	I	digital input 1 for spindle decoder
SCNTL2	11	I	digital input 2 for spindle decoder
SDRVV	12	O	phase 2 output for spindle motor
V_{CCS}	13	–	power supply of spindle motor drivers (+12 V)
SCNTL3	14	I	digital input 3 for spindle decoder
SPWMTC	15	O	capacitor for spindle low side PWM time off
SDRVN	16	O	centre TAP connection to spindle motor
SENU	17	O	digital output of back EMF sense 1
SENV	18	O	digital output of back EMF sense 2
SHPWR3	19	O	capacitor 3 for PARK supply voltage
BSTFLT	20	O	booster filter output
BSTCP2	21	O	booster capacitor 2 output
RET_{ADJ}	22	I/O	retract voltage adjustment pin
SCOMP	23	O	control amplifier pole adjustment
SDRVU	24	O	phase 1 output for spindle motor
BSTCP1	25	O	booster capacitor 1 output
SPWMFLT	26	O	capacitor for spindle PWM filter
SISINK1	27	–	connection 1 to the sense resistor
AGND1	28	–	analog ground 1
SHPWR1	29	O	capacitor 1 for PARK supply voltage
SIPWM	30	I	digital PWM input for spindle current
SISENH	31	O	sense resistor for spindle current
SISENL	32	O	isolated ground connection for spindle sense amplifier
V_{CMINP}	33	I	closed loop voltage compensation of VCM
PGND1	34	–	power ground of VCM driver
V_{PCNTL}	35	I	PARK enable 3-state voltage level input
V_{CMN}	36	O	negative output voltage of H-bridge
$V_{ref(o)}$	37	O	reference voltage output for external ADC
$V_{ref(i)}$	38	I	reference voltage input for the 2nd sense amplifier
V_{CCV}	39	–	power supply of VCM driver (+12 V)
V_{ISENH}	40	I	positive input voltage of sense resistor amplifier

SYMBOL	PIN	I/O	DESCRIPTION
V_{ISENS2}	41	O	voltage output 2 of sense resistor amplifier
V_{CMP}	42	O	positive output voltage of H-bridge
V_{ISENL}	43	I	negative input voltage of sense resistor amplifier
V_{ISENS1}	44	O	voltage output 1 of sense resistor amplifier
PGND2	45	–	power ground 2 of voice coil motor driver
V_{IPWML}	46	I	PWM input voltage (LSB)
V_{IPWMH}	47	I	PWM input voltage (MSB)
V_{FLTINP}	48	O	voice coil motor PWM filter capacitor
V_{FLTOUT}	49	O	PWM filter output voltage
V_{CCA2}	50	–	analog supply voltage 2 (+12 V)
SHPWR2	51	O	capacitor for PARK supply voltage
AGND2	52	–	analog ground 2

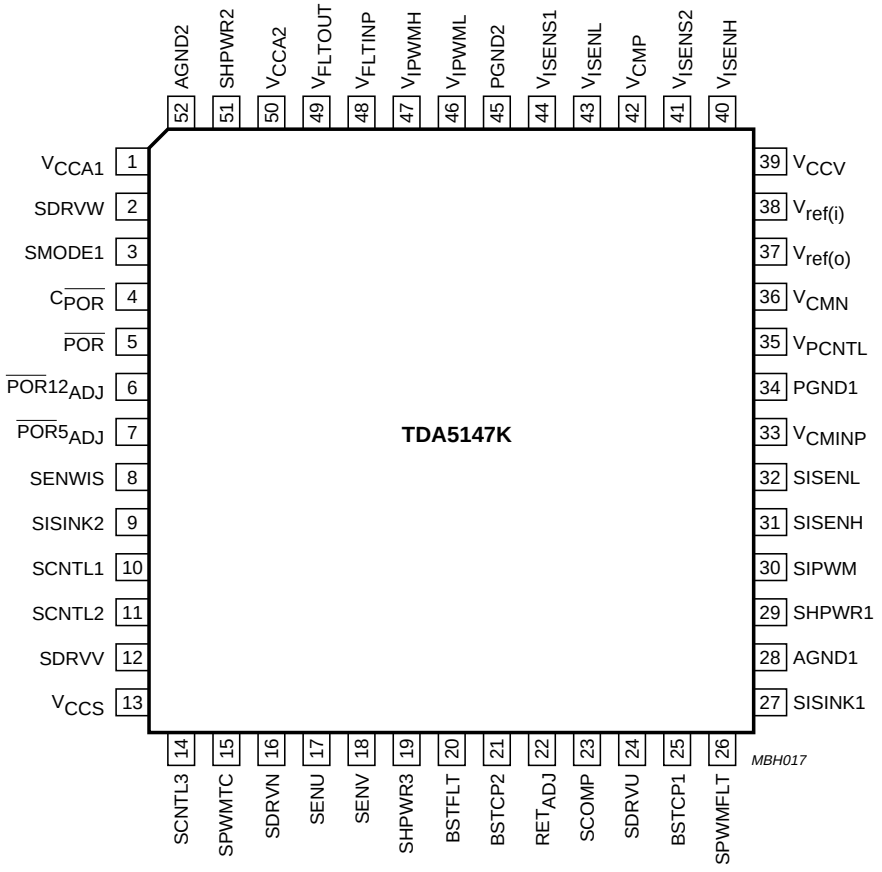


Fig.4 Pinning configuration.

FUNCTIONAL DESCRIPTION

Spindle drivers

The spindle section contains both the low and high side drivers (configured as H bridges) for a three-phase DC brushless motor. Back EMF (BEMF) sensing of the commutation rate needs to be output to an external digital ASIC circuit. This digital circuit also provides the input commutation control. Consequently, all speed control, start-up routine and commutation control will be generated by the digital circuit.

The SIPWM signal from the digital circuit is used to control the spindle current. This PWM signal is internally filtered. The output of this filter is duty factor dependent only. The filter characteristics is that of a 1-pole low-pass filter, with the pole location being controlled by the external capacitor connected to pin SPWMFLT.

Dynamic braking is possible only during non power-down situations and must be initiated by the digital circuit.

SMODE1

A 3-state level mode line (SMODE1) has been included to allow for;

1. An induction sensing algorithm in pre-start-up (V_{CCA1}).
2. PWM control during start-up ($0.5V_{CCA1}$).
3. Linear control (0 V).

SENSING MODE

The induction sensing mode is used for two purposes. Firstly one of the BEMF sensor outputs (SENWIS) will be shared with the voltage comparator that is used for the induction sensing function. Prior to start-up each phase can be excited for a short period of time. The current from each coil can be monitored via the multiplexed output (SENWIS). By comparing the rise times of each phase the rotor position can be determined.

Secondly, in situations where the spindle motor requires more current to spin-up, this mode is used with the exception that the output SENWIS is ignored. Since, in the induction sense mode, the output drivers are operated in saturation mode, the motor current is limited only by the power supply. This condition of induction sense mode can be used to overcome the head friction and must be used only when needed.

PWM MODE

The PWM mode is normally used during the start-up phase. Maximum drive voltage is applied to the low drivers to obtain high start-up torque. The purpose of the PWM mode is to drive the low drivers into saturation (saturation reduces the power dissipation in the TDA5147K during start-up).

When the spindle current reaches the programmed set current (SIPWM) value, a one-shot is fired. The output of the one-shot remains high for the programmed off-time (t_{off}) set by the capacitor/resistor network at the SPWMTC pin. The one-shot is not retriggerable for approximately 10% of the off-time, this gives a minimum of (10% t_{off}) time-on. During the off-time, the lower spindle output drivers are switched off. The on-time of the drivers is not fixed but is determined by the charging time of the coil current to reach the program set current.

The turn-off time is calculated by the equation:
$t_{off} = R \times C_{ln(2)}$

Where R = 68 kΩ and C = 220 pF, t_{off} = 10.4 μs.

The minimum on-time can be calculated by the equation:

$$t_{on} = \frac{CV}{I}$$

LINEAR MODE

The linear mode is used when the motor is near to its intended speed. It can also be used at start-up, but higher power dissipation will occur. In the linear mode the linear drivers are controlled by a sensing amplifier. A Miller network is used to obtain soft switching on the lower drivers. This prevents large voltage spikes on the motor coils when the lower drivers are switching. The high drivers are switched into the linear (resistive) region.

The transconductance gain of the low driver current to filter voltage can be calculated as follows:

$$G_m = \frac{I_{coil}}{V_{SPWMFLT}} = \frac{1}{R_s}\left\{\frac{V_{SISENH}}{V_{SPWMFLT}}\right\} = \frac{1}{R_s} = \frac{1}{5} = \text{A/V}$$

For a 100% duty factor at SIPWM, the nominal voltage at SPWMFLT = 1.74 V. The calculated coil current for a 100% duty factor (sense resistors R_S = 0.33 Ω) is:

$$I_{coil} = \frac{1}{0.33} \times \frac{1}{5} \times 1.74 = 1.05 \text{ A}$$

Referencing to the duty factor, the coil current is:

$$I_{coil} = \frac{1}{R_s} = \frac{1}{5} \times 1.74 \times \frac{0\% \text{ duty}}{100} = \frac{1}{R_s}(0.348) \times \frac{0\% \text{ duty}}{100}$$

The duty factor is arranged so that at 100%, the voltage SPWMFLT = 1.74 V and at a 5% duty factor SPWMFLT = 0 V. This is to ensure that at 0% duty factor the current will be zero (allowances for circuit tolerances).

The input decoder is driven by three lines which define the windings to be energized. The input decoder must then translate these lines to six lines to drive the six output drivers. The truth table is given in Table 1.

Table 1 Input decoder truth table

CONDITION	SCNTL1	SCNTL2	SCNTL3	SDRVU(1)	SDRVV(1)	SDRVW(1)
Disable	LOW	LOW	LOW	X	X	X
Dynamic brake	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
State 1	HIGH	HIGH	LOW	LOW	X	HIGH
State 2	HIGH	LOW	LOW	X	LOW	HIGH
State 3	HIGH	LOW	HIGH	HIGH	LOW	X
State 4	LOW	LOW	HIGH	HIGH	X	LOW
State 5	LOW	HIGH	HIGH	X	HIGH	LOW
State 6	LOW	HIGH	LOW	LOW	HIGH	X
Under voltage	–	–	–	X	X	X

Note

1. X = 3-state.

VCM driver

The VCM driver is a linear, class AB, H-bridge type power driver with all power devices internal to the chip. In addition to the power stage a sense resistor enables VCM current to be measured and brought out to a separate ADC via the V_{ISENS2} pin. The reference voltage for the V_{ISENS2} output is provided externally. The current level to the VCM is controlled via two PWM signals that are generated by the digital circuit. The input voltage at pin 47 (V_{IPWMH}) represents a weighting of 32 times more than the input voltage at pin 46 (V_{IPWML}), thus the current command is equal to 32 × duty factor ($V_{IPWML} + V_{IPWMH}$). These PWM signals are filtered by an internal 3rd-order low-pass filter (Butterworth filter). The bandwidth of this low-pass filter is nominally 40 kHz (less than 2 degrees lag at 500 Hz), but the real pole may be adjustable by an external capacitor. The analog output of the filter depends on the duty factor of the PWM signal and not on the logic level.

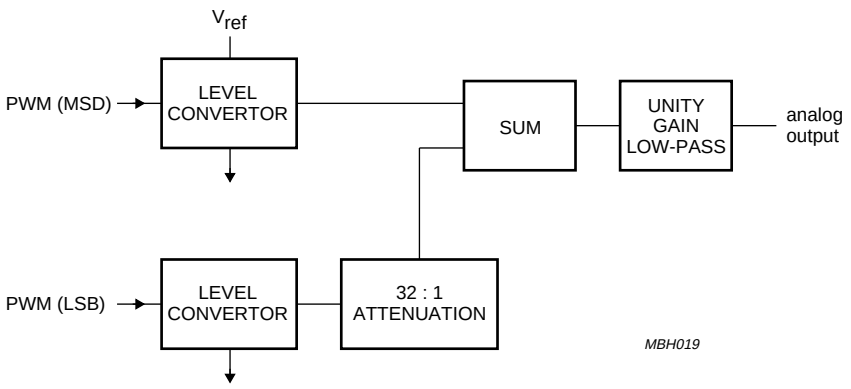


Fig.5 Block diagram of the PWM filter.

PARK ENABLE

A 3-state-level mode line (V_{PCNTL}) has been included that will:

1. Enable VCM drivers; V_{CCA1} (normal).
2. Disable VCM drivers; $0.5V_{CCA1}$.
3. PARK (soft retract the actuator); 0 V.

Enable VCM drivers

When the enable signal is HIGH, the VCM drivers are controlled by the two PWM inputs. The two digital signals convert the duty factor to a voltage level at V_{FLTOUT}. At a 100% duty factor the V_{FLTINP} voltage is approximately 1 V above $V_{ref(o)}$. At a 0% duty factor the V_{FLTINP} voltage is approximately –1 V below $V_{ref(o)}$. At a 50% duty factor, the voltage level is equal to $V_{ref(o)}$ (typical 4 V). The V_{FLTINP} voltage is amplified, filtered and output at V_{FLTOUT}. The voltage at V_{FLTOUT} varies between ±2 V about $V_{ref(o)}$. The V_{FLTOUT} voltage, in conjunction with the sense resistor amplifier, drives the two VCM drivers as illustrated in Fig.8. The transconductance equation that governs the voltage from V_{FLTINP} to I_{coil} is:

$$G_m = \frac{I_{coil}}{V_{FLTINP} - V_{ref(o)}} = \frac{I_{coil}}{(V_{FLTOUT} - V_{ref(o)})}$$

$$= 2 \times \frac{1}{gain} \times \frac{R2}{R1} \times \frac{1}{R_s} \text{ Amps per Volt}$$

In a typical application:

$$\frac{I_{coil}}{V_{FLTINP} - V_{ref(o)}} = \frac{2}{4} \times \frac{6.6\ k\Omega}{10\ k\Omega} \times \frac{1}{0.33} = 1 \text{ Amp per Volt}$$

The transconductance is variable by selecting external resistors R2/R1 and sense resistors R_s

Disable VCM drivers

With the PARK enable signal at 0.5V the VCM drivers are disabled while the rest of the circuits remain enabled. A sleep mode is initiated when the spindle and VCM are disabled (this places the TDA5147K in its lowest power setting).

ACTUATOR PARK

Retracting the actuator can be accomplished by driving V_{PCNTL} LOW in conjunction with either the spindle is turning or a brake voltage has been applied. An adjustable retract voltage of 1.2 V (max.) is applied between the V_{CMN} and V_{CMP} outputs. The retract circuit obtains its retract current from the spindle SDRVU phase. If the SDRVU phase is zero there will be no retract voltage.

The retract voltage is determined by two external resistors. One end is tied to V_{CMN} and the other to ground. The common point is tied to pin 22 (RET_{ADJ}); see Fig.1 for additional information.

The calculation of $V_{RETRACT}$ is as follows:

$$V_{RETRACT} = 0.65 \times \left(\frac{1 + R2}{R1} + \frac{R2}{50\ k\Omega} \right)$$

Where 0.65 is V_{BE} at 25 °C $\Delta V_{BE}/\Delta T$ = –2 mV/°C; 50 kΩ can vary by ±30%

It should be noted that R2 has to be less than 10 kΩ.

Power-on reset

The power-on reset circuit monitors the voltage levels of both the +5 V and the +12 V supply voltages as shown in Fig.6. The $\overline{POR}$ (active LOW) logic line is set HIGH following a supply voltage rise above a specified voltage threshold plus a hysteresis, and delayed by a time, t_C that is controlled by an external capacitor. This $\overline{POR}$ signal should remain HIGH until either the +5 or +12 V supplies drop below the voltage threshold, at which point the $\overline{POR}$ line should be asserted LOW.
The t_C timing is set by the following equation:

$$t_C = \frac{C \times V_{th}}{I}$$

Where V_{th} = 2.5 V and I is 12 μA (typ.).

A negative going pulse width of 5 μs on either the +5 or +12 V rail will provide a full output pulse. If another trigger pulse occurs before the output is completed a new output pulse will be originated. This implies the power-on reset circuit is a retriggerable one-shot with a maximum trigger pulse of 5 μs (see Fig.7).

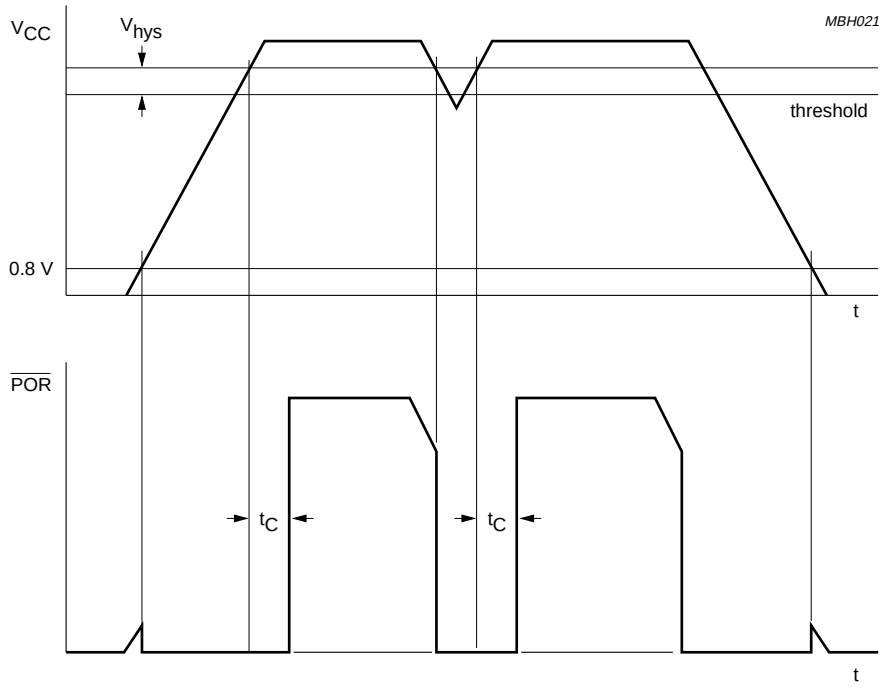


Fig.6 Power-on reset timing.

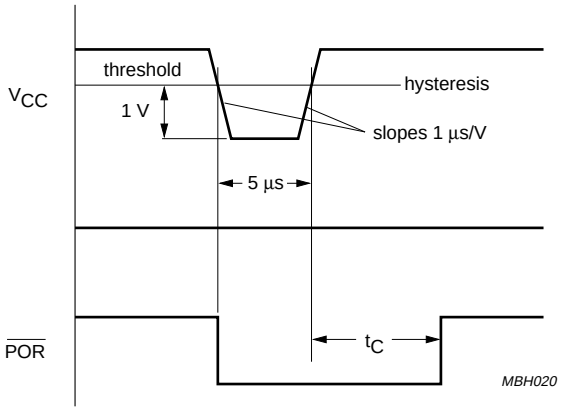


Fig.7 Trigger pulse requirement.

During a power-down situation the power-on reset circuit must not only generate a $\overline{POR}$ output signal, but must also activate the VCM retract circuitry. In doing so, the VCM driver draws power from the BEMF of the SDRVU output during spin-down, and uses this power to bias the VCM against one of the hard stops of the actuator. This prevents the heads from landing on data zones. This BEMF supply is isolated from the supply voltage for the drive, and is half-wave rectified. An external retract capacitor is used to provide the supply voltage for the retract circuit.

It should be noted that in both power-down retract and command retract situations, the voltage across the VCM is nominally limited to 1.2 V (to limit the velocity of the actuator). Additional information is given in Fig.6.

SLEEP MODE

A sleep mode is used to save power when the spindle drivers and the VCM drivers are in a disabled state. These two conditions automatically turn off all drivers and amplifiers that are not required. The total power dissipation is approximately 100 mW. The sleep mode is activated when both the spindle is disabled (SCNTL1, 2 and 3 = 0) and the VCM is disabled (V_{PCNTL} left open-circuit).

THERMAL SHUTDOWN

When the TDA5147K chip temperature is greater than 150 °C all power drivers will be automatically disabled. This is to ensure that no fire hazard occurs due to chip overheating.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA1}	analog supply voltage 1	indefinite time period	–0.3	6.0	V
		note 1	–0.3	7.0	V
V_{CCA2}	analog supply voltage 2	indefinite time period	–0.3	13.5	V
		note 1	–0.3	15.0	V
V_o	output voltage (pins 2, 12 and 24)		–0.3	20	V
V_n	output voltage on other pins		–0.3	–	V
T_{stg}	IC storage temperature		–55	+125	°C
T_j	maximum junction temperature		–	150	°C
T_{amb}	operating ambient temperature		0	70	°C

Note

1. Stress beyond these levels may cause permanent damage to the device. This is a stress rating only and functional operation of the device under this condition is not implied.

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL CHARACTERISTICS

See report AA94052 (dated 94-02-03): *"PLCC52 - Thermal resistance evaluation".*

SYMBOL	PARAMETER	VALUE	UNIT
$T_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	30	K/W

OPERATING CHARACTERISTICS

V_{CCA1} = 5 V; V_{CCS} = V_{CCA2} = V_{CCV} = 12 V; T_{amb} = 0 to 70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA1}	analog supply voltage 1		4.5	5	5.5	V
V_{CCS}	supply voltage for spindle motor drivers		10.8	12	13.2	V
V_{CCV}	supply voltage for VCM driver		10.8	12	13.2	V
V_{CCA2}	analog supply voltage 2		10.8	12	13.2	V
Reference voltage; pin 38 ($V_{ref(i)}$)						
$V_{ref(i)}$	reference voltage input		1.75	–	2.75	V
Upper booster						
C_O	external output capacitor	connected between BSTCP1 and BSTCP2	–	10	–	nF
C_{CP}	charge pump capacitor	connected between BSTFLT and ground	–	22	–	nF
Spindle low side; pin 15 (SPWMTC)						
C_{sl}	capacitor for spindle low side		–	220	–	pF
R_{sl}	resistor for spindle low side		–	68	–	kΩ
Capacitors for PARK voltage supply; pins 19 and 51 (SHPWR3 and SHPWR2)						
C_{clamp}	clamp capacitor		–	22	–	µF
Digital PWM input; pin 30 (SIPWM)						
V_{IH}	HIGH level input voltage		3	5	5.5	V
V_{IL}	LOW level input voltage		–0.3	0	2	V
Digital inputs of spindle decoder; pins 10, 11 and 14 (SCNTL1, 2 and 3)						
V_{IH}	HIGH level input voltage	see Table 1; V_{CCA1} = 5 V	3.5	–	–	V
3-state level input; pin 3 (SMODE1)						
V_{oh}	3-state voltage level for current sense in non PWM mode		$0.75V_{CCA1}$ + 150 mV	–	–	V
V_{iZ}	3-state voltage level for BEMF sense and PWM switch control	see Table 1; state also achieved with floating input	$0.25V_{CCA1}$ + 150 mV	$0.50V_{CCA1}$	$0.75V_{CCA1}$ – 150 mV	V
V_{ol}	3-state voltage level for BEMF sense and linear control		–	–	$0.25V_{CCA1}$ – 150 mV	V
Control amplifier; pin 23 (SCOMP)						
C_{SCOMP}	control loop capacitor		–	47	–	nF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PARK enable; pin 35 (V_{PCNTL})						
V_{oh}	voltage level for enable		0.75_{VCCA1} + 150 mV	–	–	V
V_{iZ}	voltage level for disable	see Table 1; state also achieved with floating input	$0.25V_{CCA1}$ + 150 mV	$0.50V_{CCA1}$	$0.75V_{CCA1}$ – 150 mV	V
V_{ol}	voltage level for retract		–	–	$0.25V_{CCA1}$ – 150 mV	V
PWM decoder; pins 46 and 47 (V_{IPWML} and V_{IPWMH})						
V_{IH}	HIGH level input voltage		3.0	–	–	V
V_{IL}	LOW level input voltage		–	–	2.0	V
f_{PWM}	frequency range at the inputs of the PWM	C_{FLTINP} = 1.8 nF	–	–	625	kHz
T_{PWM}	PWM pulse width		25	–	–	ns
Sense resistor amplifier; pins 40 and 43 (V_{ISENH} and V_{ISENL})						
V_{iCM}	common mode input sense voltage		0	–	2	V
$R_{s(S)}$	spindle sense resistor		–	0.33	–	Ω
Power-on reset generator						
$C_{\overline{POR}}$	power-on reset capacitor	see Fig.6	–	220	–	nF
VCM PWM filter						
C_{FLTINP}	filter capacitor		–	1.8	–	nF
VCM driver						
$R_{s(VCM)}$	VCM sense resistor		–	0.33	–	Ω

ELECTRICAL CHARACTERISTICS

V_{CCA1} = 5 V; V_{CCS} = V_{CCA2} = V_{CCV} = 12 V; T_{amb} = 0 to 70 °C; note 1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog supply current (nominal voltage)						
I_{CCA1}	analog supply current 1	linear (no spindle or VCM load)	–	5.0	8.0	mA
		sleep mode (no spindle or VCM load)	–	3.0	–	mA
I_{CCA2}	analog supply current 2	linear (no spindle or VCM load)	–	20	33	mA
		sleep mode (no spindle or VCM load) sense resistor output	–	2.3	–	mA
		sleep mode (no spindle or VCM load) sense resistor input	–	6.0	–	mA
P_{tot}	total power dissipation	sleep mode	–	–	150	mW

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Voltage booster; pin 20 (BSTFLT)						
V_{oCP}	charge pump output voltage	nominal voltages	18.2	19.2	19.8	V
I_{oCP}	charge pump output current	voltage drop of 100 mV across booster	–	1.5	–	mA
Power monitor comparators; pins 6 and 7 ($\overline{POR12}_{ADJ}$ and $\overline{POR5}_{ADJ}$)						
V_{th12}	threshold voltage level adjustment for +12 V		8.7	9.0	9.3	V
V_{th5}	threshold voltage level adjustment for +5 V		4.4	4.5	4.6	V
V_{hys1}	hysteresis on V_{CCA1} comparator	hysteresis in positive direction.	40	60	80	mV
V_{hys2}	hysteresis on V_{CCA2} comparator	hysteresis in positive direction.	130	200	270	mV
V_{12adj}	power-on reset 12 V adjustable voltage	normal power supply to resistor divider 25.4 and 9.7 kΩ	3.25	3.32	3.39	V
V_{5adj}	power-on reset 5 V adjustable voltage	normal power supply to resistor divider 7.86 and 10 kΩ	2.74	2.8	2.86	V
Power-on reset generator; pins 4 and 5 ($C_{\overline{POR}}$ and $\overline{POR}$); see Fig.6						
V_{OL}	LOW level input voltage	I_{OL} = 2 mA; V_{CC} = 5 or 12 V (below threshold voltage)	–	–	0.7	V
V_{OH}	HIGH level input voltage	V_{CC} = 5 or 12 V (above hysteresis voltage)	4.85	–	–	V
I_{source}	source current for charging capacitor (pin 4)		8.2	12	15.3	µA
V_{th}	threshold voltage (pin 4)		–	2.5	–	V
$t_{d\overline{POR}}$	power-on reset delay	C = 220 nF	–	45	–	ms
t_{RPULSE}	power supply maximum pulse duration	see Fig.7	–	2.5	5.0	µs
Thermal protection						
T_{Soff}	switch-off temperature	prevents fire hazard (junction temperature)	150	–	164	°C
ΔT	thermal hysteresis		–	30	–	°C

Note

1. V_{CCA2}, V_{CCV}, V_{CCS} and V_{CCA1} are connected together; the outputs SDRVU, SDRVV, SDRVW, VCMP and VCMN are not loaded. Sleep mode defined by 000 as spindle code and VCM disable.

SPINDLE MOTOR DRIVER CHARACTERISTICS

V_{CCA1} = 5 V; V_{CCS} = V_{CCA2} = V_{CCV} = 12 V; T_{amb} = 0 to 70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Overvoltage protection; pins 2, 12 and 24 (SDRVW, SDRVV and SDRVU)						
V_{CLP}	overvoltage protection clamping voltage	power supply off; apply voltage to outputs; check clamping voltage is at 100 mA	–	19	–	V
Spindle state control inputs; pins 10, 11 and 14 (SCNTL1, 2 and 3)						
I_i	input current		–10	–	+10	μA
Back EMF comparators						
V_{CM}	common mode input voltage for centre TAP connection (pin 16)	comparators will be operational with other inputs at V_{CCA2} – 1 V	–0.5	–	V_{CCA2} + 0.7	V
I_{CLP}	common mode clamping current	V_{16} = 0 V	–1.6	–	–0.2	mA
V_{Cos}	comparator offset voltage relative to pin 16	SDRVN voltage range from 3 to 10 V	–5	–	+5	mV
ΔV_{Cos}	variation in comparator voltages	for the same IC	–7	–	+7	mV
V_{sink}	comparators output drive sink voltage	$I_{o(sink)}$ = 1 mA	–	–	0.5	V
V_{source}	comparators output drive source voltage	$I_{o(source)}$ = 40 μA	2.7	–	–	V
Spindle output drivers; pins 2, 12 and 24 (SDRVW, SDRVV and SDRVU)						
$R_{ds(on)}$	total resistance at output (source + sink + isolation)	I_o = 1 A at T_{amb} = 25 °C	–	0.8	1.0	Ω
		I_o = 1 A at T_j = 125 °C	–	1.3	1.7	Ω
I_{LO}	off-state output leakage current	T_j = 125 °C	–	0.3	1.0	mA
V_F	recirculating diode forward voltage	I_F = 1 A	–	0.8	–	V
SRT	slew rate test	test for Miller network	0.12	–	0.24	V/μs
Spindle current control PWM DAC and filter; pins 26 and 30 (SPWMFLT and SIPWM)						
I_{30}	input current at pin 30	at HIGH-to-LOW voltage transition	–200	–	+200	mA
R_{26}	output resistance at pin 26		23	34	45	kΩ
V_{26}	output voltage	100% duty factor at pin 30	–	1.75	–	V
		50% duty factor at pin 30	–	0.85	–	V
		0% duty factor at pin 30	–	0	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PWM one-shot; pin 15 (SPWMTC)						
I_{sink}	output sink current	V_o = 3 V	600	850	1100	μA
I_{source}	output source current	V_o = 1 V	–	–12	–	μA
V_{thST}	threshold voltage start level	voltage for discharging	2.0	2.56	3.0	V
V_{thEND}	threshold voltage end level	voltage for charging	–	0.1	0.2	V
t_{off}	one-shot off time	external network of R = 68 kΩ and C = 220 pF	–	10	–	μs
$t_{on(min)}$	one-shot minimum on time	external network of R = 68 kΩ and C = 220 pF	1	–	–	μs
Current control loop and sense amplifier; pins 23 and 31 (SCOMP and SISENH)						
V_i	current sense amplifier common mode input voltage	current sense amplifier operational over range	0	–	3.0	V
I_{SENSE}	current sense amplifier input current		–10	–	–	μA
V_{ratio}	voltage ratio between SPWMFLT and SISENH	over sense resistance = 0.1 to 1 Ω	4.9	5.0	5.1	V/V
V_{31}	output voltage at SENSH (pin 31)	for 100% duty factor; R_s = 0.33 Ω; note 1	0.317	0.335	0.353	V
		for 50% duty factor; R_s = 0.33 Ω	–	0.174	–	V
		for 5% duty factor; R_s = 0.33 Ω; note 2	0	0.018	0.026	V
		for 0% duty factor; R_s = 0.33 Ω; note 3	0	0	1.0	mV
B_{WD}	current loop bandwidth for SPWMFLT to motor current	R_s = 0.33 Ω, L_{motor} = 1 mH, R_{motor} = 12.0 Ω	–	1	–	kHz

Notes

1. Maximum current will be activated at 100% duty factor.
2. 5% duty factor guarantees current output.
3. Zero duty factor guarantees zero current output.

VOICE COIL MOTOR DRIVER CHARACTERISTICS

V_{CCA1} = 5 V; V_{CCS} = V_{CCA2} = V_{CCV} = 12 V; T_{amb} = 0 to 70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Retract control voltage; pin 22 (RET_{ADJ})						
I_{RET}	retract voltage load current	V_{29} = 9 V; power supplies off	–	3.0	–	µA
$t_{h;RET}$	retract voltage hold time (power down)	retract capacitor = 2.2 µF	5	–	–	s
V_{RET}	retract voltage regulation	nominal power supply at T_{amb} = 25 °C	–	1.0	–	V
		power supply off; V_{24} = 9 to 2 V; V_{29} = 7.5 V	–	1.0	–	V
VCM current control PWM DAC; pins 46 to 48 (V_{IPWML}, V_{IPWMH} and V_{FLTINP})						
$I_{47, 46}$	input current at pins 47 and 46	voltage range 0 to 5 V	–200	–	+200	µA
$V_{FL(p)}$	positive full scale DAC output voltage at pin 48 relative to pin 37	100% duty factor	–	+1.0	–	V
$F_{LI(n)}$	negative full scale DAC output voltage at pin 48 relative to pin 37	0% duty factor	–	–1.0	–	V
	current ratio between MSB and LSB		31.5	32	32.5	
Z_o	output impedance from pin 48 to pin 37		1.40	2.0	2.6	kΩ
VCM PWM filter; pins 48 and 49 (V_{FLTINP} and V_{FLTOUT})						
I_o	output current on pin 49	$V_{49} = \Delta V_o$ + 10 mV	500	–	–	µA
$\Delta\Phi$	maximum phase shift from pin 48 to pin 49	measured at 500 Hz; C_{filter} = 1.8 nF	–	–	2	deg
f_{co}	filter cut-off frequency from pin 48 to pin 49		–	40	–	kHz
α_{filter}	filter attenuation at 1 MHz measured from pin 48 to pin 49		–	70	–	dB
V_{49}	output voltage range measured at pin 49	pins 46 and 47 at 0% duty factor	V_{37} – 2.06	V_{37} – 1.98	V_{37} – 1.90	V
		pins 46 and 47 at 50% duty factor	0.065	V_{37}	0.065	V
		pins 46 and 47 at 100% duty factor	V_{37} + 1.90	V_{37} + 1.98	V_{37} + 2.06	V
Reference voltage; pin 37 ($V_{ref(o)}$)						
$V_{ref(o)}$	output reference voltage	I_o = 4 mA; C_L = 10 nF	3.8	4.0	4.2	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Current sense amplifier; pins 38, 40, 41, 43 and 44 ($V_{ref(i)}$, V_{ISENH}, V_{ISENS2}, V_{ISENL} and V_{ISENS1})						
$I_{40, 43}$	input current at pins 40 and 43	overvoltage range of 0 to 12 V	–200	415	540	µA
I_{sink1}	output sink current 1 (pin 44)	force $V_{40} - V_{43}$ to equal –250 mV; allow output drop of 100 mV between no load and full load	+400	–	–	µA
$I_{source1}$	output source current 1 (pin 43)	force $V_{40} - V_{43}$ to equal –250 mV; allow output drop of 100 mV between no load and full load	–	–	–400	µA
$V_{40, 43}$	operating voltage range (pins 40 and 43)	gain and offset valid	0	–	12	V
G1	amplifier gain for $V_{44} - V_{37}/V_{40} - V_{43}$	under all conditions	3.8	4.0	4.2	V/V
V_{os1}	output offset voltage	$V_{40} - V_{43}$ = 0 V at $0.5V_{CC}$	–15	–	+15	mV
B_{G1}	unity gain bandwidth		–	10	–	MHz
PSRR	power supply rejection ratio	f_i < 20 kHz	–	60	–	dB
$V_{40, 43}$	operating voltage range (pins 40 and 43)	gain and offset valid	0	–	12	V
I_{sink2}	output sink current 2 (pin 41)	force $V_{40} - V_{43}$ to equal –250 mV; allow output drop of 100 mV between no load and full load	+400	–	–	µA
$I_{source2}$	output source current 2 (pin 43)	force $V_{40} - V_{43}$ to equal –250 mV; allow output drop of 100 mV between no load and full load	–	–	–400	µA
G2	amplifier gain for $V_{41} - V_{38}/V_{40} - V_{43}$	under all conditions	3.8	4.0	4.2	V/V
V_{os2}	output offset voltage	$V_{40} - V_{43}$ = 0 V at $0.5V_{CC}$	–23	–	+23	mV
B_{G2}	unity gain bandwidth		–	10	–	MHz
$V_{ref(i)}$	input voltage level (pin 38)		–	–	4.5	V
$I_{ref(i)}$	input current range (pin 38)	V_i = 0 to 4.5 V	–	0.06	1	µA
VCM output drivers; pins 33, 36 and 42 (V_{CMINP}, V_{CMN} and V_{CMP})						
R_{tot}	total output resistance (source + sink + isolation)	T_{amb} = 25 °C	–	1.0	1.25	Ω
		T_j = 125 °C	–	1.5	1.9	Ω
I_{LO}	output leakage current	T_j = 125 °C	–	–	1	mA
B_G	unity gain bandwidth	from pin 33 to pins 36 and 42	–	2	–	MHz
t_{cro}	crossover distortion time	ramp input pin 33 = 20 µs	–	2	5	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RATIO = $\frac{/2}{/1}$	symmetry of VCM drivers (pins 33 and 36)	$I_2 = I_{RVCM}$ at duty factor = 10%; $I_1 = I_{RCVM}$ at duty factor = 90%; $I_0 = I_{RCVM}$ at duty factor = 50%; R_S = 0.33 Ω; R_1 = 10 kΩ, R_2 = 6.6 kΩ, R_L = 15 Ω	0.93	1	1.03	
L = $\left\lvert\frac{/2 - /0}{/1 - /0}\right\rvert$	linearity of VCM drivers (pins 33 and 36)	$I_2 = I_{RVCM}$ at duty factor = 10%; $I_1 = I_{RCVM}$ at duty factor = 90%; $I_0 = I_{RCVM}$ at duty factor = 50%; R_S = 0.33 Ω; R_1 = 10 kΩ, R_2 = 6.6 kΩ, R_L = 15 Ω	0.97	1	1.03	
I_{os}	VCM output offset current	pins 47 and 46 at 50% duty factor; R_S = 0.33 Ω; R_1 = 10 kΩ, R_2 = 6.6 kΩ, R_L = 15 Ω	−28	0	+28	mA
I_{33}	input current (pin 33)	V_i = 0 to 10 V	–	0.07	0.2	µA
V_{33}	input offset voltage (pin 33)	from pin 33 to pin 37	−10	–	+10	mV

MODE TABLES

Table 2 V_{PCNTL} and SCNTL modes

MODES OF OPERATION AT POWER GOOD ($\overline{POR}$ = HIGH)	V_{PCNTL} INPUT STATE(1)	SCNTL INPUT STATES(1)		
		SCNTL1	SCNTL2	SCNTL3
VCM enable	HIGH	X	X	X
VCM disable	high impedance	X	X	X
Park	LOW	X	X	X
Spindle enable	X	see Table 3	see Table 3	see Table 3
Spindle disable	X	LOW	LOW	LOW
Spindle brake	X	HIGH	HIGH	HIGH
Spindle mode	high impedance	LOW	LOW	LOW

Note

1. X = Don't care.

Table 3 Booster, driver, comparator, decoder, amplifier and filter modes

FUNCTION	UPPER BOOSTER	UPPER DRIVERS	LOWER DRIVERS	COMPARATOR	CONTROL AMPLIFIER
Spindle enable	ON	ON	ON	ON	ON
Spindle disable	ON	ON	ON	ON	ON
$\overline{POR}$ LOW	OFF	OFF	ON	ON	OFF
Sleep	OFF	OFF	ON	ON	OFF

Table 4

FUNCTION	ONE-SHOT	CURRENT COMPARATOR	PWM DECODER FILTER	SMODE COMPARATOR	CURRENT SENSE AMPLIFIER	LOGIC DECODER
Spindle enable	ON	ON	ON	ON	ON	ON
Spindle disable	ON	ON	ON	ON	ON	ON
$\overline{POR}$ LOW	ON	ON	ON	ON	OFF	ON
Sleep	ON	ON	ON	ON	OFF	ON

Table 5 V_{ISBUF}, PWM, power, $\overline{POR}$, retract, reference, sense, thermal, voltage and sleep modes

FUNCTION	V_{ISREF} BUFFER	PWM DECODER	12 AND 5 V COMPARATOR	FILTER AMPLIFIER	$\overline{POR}$ DETECTOR	RETRACT CIRCUIT
VCM enable	ON	ON	ON	ON	ON	OFF
VCM Disable	ON	ON	ON	ON	ON	OFF
Park	ON	ON	ON	ON	ON	ON
Sleep	OFF	OFF	ON	OFF	ON	OFF
$\overline{POR}$ LOW	OFF	OFF	ON	OFF	ON	ON

Table 6

FUNCTION	VOLTAGE 3-STATE LEVEL	Vref OUTPUT BUFFER	Vref OUTPUT	SENSE2	SENSE1	VCM POWER AMPLIFIER	VOLTAGE GENERATOR	THERMAL SHUTDOWN	SLEEP FUNCTION
VCM enable	ON	ON	ON	ON	ON	ON	ON	ON	OFF
VCM disable	ON	ON	ON	ON	ON	OFF	ON	ON	OFF[2]
Park[1]	ON	ON	ON	ON	ON	OFF	ON	ON	OFF
Sleep	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	ON[3]
$\overline{POR}$ LOW	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	ON

Notes

1. Park will provide adjustable retract if the spindle brake is on, or if the spindle brake is enabled.
2. If disable SP is OFF.
3. Requires disable SP and VCM disable to be ON.

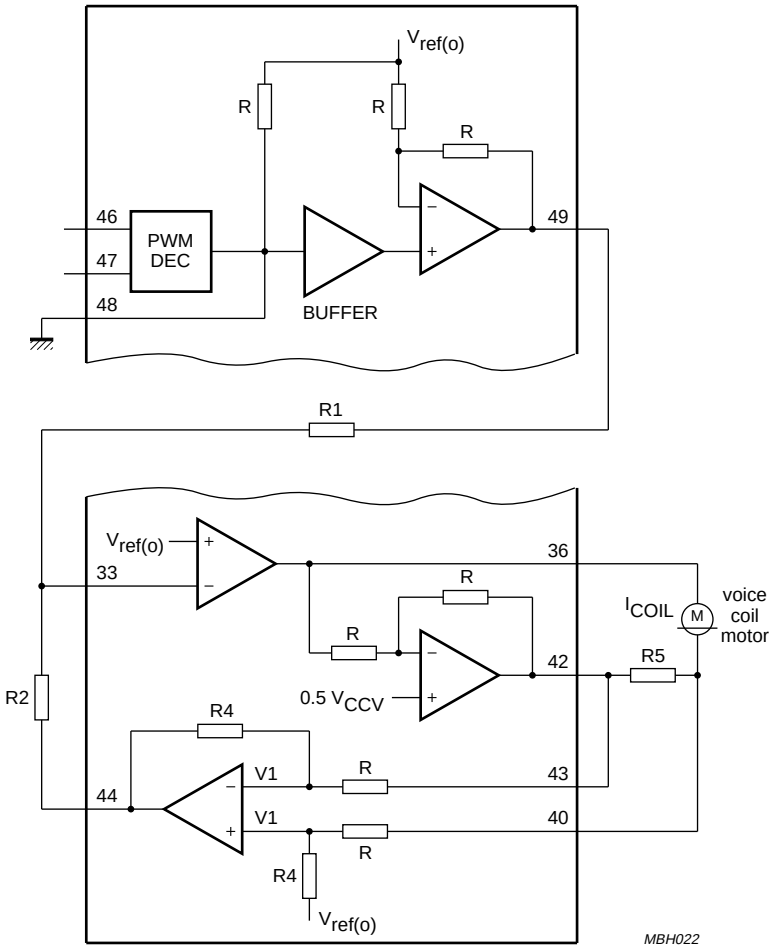


Fig.8 Transconductance model.

EQUATIONS

Gain from V_{FLTINP} to V_{FLTOUT}

$$\frac{V_{FLTOUT} - V_{ref(o)}}{V_{FLTINP} - V_{ref(o)}} = 2 \quad (1)$$

Gain from V_{FLTOUT} to V_{ISENS1} (under closed loop $V_{CMINP} = V_{ref(o)}$)

$$\frac{V_{FLTOUT} - V_{ref(o)}}{R1} = \frac{V_{ISENS1} - V_{ref(o)}}{R2} \text{ or } \frac{V_{FLTOUT} - V_{ref(o)}}{V_{SENS1} - V_{ref(o)}} = \frac{R1}{R2} \quad (2)$$

Gain of V_{ISENS1} relative to ΔV_s (voltage across R_s)

$$\text{HAVE } \frac{V1 - V_{ref(o)}}{4R} = \frac{V_{ISENH}}{R} \quad \frac{V1 - V_{SENS1}}{4R} = \frac{V_{ISENL}}{R} \quad (3)$$

$$\text{SUB } \frac{1 - V_{ref(o)}}{4R} = \frac{V_{ISENL} - V_{ISENH}}{R} = \frac{\Delta V_s}{R} \text{ or } \frac{V_{SENS1} - V_{ref(o)}}{\Delta V_s} = 4 \quad (4)$$

Transconductance Equation

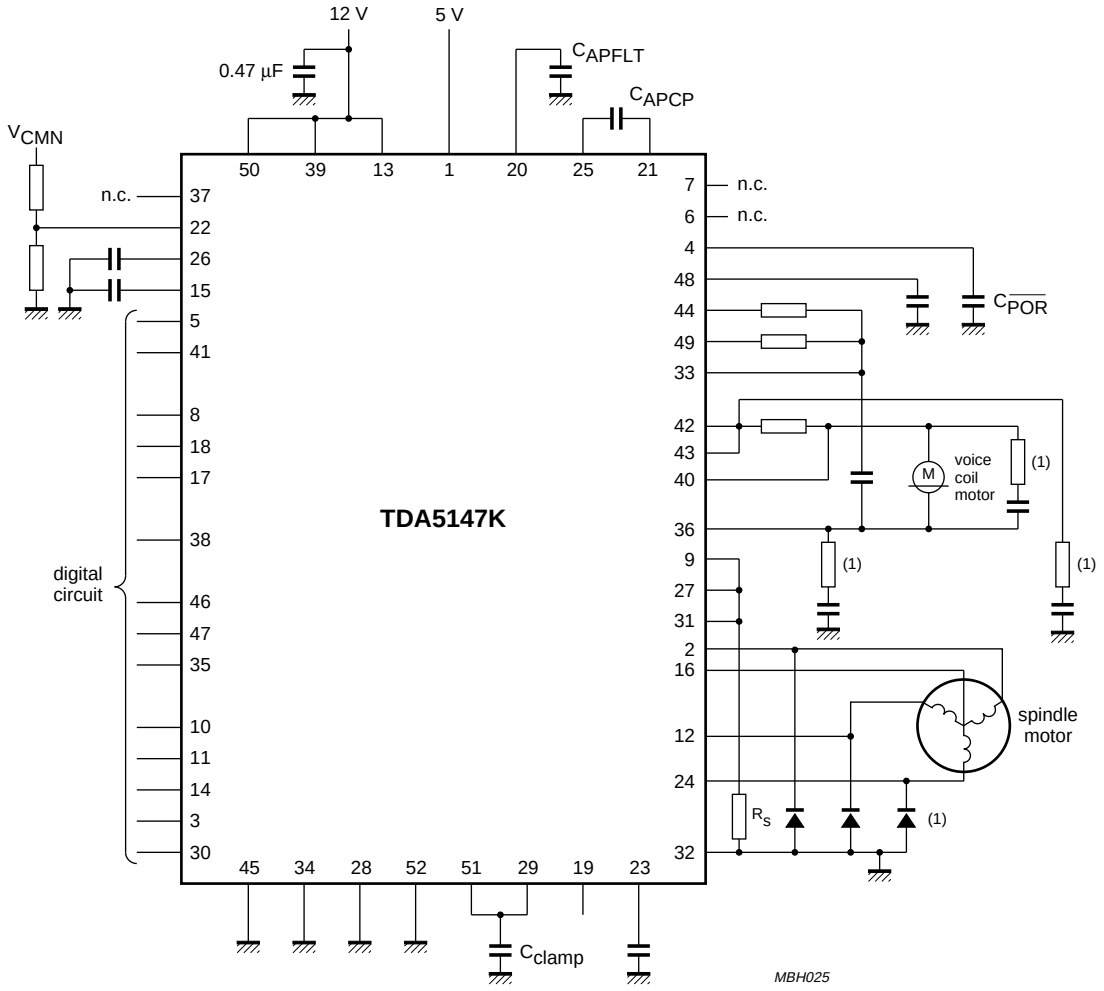
$$G_m = \frac{I_{COIL}}{V_{FLINP} - V_{ref(o)}} = \frac{\Delta V_s}{R_s} \times \frac{1}{V_{FLINTP} - V_{ref(o)}} \quad (5)$$

From equation (1) $G_m = \frac{\Delta V_s}{R_s} \quad \frac{2}{V_{FTOUT} - V_{ref(o)}}$

From equation (2) $G_m = \frac{\Delta V_s}{R_s} \times 2 \times \frac{R2}{R1} (V_{SENS1} - V_{ref(o)})$

From equation (3) and (4) $G_m = \frac{1}{R_s} \times \frac{1}{4} \times 2 \times \frac{R2}{R1} = \frac{1}{2} \times \frac{1}{R_s} \times \frac{R2}{R1}$

APPLICATION INFORMATION

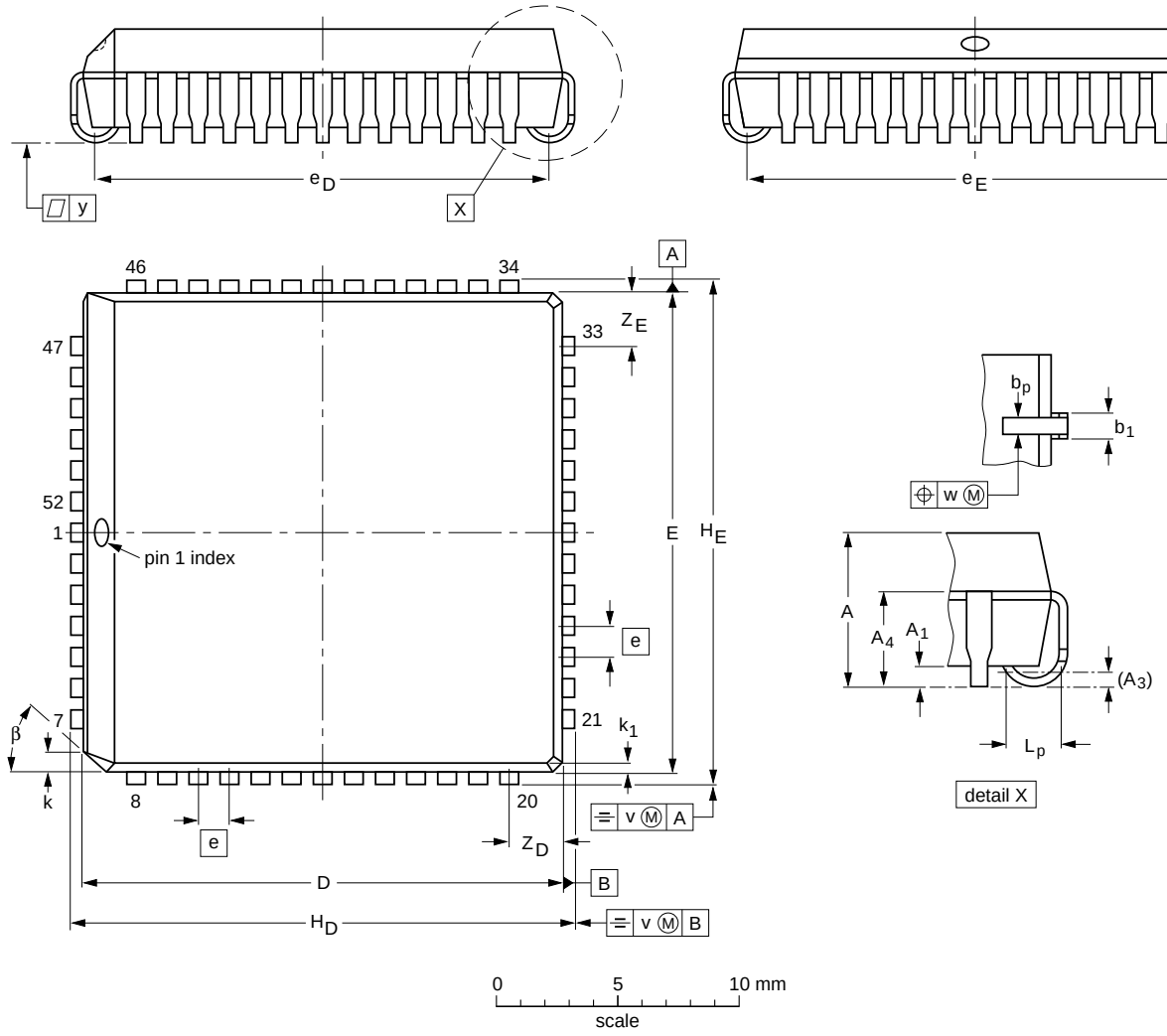


(1) Optional.

Fig.9 Application diagram.

PACKAGE OUTLINES

PLCC52: plastic leaded chip carrier; 52 leads **SOT238-2**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	k_1 max.	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	19.15 19.05	19.15 19.05	1.27	18.54 17.53	18.54 17.53	20.19 19.94	20.19 19.94	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.12	0.021 0.013	0.032 0.026	0.754 0.750	0.754 0.750	0.05	0.730 0.690	0.730 0.690	0.795 0.785	0.795 0.785	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT238-2						~~92-10-08~~ 95-02-25

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all PLCC packages.

The choice of heating method may be influenced by larger PLCC packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all PLCC packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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