TEA1532BT; TEA1532CT

GreenChip II SMPS control IC

Rev. 01 — 18 January 2007 Product data sheet

1. General description

The GreenChip II is the second generation of controller ICs intended for green flyback Switched Mode Power Supplies (SMPS). Its high level of integration allows the design of a cost effective power supply with a very low number of external components.

The TEA1532BT; TEA1532CT can also be used in fixed frequency, Continuous Conduction Mode (CCM) converter designs for low voltage and high current applications. At low power (standby) levels the system operates in cycle skipping mode which minimizes the switching losses during standby.

The special built-in green functions allow the efficiency to be optimum at all power levels. This holds for quasi-resonant operation at high power levels, as well as fixed frequency operation with valley switching at medium power levels. At low power (standby) levels, the system operates in cycle skipping mode with valley detection.

The proprietary high voltage BCD800 process makes direct start-up possible from the rectified universal mains voltage in an effective and energy efficient way. A second low voltage, Bipolar CMOS (BICMOS) IC is used for accurate, high speed protection functions and control.

The TEA1532BT; TEA1532CT enables highly efficient and reliable supplies to be designed easily.

2. Features

2.1 Distinctive features

- Universal mains supply operation (70 V to 276 V AC)
- High level of integration resulting in a very low external component count
- Fixed frequency Continuous Conduction Mode (CCM) operation capability
- Quasi-Resonant (QR) Discontinuous Conduction Mode (DCM) operation capability

2.2 Green features

- Valley or zero voltage switching for minimum switching losses in QR operation
- Cycle skipping mode at very low loads; input power < 300 mW at no-load operation for a typical adapter application
- On-chip start-up current source

2.3 Protection features

- Safe restart mode for system fault conditions
- Zero current switch-on in QR mode

- Undervoltage protection (fold back during overload)
- IC OverTemperature Protection (OTP) (latched)
- Low and adjustable OverCurrent Protection (OCP) trip level
- Soft (re)start
- Mains voltage-dependent operation-enabling level
- TEA1532CT: general purpose input for latched or safe restart protection and timing, e.g. to be used for OverVoltage Protection (OVP), output short-circuit protection or system OTP
- TEA1532BT: general purpose input for latched protection and timing, e.g. to be used for OVP, output short-circuit protection or system OTP
- Brown-out protection

3. Applications

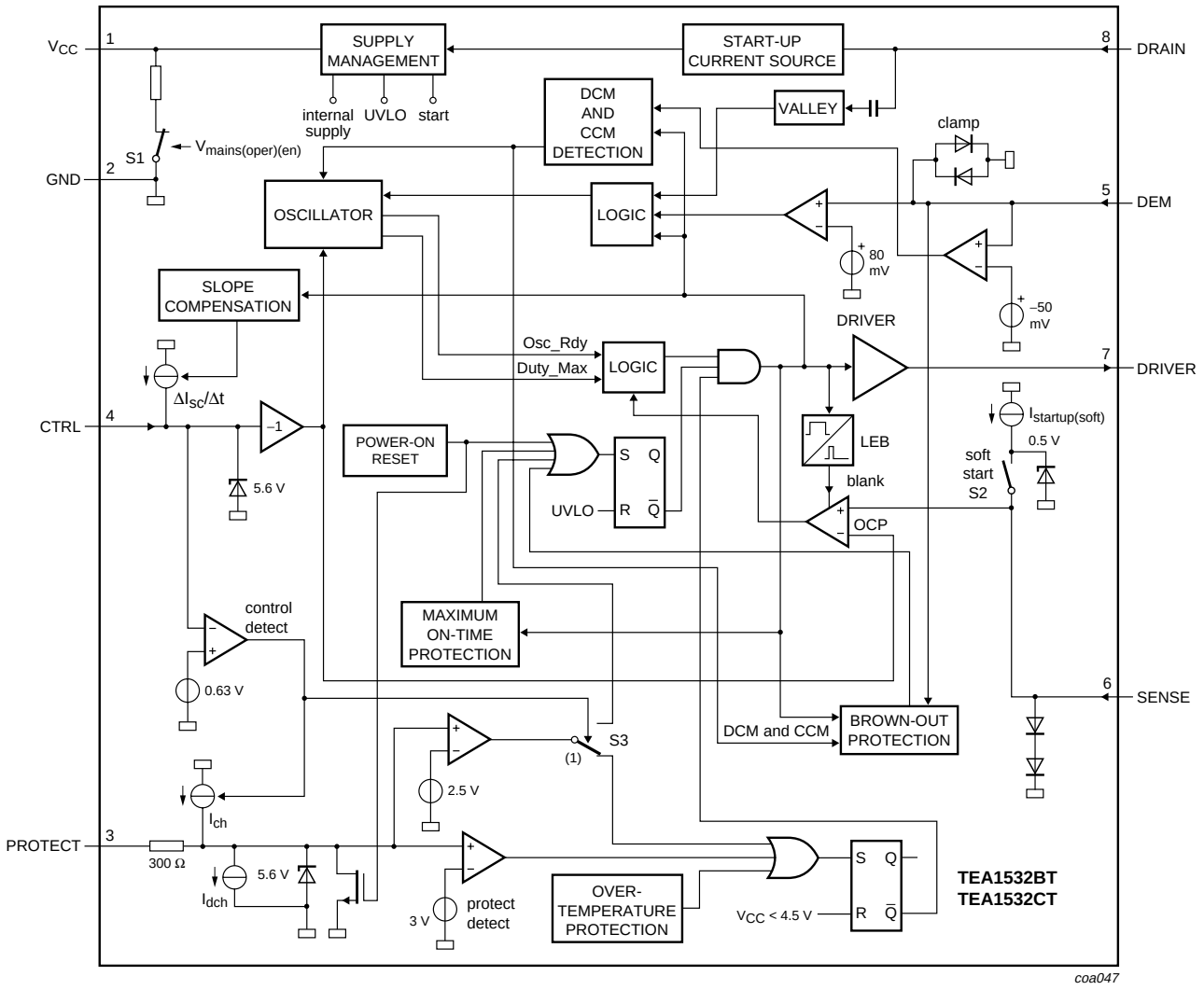
- Adapters and open frame flyback power supplies. The device can also be used in all applications that demand an efficient and cost-effective solution up to 250 W.

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TEA1532BT	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
TEA1532CT			

5. Block diagram



(1) Switch S3 is not controlled in the TEA1532BT (fixed as drawn).

Fig 1. Block diagram

6. Pinning information

6.1 Pinning

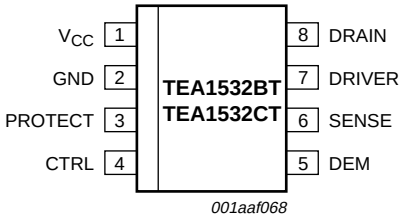


Fig 2. Pin configuration: TEA1532BT and TEA1532CT (SOT96-1)

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
V_{CC}	1	supply voltage
GND	2	ground
PROTECT	3	protection and timing input
CTRL	4	control input
DEM	5	input from auxiliary winding for demagnetization timing
SENSE	6	programmable current sense input
DRIVER	7	MOSFET gate driver output
DRAIN	8	drain of the external MOS switch, input for start-up current and valley sensing

7. Functional description

The TEA1532BT; TEA1532CT is a controller for a compact flyback converter with the IC situated on the primary side. An auxiliary winding of the transformer provides demagnetization detection and powers the IC after start-up; see Figure 3.

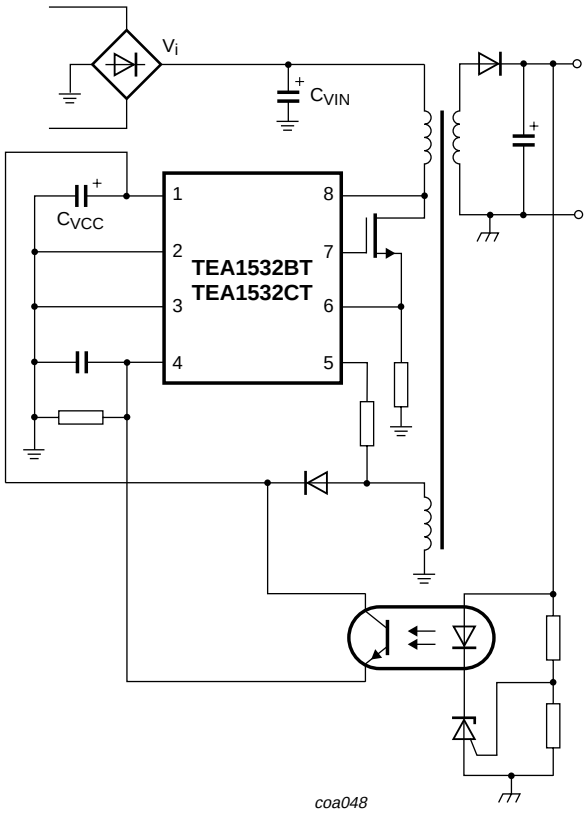


Fig 3. Basic configuration

The TEA1532BT; TEA1532CT can operate in multi modes; see Figure 4.

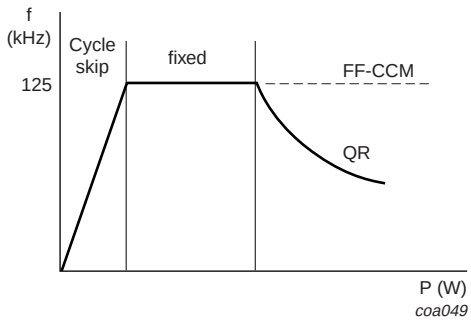


Fig 4. Multi mode and FF-CCM operation

In QR mode, the next converter stroke is started only after demagnetization of the transformer current (zero current switching), while the drain voltage has reached the lowest voltage to minimize switching losses (green function). The primary resonant circuit of primary inductance and drain capacitor ensures this quasi-resonant operation. The design can be optimized in such a way that zero voltage switching can extend over most of the universal mains range.

To prevent very high frequency operation at lower loads, the quasi-resonant operation changes smoothly in fixed frequency Pulse Width Modulation (PWM) control.

In fixed frequency continuous conduction mode, which can be activated by grounding pin DEM, the internal oscillator determines the start of the next converter stroke.

In both operating modes, a cycle skipping mode is activated at very low power (standby) levels.

7.1 Start-up, mains enabling operation level and undervoltage lock out

Refer to Figure 9 and Figure 10. Initially, the IC is self supplying from the rectified mains voltage via pin DRAIN. Supply capacitor C_{VCC} (at pin 1) is charged by the internal start-up current source to a level of about 4 V or higher, depending on the drain voltage. Once the drain voltage exceeds the $V_{mains(oper)(en)}$ (mains-dependent operation-enabling level), the start-up current source will continue charging capacitor C_{VCC} (switch S1 will be opened); see Figure 1. The IC will activate the power converter as soon as the voltage on pin V_{CC} passes the $V_{startup}$ level. At this moment the IC supply from the high voltage pin is stopped (green function). The IC supply is taken over by the auxiliary winding of the flyback converter.

The moment the voltage on pin V_{CC} drops below $V_{th(UVLO)}$ (undervoltage lock out), the IC stops switching and performs a safe restart from the rectified mains voltage. In the safe restart mode the driver output is disabled and pin V_{CC} voltage is recharged via pin DRAIN.

7.2 Supply management

All (internal) reference voltages are derived from a temperature compensated, on-chip band gap circuit.

7.3 Oscillator

The fixed frequency of the oscillator is set by an internal current source and capacitor.

7.4 Cycle skipping

At very low power levels a cycle skipping mode activates. An internal control voltage ($V_{sense(max)}$) lower than 25 mV will inhibit switch-on of the external power MOSFET until this voltage increases to a higher value; see Figure 5.

7.5 Current control mode

Current control mode is used for its good line regulation behavior.

The primary current is sensed across an external resistor and compared with the internal control voltage. The driver output is latched in the logic, preventing multiple switch-on.

The internal control voltage is inversely proportional to the external pin CTRL voltage, with an offset of 1.5 V. This means that a voltage range from 1 V to approximately 1.5 V on pin CTRL will result in an internal control voltage range from 0.5 V to 0 V (a high external control voltage results in a low duty cycle).

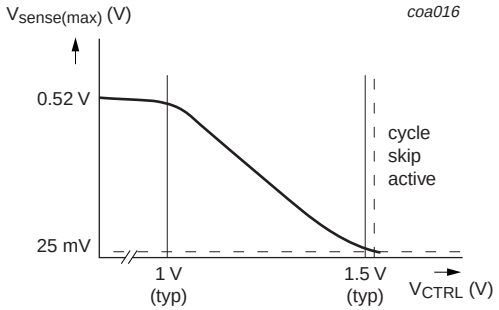


Fig 5. The $V_{sense(max)}$ voltage as a function of V_{CTRL}

7.6 OverCurrent Protection (OCP)

The primary peak current in the transformer is measured accurately cycle-by-cycle using the external sense resistor R_{sense}. The OCP circuit limits the voltage on pin SENSE to an internal level equal to 1.5 V − V_{CTRL} (see also Section 7.5). The OCP detection is suppressed during the leading edge blanking period, t_{leb}, to prevent false triggering caused by the switch-on spikes.

7.7 Demagnetization (QR operation)

The system will be in Discontinuous Conduction Mode (DCM) (QR operation) when resistor R_{DEM} is applied. The oscillator will not start a new primary stroke until the previous secondary stroke has ended.

Demagnetization features a cycle-by-cycle output short-circuit protection, which immediately reduces the frequency (longer off-time), thereby reducing the power level.

Demagnetization recognition is suppressed during the first $t_{sup(xfmr\_ring)}$ time (typical 1.5 µs). This suppression may be necessary in applications where the transformer has a large leakage inductance and at low output voltages or start-up.

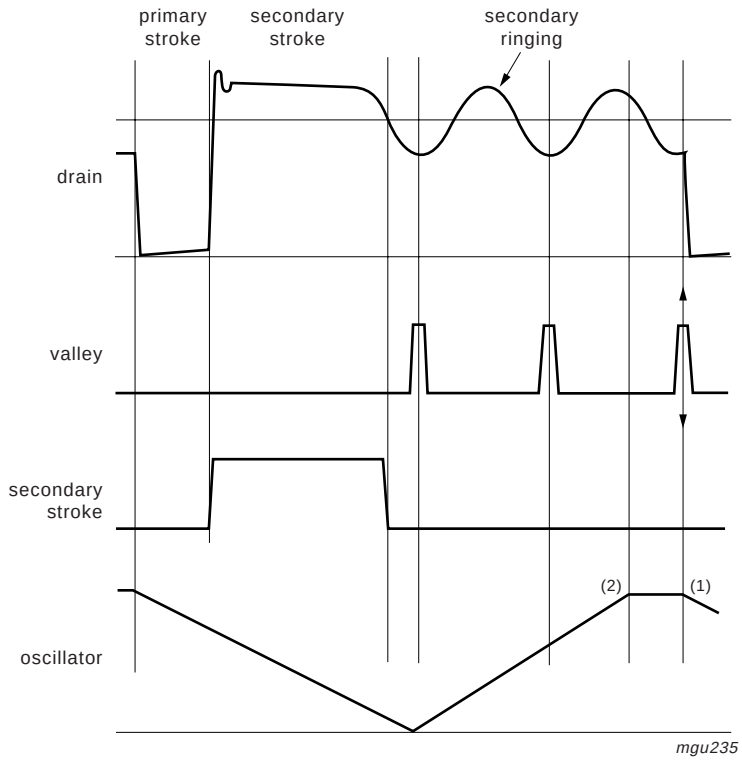
7.8 Valley switching

Refer to Figure 6. A new cycle starts when the power switch is activated. After the on-time (determined by the sense voltage and the internal control voltage), the switch is opened and the secondary stroke starts. After the secondary stroke, the drain voltage shows an oscillation with a frequency of approximately $\frac{1}{2 \times \pi \times \sqrt{L_p \times C_d}}$

where L_p is the primary self inductance of the transformer and C_d is the capacitance on the drain node.

As soon as the oscillator voltage is high again and the secondary stroke has ended, the circuit waits for the lowest drain voltage before starting a new primary stroke. This method is called valley detection. Figure 6 shows the drain voltage, valley signal, secondary stroke signal and the oscillator signal.

In an optimum design, the reflected secondary voltage on the primary side will force the drain voltage to zero. Thus, zero voltage switching is possible, preventing large capacitive switching losses $\left(P = \frac{1}{2} \times C \times V^2 \times f\right)$, and allowing high frequency operation, which results in small and cost-effective magnetics.



(1) Start of new cycle at lowest drain voltage.

(2) Start of new cycle in a classical PWM system at high drain voltage.

Fig 6. Signals for valley switching

7.9 Continuous Conduction Mode (CCM)

It is also possible to operate the IC in the so-called Fixed Frequency Continuous Conduction Mode (FF CCM). This mode is activated by connecting pin DEM to ground and connecting pin DRAIN to the rectified V_I voltage; see Figure 12.

7.10 Adjustable slope compensation

A slope compensation function has been added at pin CTRL; see Figure 7. The slope compensation function prevents sub-harmonic oscillation in CCM at duty cycles over 50 %. The CTRL voltage is modulated by sourcing a (non-constant) current out of pin CTRL and adding a series resistor $R_{slopecomp}$. This increases the CTRL voltage proportionally with the on-time, which therefore limits the OCP level. Thus, a longer on-time results in a higher CTRL voltage. However, this increase in CTRL voltage will actually decrease the on-time. Slope compensation can be adjusted by changing the

value of $R_{slopecomp}$. Slope compensation prevents modulation of the on-time (duty cycle) while operating in FF CCM. A possible drawback of sub-harmonic oscillation can be output voltage ripple.

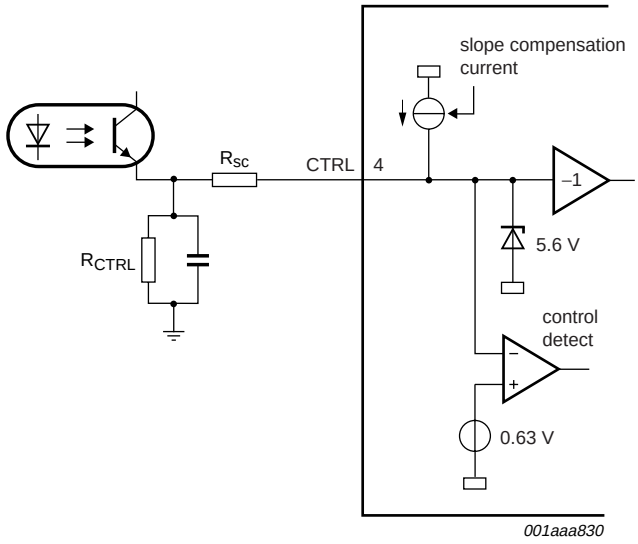


Fig 7. Slope compensation

7.11 Minimum and maximum on-time

The minimum on-time of the SMPS is determined by the Leading Edge Blinking (LEB) time (typically 400 ns). The IC limits the on-time to a maximum time, which is dependent on the mode of operation:

QR mode: When the system requires an ‘on-time’ of more than 25 µs, a fault condition is assumed (e.g. C_{VCC} removed). The IC stops switching and enters the safe restart mode.

CCM: The driver duty cycle is limited to 70 %. So the maximum on-time is correlated to the oscillator time, which results in an accurate limit of the minimum input voltage of the flyback converter.

7.12 Soft start-up (pin SENSE)

To prevent transformer rattle at start-up or during hiccup, the transformer peak current is slowly increased by the soft start function. This can be achieved by inserting a resistor and a capacitor between pin SENSE (pin 6) and sense resistor R_{sense}. An internal current source charges the capacitor to $V_{SENSE} = I_{startup(soft)} \times R_{ss}$ (about 0.5 V maximum).

The start level and the time constant of the increasing primary current level can be adjusted externally by changing the values of R_{ss} and C_{ss}.

$$I_{DM} = \frac{V_{sense(max)} - (I_{startup(soft)} \times R_{ss})}{R_{sense}}$$

$$\tau = R_{ss} \times C_{ss}$$

The charging current $I_{startup(soft)}$ will flow as long as the voltage on pin SENSE is below approximately 0.5 V. If the voltage on pin SENSE exceeds 0.5 V, the soft start current source will start limiting current $I_{startup(soft)}$. At $V_{startup}$, the $I_{startup(soft)}$ current source is completely switched off; see Figure 8.

Since the soft start current is supplied from pin DRAIN, the R_{ss} value will not affect V_{CC} current during start-up.

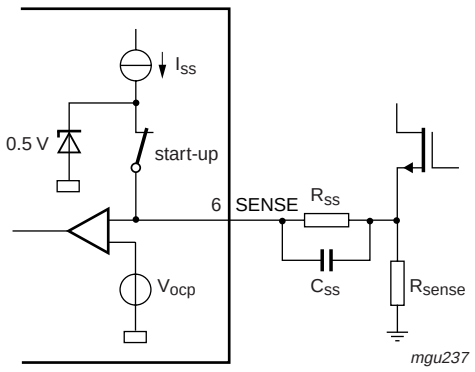


Fig 8. Soft start-up

7.13 Control pin protection

If the pin CTRL becomes open-circuit or is disconnected, a fault condition is assumed and the converter will stop switching immediately. Operation recommences when the fault condition is removed.

7.14 PROTECT and timing input

The PROTECT input (pin 3) is a multi-purpose (high-impedance) input, which can be used to switch off the IC and create a relatively long timing function. As soon as the voltage on this pin rises above 2.5 V, switching stops immediately. For the timing function, a current of typically 50 μA flows out of pin PROTECT and charges an external capacitor until the activation level of 2.5 V is reached. This current source is only activated when the converter is not in regulation, which is detected by the voltage on pin CTRL (V_{CTRL} < 0.63 V). A (small) discharge current is also implemented to ensure that the capacitor is not charged, for example, by spikes. A MOSFET switch is added to discharge the external capacitor and ensure a defined start situation. For the TEA1532CT, the voltage on pin CTRL determines whether the IC enters latched protection mode, or safe restart protection mode:

- When the voltage on pin CTRL is below 0.63 V, the IC is assumed to be out of regulation (e.g. the control loop is open). In this case activating pin PROTECT ($V_{PROTECT}$ > 2.5 V) will cause the converter to stop switching. Once V_{CC} drops below $V_{th(UVLO)}$, capacitor C_{VCC} will be recharged and the supply will restart. This cycle will be repeated until the fault condition is removed (safe restart mode).
- When the voltage on pin CTRL is above 0.63 V, the output is assumed to be in regulation. In this case activating pin PROTECT ($V_{PROTECT}$ > 2.5 V), by external means, will activate the latch protection of the IC: The voltage on pin V_{CC} will cycle between $V_{startup}$ and $V_{th(UVLO)}$, but the IC will not start switching again until the latch

protection is reset. The latch is reset as soon as V_{CC} drops below 4.5 V (typical value) (this only occurs when the mains has been disconnected). The internal overtemperature protection will also trigger this latch; see also Figure 1.

For the TEA1532BT the IC always enters the latched mode protection independent of the voltage on pin CTRL.

A voltage higher than 3 V on pin PROTECT will always latch the IC. This is independent of the state or the version of the IC.

7.15 OverTemperature Protection (OTP)

The IC provides accurate OTP. The IC will stop switching when the junction temperature exceeds the thermal shutdown temperature. When V_{CC} drops to $V_{th(UVLO)}$, capacitor C_{VCC} will be recharged to the $V_{startup}$ level, however switching will not restart. Subsequently, V_{CC} will drop again to $V_{th(UVLO)}$, etc.

Operation only recommences when V_{CC} drops below a level of about 4.5 V (typically, when V_{mains} is disconnected for a short period).

7.16 Brown-out protection

During the so called brown-out test, the input voltage is slowly decreased. Since the on-time depends on V_i, long on-times at low V_i can damage the (external) power device. This is prevented by stopping the converter when the input voltage drops too low.

When the voltage on pin DEM drops below –50 mV during the on-time (QR mode), the maximum on-time is set to 25 µs. The maximum on-time will be reached while V_i is low. Subsequently, the IC stops switching and V_{CC} drops below $V_{th(UVLO)}$. Capacitor C_{VCC} will only be recharged and the supply will restart only when voltage V_I is high enough ($V_{mains(oper)(en)}$, also see Section 7.1). In addition to this, a V_I level at which the converter has to enter a safe restart can be set with a demagnetization resistor. During the primary stroke, the rectified mains input voltage is measured by sensing the current drawn from pin DEM. This current depends on the mains voltage, according to the following equation:

$$I_{DEM} \approx \frac{V_{aux}}{R_{DEM}} \approx \frac{N \times V_{mains}}{R_{DEM}}$$

Where: $N = \frac{N_{aux}}{N_p}$ (ratio of the number of auxiliary to the number of primary windings)

The latter function requires an on-time of at least 2 µs. This on-time ensures that a reliable demagnetization current can be measured.

When pin DEM is grounded (CCM), the brown-out protection is disabled. In this case the duty cycle is limited to 0.7, so at low mains voltage the on-time is limited and therefore the dissipation in the FET is limited.

7.17 Driver

The driver circuit to the gate of the power MOSFET has a current sourcing capability of typically 170 mA and a current sink capability of typically 700 mA. This permits fast turn-on and turn-off of the power MOSFET for efficient operation.

A low driver source current has been chosen to limit the $\Delta V/\Delta t$ at switch-on. This reduces ElectroMagnetic Interference (EMI) and also limits the current spikes across R_{sense}.

8. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Voltages						
V_{CC}	supply voltage	continuous		–0.4	+20	V
$V_{PROTECT}$	voltage on pin PROTECT	continuous		–0.4	+5	V
V_{CTRL}	voltage on pin CTRL			–0.4	+5	V
V_{DEM}	voltage on pin DEM	current limited		-	-	V
V_{SENSE}	voltage on pin SENSE	current limited		–0.4	-	V
V_{DRAIN}	voltage on pin DRAIN			–0.4	+650	V
Currents						
I_{CTRL}	current on pin CTRL	d < 10 %		-	50	mA
I_{DEM}	current on pin DEM			–1000	+250	µA
I_{SENSE}	current on pin SENSE			–1	+10	mA
I_{DRIVER}	current on pin DRIVER	d < 10 %		–0.8	+2	A
I_{DRAIN}	current on pin DRAIN			-	5	mA
General						
P_{tot}	total power dissipation	T_{amb} < 70 °C		-	0.5	W
T_{stg}	storage temperature			–55	+150	°C
T_j	junction temperature			–20	+145	°C
ESD						
V_{ESD}	electrostatic discharge voltage	class 1				
	human body model	pins 1 to 7	[1]	-	2000	V
		pin 8 (DRAIN)	[1]	-	1500	V
	machine model		[2]	-	200	V

[1] Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[2] Equivalent to discharging a 200 pF capacitor through a 0.75 µH coil and a 10 Ω resistor.

9. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	150	K/W

10. Characteristics

Table 5. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Start-up current source (pin DRAIN)						
I_{DRAIN}	current on pin DRAIN	V_{DRAIN} > 100 V				
		V_{CC} = 0 V	1.0	1.2	1.4	mA
		with auxiliary supply	-	100	300	µA
V_{BR}	breakdown voltage		650	-	-	V
$V_{mains(oper)(en)}$	mains-dependent operation-enabling voltage		60	-	100	V
Supply voltage management (pin V_{CC})						
$V_{startup}$	start-up voltage		10.3	11	11.7	V
$V_{th(UVLO)}$	undervoltage lockout threshold voltage		8.1	8.7	9.3	V
V_{hys}	hysteresis voltage	$V_{startup} - V_{th(UVLO)}$	2.0	2.3	2.6	V
$I_{ch(high)}$	high charging current	V_{DRAIN} > 100 V; V_{CC} < 3 V	–1.2	–1	–0.8	mA
$I_{ch(low)}$	low charging current	V_{DRAIN} > 100 V; 3 V < V_{CC} < $V_{th(UVLO)}$	–1.2	–0.75	–0.45	mA
$I_{restart}$	restart current	V_{DRAIN} > 100 V; $V_{th(UVLO)}$ < V_{CC} < $V_{startup}$	–650	–550	–450	µA
$I_{CC(oper)}$	operating supply current	no load on pin DRIVER	1.1	1.3	1.5	mA
Demagnetization management (pin DEM)						
$V_{th(DEM)}$	threshold voltage on pin DEM		50	80	110	mV
$V_{th(det)(CCM)}$	continuous conduction mode detection threshold voltage		–80	–50	–20	mV
$V_{CL(neg)}$	negative clamp voltage	I_{DEM} = –500 µA	–0.5	–0.45	–0.40	V
$V_{CL(pos)}$	positive clamp voltage	I_{DEM} = 250 µA	0.5	0.7	0.9	V
$t_{sup(xfmr\_ring)}$	transformer ringing suppression time	at start of secondary stroke	1.1	1.5	1.9	µs
Pulse width modulator						
$t_{on(min)}$	minimum on-time		-	t_{leb}	-	ns
$t_{on(max)}$	maximum on-time	QR mode	20	25	30	µs
δ_{max}	maximum duty cycle		67	70	73	%
Oscillator						
f_{osc}	oscillator frequency	V_{CTRL} < 1 V	100	125	150	kHz

Table 5. Characteristics *...continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Duty cycle control (pin CTRL)							
$V_{min(\delta max)}$	minimum voltage (maximum duty cycle)			-	1.0	-	V
$V_{max(\delta min)}$	maximum voltage (minimum duty cycle)			-	1.5	-	V
$\Delta I_{sc}/\Delta t$	slope compensation current			–1.2	–1	–0.8	µA/µs
$V_{CTRL(detect)}$	detection voltage on pin CTRL			0.56	0.63	0.70	V
Protection and timing input (pin PROTECT)							
V_{trip}	trip voltage		[1]	2.37	2.5	2.63	V
$V_{trip(latch)}$	latch trip voltage			2.85	3	3.15	V
$V_{VCC(latch)(reset)}$	latch reset voltage on pin VCC	$V_{PROTECT}$ < 2.3 V		-	4.5	-	V
I_{ch}	charge current	V_{CTRL} < 0.63 V		–57	–50	–43	µA
I_{dch}	discharge current			-	100	-	nA
Valley switch (pin DRAIN)							
$(\Delta V/\Delta t)_{vrec}$	valley recognition voltage change with time			–43	-	+43	V/µs
$t_{d(vrec\text{-}swon)}$	valley recognition to switch-on delay time		[2]	-	150	-	ns
Overcurrent and winding short-circuit protection (pin SENSE)							
$V_{sense(max)}$	maximum sense voltage	$\Delta V/\Delta t$ = 0.1 V/µs		0.48	0.52	0.56	V
t_{PD}	propagation delay	$\Delta V/\Delta t$ = 0.5 V/µs		-	140	185	ns
t_{leb}	leading edge blanking time			330	400	470	ns
$I_{startup(soft)}$	soft startup current	V_{SENSE} < 0.5 V		45	60	75	µA
Brown-out protection (pin DEM)							
$I_{prot(bo)}$	brownout protection current	A constant $I_{prot(bo)}$ is drawn from pin DEM.	[3]	–68	–60	–52	µA
$t_{en(prot)bo}$	brownout protection enable time			1.5	2	2.5	µs

Table 5. Characteristics *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Driver (pin DRIVER)						
I_{source}	source current	V_{CC} = 9.5 V; V_{DRIVER} = 2 V	-	–170	–88	mA
I_{sink}	sink current	V_{CC} = 9.5 V				
		V_{DRIVER} = 2 V	-	300	-	mA
		V_{DRIVER} = 9.5 V	400	700	-	mA
$V_{o(max)}$	maximum output voltage	V_{CC} > 12 V	-	11.5	12	V
Temperature protection						
$T_{pl(max)}$	maximum protection level temperature		130	140	150	°C
$T_{pl(hys)}$	protection level hysteresis temperature	V_{CC} > 2 V	-	8	-	°C

[1] TEA1532CT: safe restart; TEA1532BT: latch.

[2] Guaranteed by design.

[3] V_i detection level. Set by the demagnetization resistor R_{DEM}; see Section 7.16.

11. Application information

A converter with the TEA1532BT; TEA1532CT consists of an input filter, a transformer with a third winding (auxiliary), and an output stage with a feedback circuit.

Capacitor C_{VCC} buffers the IC supply voltage, which is powered via the internal current source, that is connected to the rectified mains during start-up and, via the auxiliary winding, during operation.

A sense resistor R_{sense} converts the primary current into a voltage at pin SENSE. The value of R_{sense} defines the maximum primary peak current.

Figure 9 shows a flyback configuration using the discontinuous conduction mode. Pin PROTECT is used in this example for external overvoltage protection and open loop or output short-circuit protection. If this pin is not used, it must be tied to ground. Figure 12 shows a flyback configuration using the continuous conduction mode. The pin PROTECT is used in this example for external overtemperature protection and open loop or output short-circuit protection.

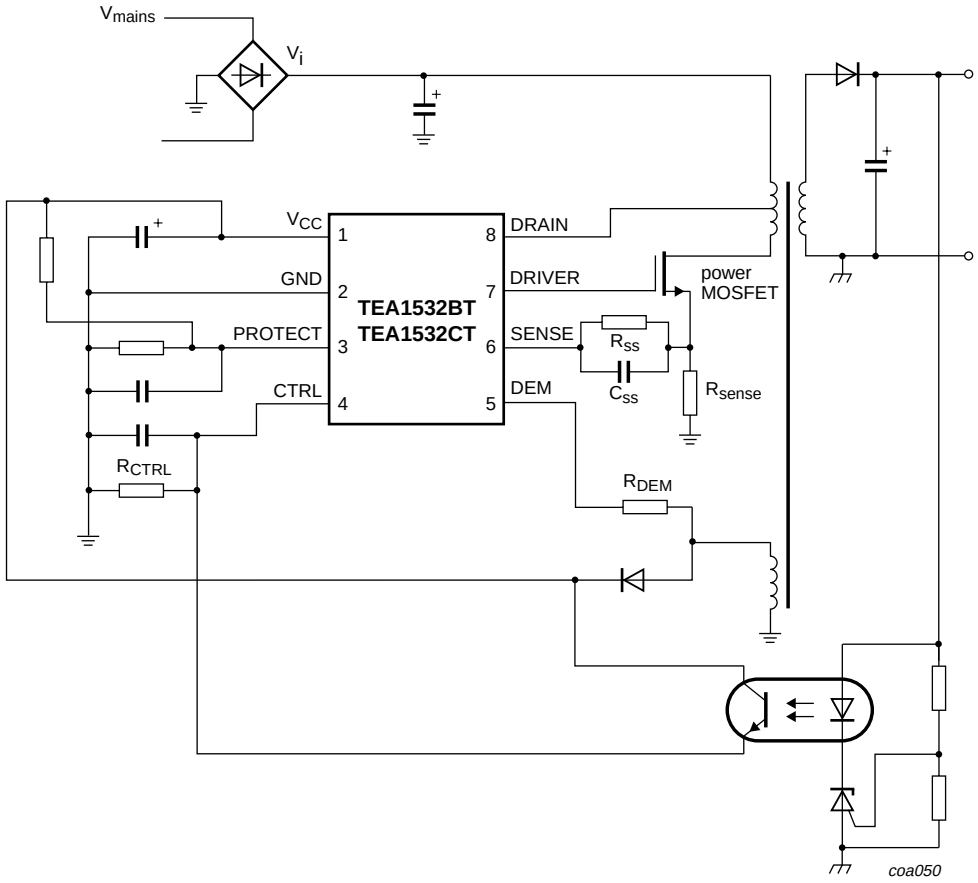
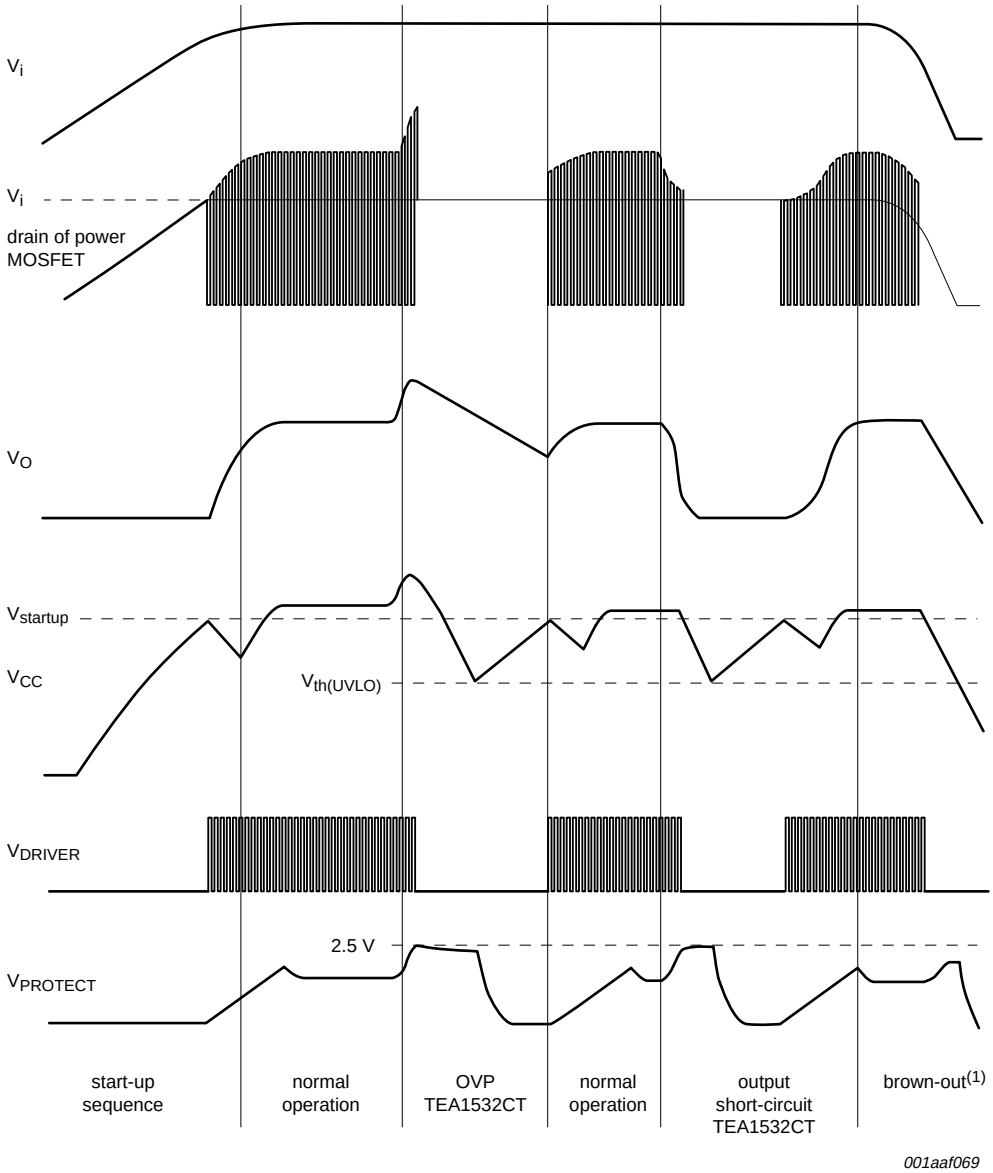
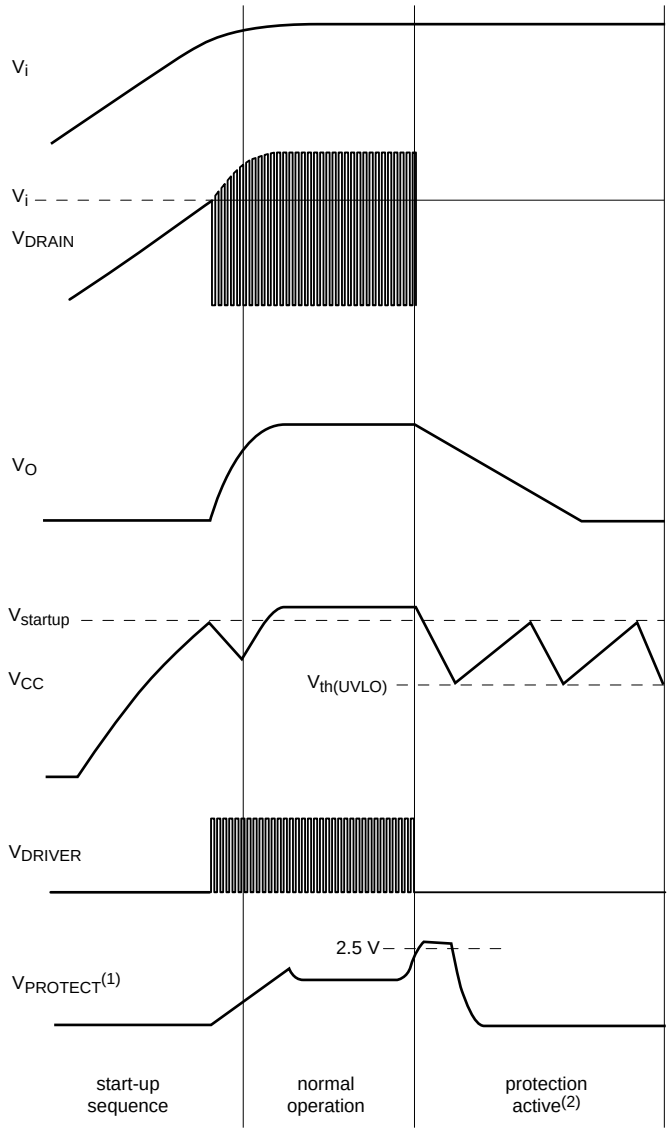


Fig 9. Flyback configuration using the discontinuous conduction mode



(1) In CCM, the brown-out protection is implemented by the maximum duty cycle in combination with pin PROTECT.

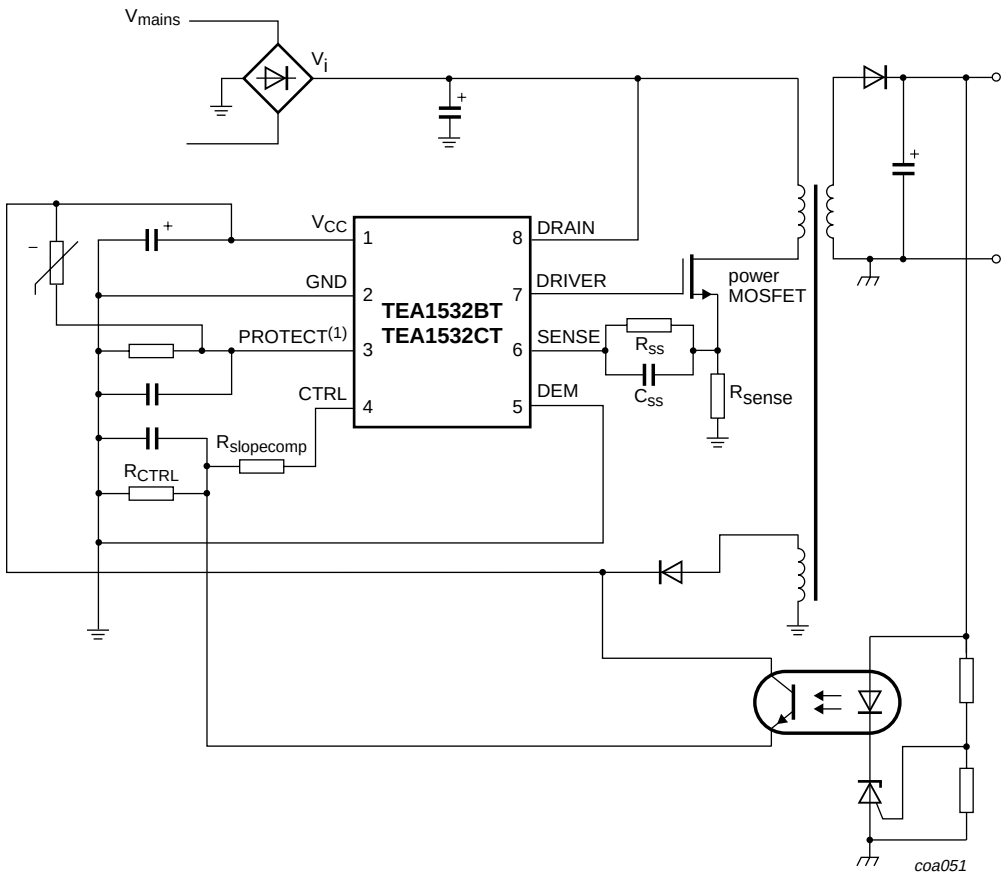
Fig 10. Typical waveforms 1



(1) When $V_{PROTECT}$ is forced above 3 V, the protection is always latched. So the IC is not started at $V_{startup}$ unless the V_{CC} voltage drops below the $V_{VCC(latch)(reset)}$ level. This is the same action used for external OTP compensation described in Section 7.15.

(2) External OTP for TEA1532BT and TEA1532CT; OVP and output short circuit for TEA1532BT.

Fig 11. Typical waveforms 2



(1) The pin PROTECT is used in this example for external OTP and open loop or output short-circuit protection. Slope compensation is determined by the value of $R_{slopecomp}$.

Fig 12. Flyback configuration using the continuous conduction mode

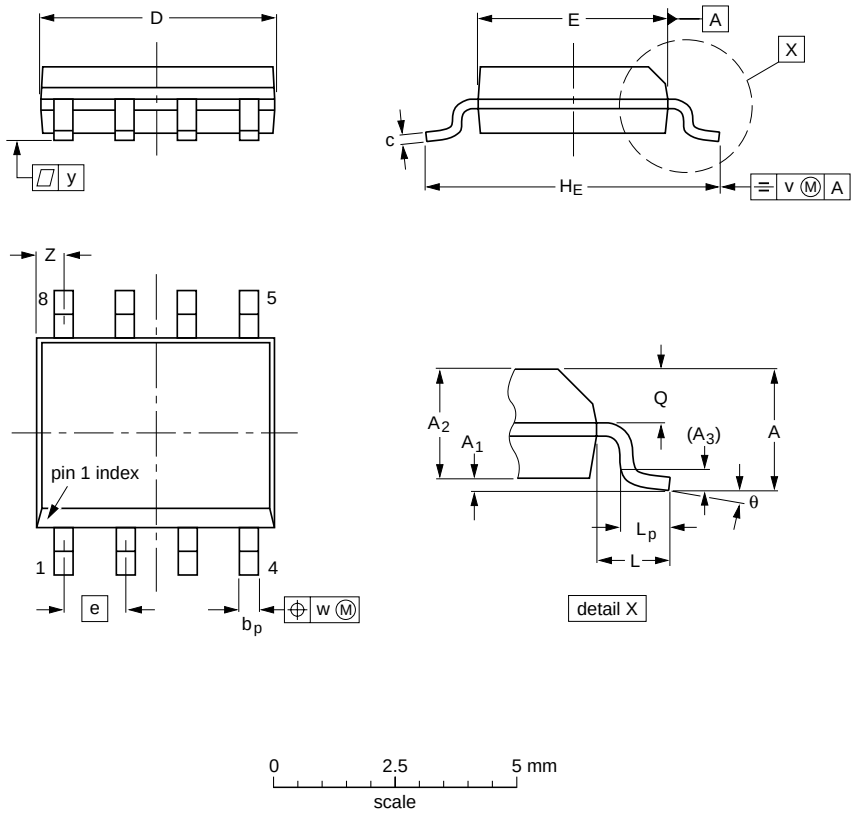
12. Test information

12.1 Quality information

The *General Quality Specification for Integrated Circuits, SNW-FQ-611* is applicable.

13. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 13. Package outline SOT96-1 (SO8)

14. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TEA1532BT_TEA1532CT_1	20070118	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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17. Contents

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Date of release: 18 January 2007

Document identifier: TEA1532BT_TEA1532CT_1