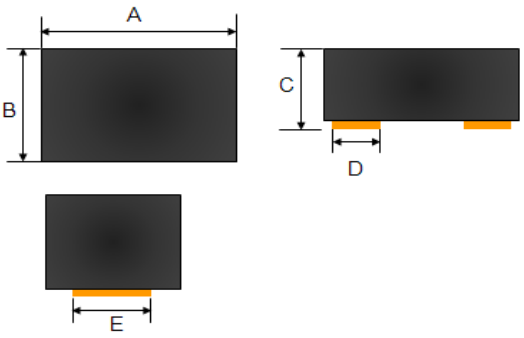
TAIWAN SEMICONDUCTOR

TESDQ5V0
Bi-directional ESD Protection Diode

Small Signal Diode

DFN1006 (0402)



Features

✧Meet IEC61000-4-2 (ESD) ±15kV (air), ±8kV (contact)
✧Meet IEC61000-4-4 (EFT) rating. 40A (5/50ńs)
✧100W Peak Pulse Power per Line (tp=8/20μs)
✧Protects one birectional I/O line
✧Working Voltage : 5V
✧Pb free version, RoHS compliant, and Halogen free

Mechanical Data

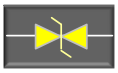
✧Case : DFN1006(0402) 1.0mm x 0.6mm x 0.5mm package, molded plastic
✧Molding Compound Flammability Ratting: UL94V-0
✧Terminal: Gold plated,solder per MIL-STD-750, Method 2026 guaranteed
✧High temperature soldering guaranteed: 260℃/10s
✧Mounting position: Any
✧Weight :0.5 mg (approximately)
✧Marking Code : M

Dimensions	Unit (mm)		Unit (inch)	
	Min	Max	Min	Max
A	0.950	1.050	0.037	0.041
B	0.550	0.650	0.022	0.026
C	0.450	0.550	0.018	0.022
D	0.275	0.325	0.011	0.013
E	0.275	0.325	0.011	0.013

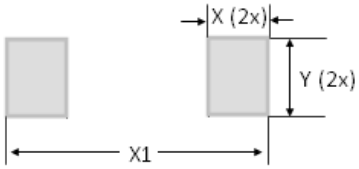
Applications

✧Cell Phone Handsets and Accessories
✧Notebooks, Desktops, and Servers
✧Keypads, Side Keys, LCD Displays
✧Portable Instrumentation
✧Touch panel

Pin Configutation



Suggested PAD Layout



Dimensions	Value (in mm)
X	0.354
X1	1.110
Y	0.354

rdering Information

Part No.	Package	Packing	Packing Code	Marking
TESDQ5V0	0402	5K / 7" Reel	RJG	M

Maximum Ratings and Electrical Characteristics

Rating at 25°C ambient temperature unless otherwise specified.

Maximum Ratings

Type Number	Symbol	Value	Units
Peak Pulse Power (tp=8/20μs waveform)	P_{PP}	100	W
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	±30 ±8	KV
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to + 150	°C

Electrical Characteristics

Type Number		Symbol	Min	Max	Units
Reverse Stand-Off Voltage		V_{RWM}	-	5	V
Reverse Breakdown Volt	I_R= 1mA	$V_{(BR)}$	6	-	V
Reverse Leakage Curren	V_R= 5V	I_R	-	1	uA
Clamping Voltage	I_{PP}= 1A	Vc	-	12.5	V
	I_{PP}= 2A		-	20	
Junction Capacitance	V_R=0V, f=1.0MHz	C_J	10 (Typ.)		pF

Notes: 1. The suggested land pattern dimensions have been provided for reference only, as actual pad layouts may vary despending on application.

Small Signal Diode

Rating and Characteristic Curves

FIG 1 Admissible Power Derating Curve

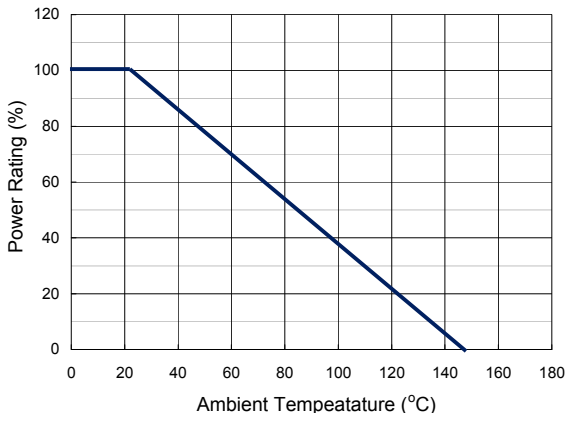


FIG 2 Pulse Waveform

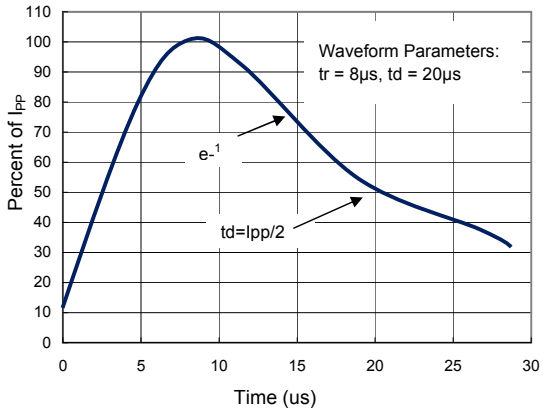


FIG 3 Max. Clamping Voltage vs. Peak Pulse

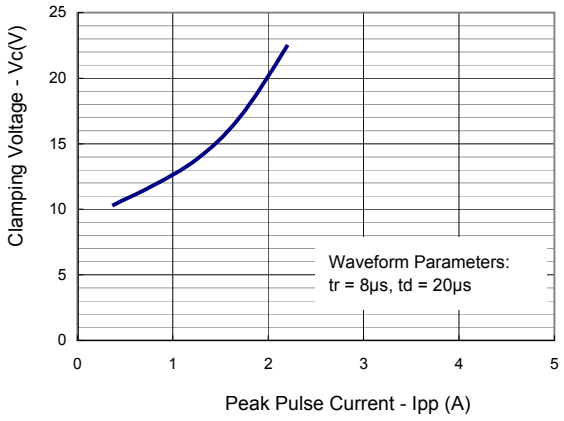
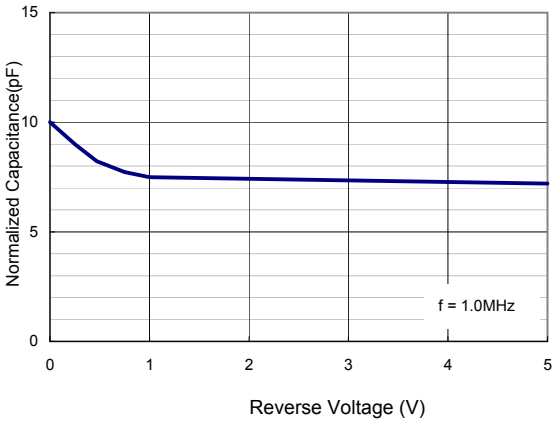


FIG 4 Typical Junction Capacitance



Applications Information

✧Designed to protect one data, I/O, or power supply line.
✧Designed to protect sensitive electronics from damage or latch-up due to ESD
✧Designed to replace multilayer varistors (MLVs) in portable applications
✧Features large crosssectional area junctions for conducting high transient currents
✧Offers superior electrical characteristics such as lower clamping voltage and no device degradation when compared to MLVs
✧The combination of small size and high ESD surge capability makes them ideal for use in portable applications.

Circuit Board Layout Recommendations

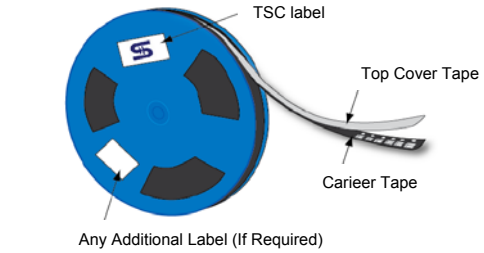
Good circuit board layout is critical for the suppression of ESD induced transients.
✧Place the ESD Protection Diode near the input terminals or connectors to restrict transient
✧Minimize the path length between the ESD Protection Diode and the protected line.
✧Minimize all conductive loops including power and ground loops.
✧The ESD transient return path to ground should be kept as short as possible.
✧Never run critical signals near board edges.
✧Use ground planes whenever possible.

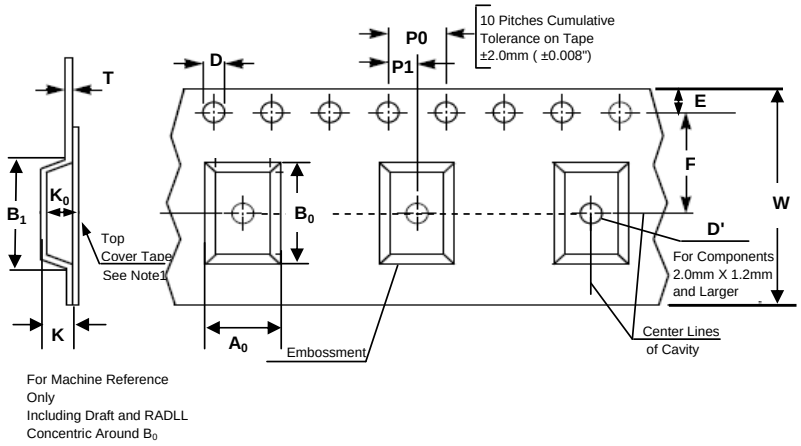
TAIWAN SEMICONDUCTOR

TESDQ5V0
Bi-directional ESD Protection Diode

Small Signal Diode

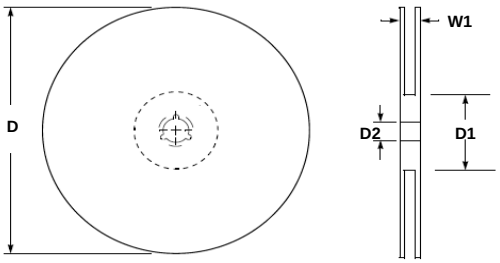
Carrier & Reel specification

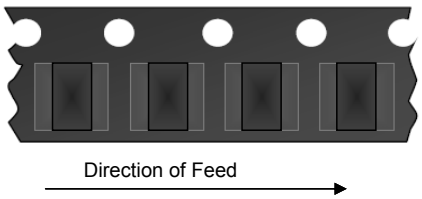




For Machine Reference
Only
Including Draft and RADLL
Concentric Around B_0

Item	Symbol	Dimension(mm)
Carrier depth	K	1.2 Max.
Sprocket hole	D	1.50 +0.10
Reel outside diameter	A	178 ± 1
Reel inner diameter	D1	50 Min.
Feed hole width	D2	13.0 ± 0.5
Sprocke hole position	E	1.75 ±0.10
Sprocke hole pitch	P0	4.00 ±0.10
Embossment center	P1	2.00 ±0.10
Overall tape thickness	T	0.6 Max.
Tape width	W	8.30 Max.
Reel width	W1	14.4 Max.





Note 1: A_0, B_0, and K_0 are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min. to 0.1 mm max. The component cannot rote more than 10o within the determined cavity.

Note 2: If B1 exceeds 4.2 mm(0.165") for 8 mm embossed tape, the tape may not feed through all tape feeders.