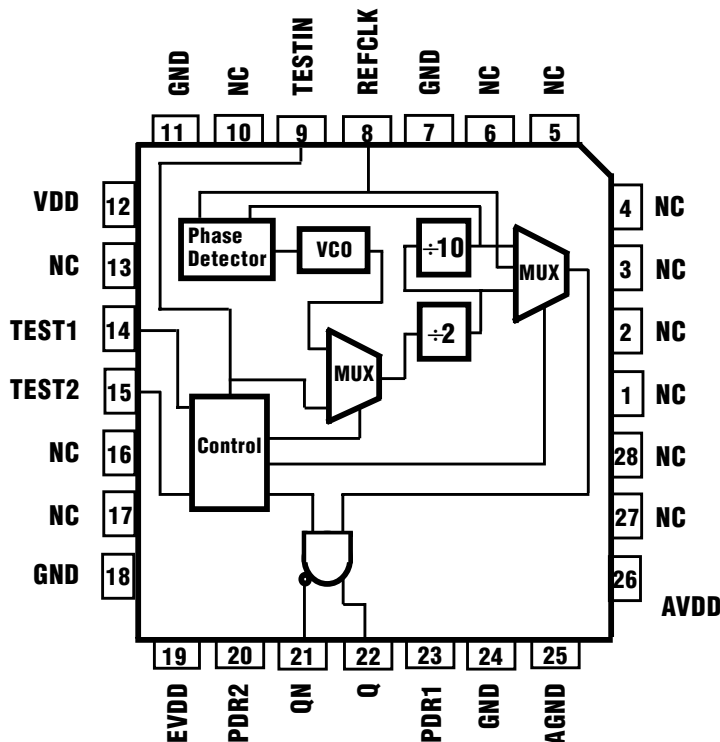


Figure 1. Pinout Diagram



TriQuint's TQ2059 is a high-frequency clock generator. It utilizes a 20 MHz to 35 MHz TTL input to generate a 200 MHz to 350 MHz PECL output. The TQ2059 has a completely self-contained Phase-Locked Loop (PLL) running at 400 MHz to 700 MHz. This stable PLL allows for a low period-to-period output jitter of 120 ps (max), and enables tight duty-cycle control of 55% to 45% (worst case).

The TQ2059 provides optional 200-ohm on-chip pull-down resistors which are useful if the output is AC-coupled to the device being driven. In order to use these resistors, pin 20 (PDR2) should be connected to pin 21 (QN), and pin 23 (PDR1) should be connected to pin 22 (Q).

Various test modes on the chip simplify debug and testing of systems by slowing the clock output or by bypassing the PLL.

TQ2059

High-Frequency Clock Generator

Features

- Output frequency range: 200 MHz to 350 MHz
- One differential PECL output: 600 mV (min) swing
- Common-mode voltage: $V_{DD} - 1.2 V$ (max), $V_{DD} - 1.6 V$ (min)
- Period-to-period output jitter: 30 ps peak-to-peak (typ), 120 ps peak-to-peak (max)
- Reference clock input: 20 MHz to 35 MHz TTL-level crystal oscillator
- Self-contained loop filter
- Optional 200-ohm pull-down resistors for AC-coupled outputs
- +5 V power supply
- 28-pin J-lead surface-mount package
- Ideal for designs based on DEC Alpha AXP™ processors

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Figure 2. Simplified Block Diagram

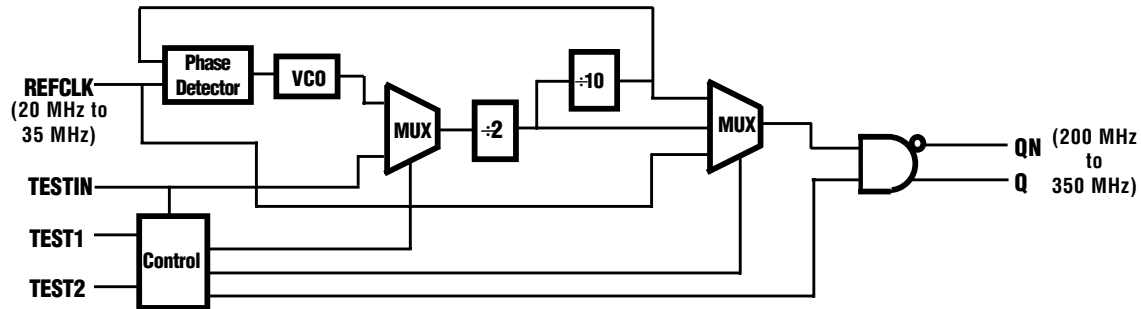


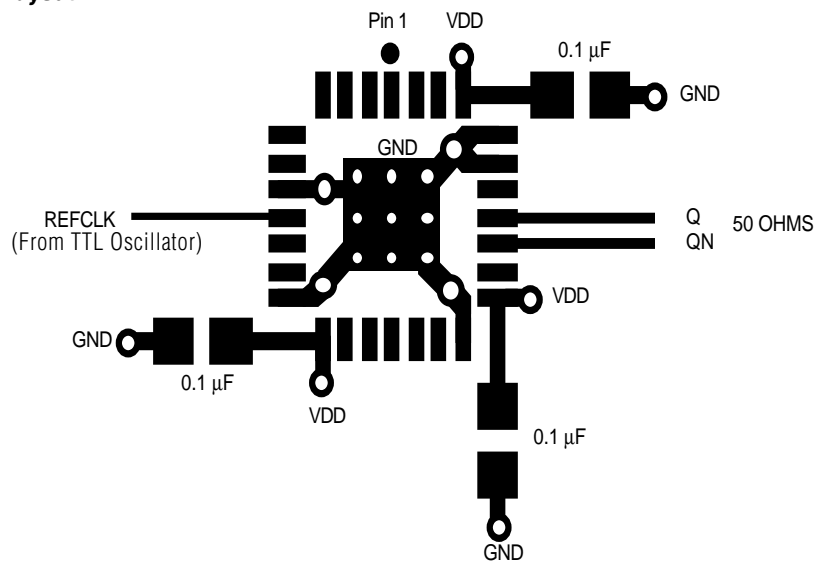
Table 1. Mode Selection

Mode	TEST1	TEST2	TESTIN ¹	REFCLK ²	Q, QN
1 (Test)	0	0	f _{TESTCLK}	"don't care"	f _{TESTCLK} ÷ 20
2 (Test)	0	1	"don't care"	"don't care"	0, 1
3 (Test)	1	0	f _{TESTCLK}	"don't care"	f _{TESTCLK} ÷ 2
4 (Bypass)	1	1	0	f _{REFCLK}	f _{REFCLK}
5 (Normal)	1	1	1	f _{REFCLK}	10 x f _{REFCLK} ³

Note: 1. In modes 1 and 3, TESTIN may be used to bypass the PLL. A clock input at TESTIN will be divided as shown.
 2. REFCLK = 20 MHz to 35 MHz.
 3. Q, QN = 200 MHz to 350 MHz.

Recommended Layout

(Not to scale)



Absolute Maximum Ratings

Storage Temperature	-65°C to +150°C
Ambient temperature with power applied	-55°C to +110°C
Supply voltage to ground potential	-0.5 V to +7.0 V
DC input voltage	-0.5 V to (V _{DD} + 0.5) V
DC input current	-30 mA to +5 mA
Package thermal resistance (MQuad)	θ _{JA} = 45°C/W
Die junction temperature	T _J = 150°C

Note: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. The device should be operated only under the DC and AC conditions shown below.

DC Characteristics (V_{DD} = +5 V ± 5%, T_A = 0 °C to +70 °C)¹

Symbol	Description	Test Conditions	Limits ¹			Unit
			Min	Typ	Max	
V _{OH}	Output HIGH voltage	V _{CC} = Min PECL load	V _{CC} -1.20		V _{CC} -0.50	V
V _{OL}	Output LOW voltage	V _{CC} = Min PECL load	V _{CC} -2.00		V _{CC} -1.60	V
V _{CMO}	Output common mode voltage	PECL	V _{CC} -1.60		V _{CC} -1.20	V
Δ V _{OUT}	Output differential voltage	PECL	0.6		1.2	V
V _{IH} ²	Input HIGH level	Guaranteed input logical HIGH Voltage for all inputs	2.0			V
V _{IL} ²	Input LOW level	Guaranteed input logical LOW Voltage for all inputs			0.8	V
I _{IL}	Input LOW current	V _{DD} = Max V _{IN} = 0.40 V		-150	-400	μA
I _{IH}	Input HIGH current	V _{DD} = Max V _{IN} = 2.7 V		0	25	μA
I _I	Input HIGH current	V _{DD} = Max V _{IN} = 5.3 V		2	1000	μA
I _{DDS} ³	Power supply current	V _{DD} = Max		85	120	mA
V _I	Input clamp voltage	V _{DD} = Min I _{IN} = -18 mA		-0.70	-1.2	V

Capacitance

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
C _{IN}	Input Capacitance	V _{IN} = 2.0 V at f = 1 MHz		6		pF
C _{OUT}	Output Capacitance	V _{OUT} = 2.0 V at f = 1 MHz		9		pF

Notes: 1. Typical limits are at V_{DD} = 5.0 V and T_A = 25°C.

2. These are absolute values with respect to device ground and include all overshoots due to system or tester noise.

3. This parameter is measured with device not switching and unloaded.

TQ2059

AC Characteristics ($V_{DD} = +5\text{ V} \pm 5\%$, $T_A = 0^\circ\text{C to } +70^\circ\text{C}$)

Symbol	Input Clock (REFCLK)	Test Conditions	Min	Typ	Max	Unit
t_{CPWH}	CLK pulse width HIGH	Figure 2	4	—	—	ns
t_{CPWL}	CLK pulse width LOW	Figure 2	4	—	—	ns
t_{IR}	Input rise time (0.8 V – 2.0 V)		—	—	2.0	ns

Symbol	Input Clock (REFCLK)	Test Conditions	Min	Typ	Max	Unit
t_{OR}, t_{OF}	Rise/fall time (20% – 80%)	Figure 2	100	220	350	ps
t_{CYC}	Duty-cycle	Figure 2	45	50	55	%
t_{JP}^2	Period-to-Period Jitter		—	30	120	ps
t_{SYNC}^3	Synchronization Time		—	10	500	μs

- Notes: 1. All measurements are tested with a REFCLK having a rise time of 0.5 ns (0.8 V to 2.0 V).
 2. Jitter specification is peak to peak. Period-to-Period jitter is the jitter on the output with respect to the output's previous crossing.
 3. t_{SYNC} is the time required for the PLL to synchronize and assumes the presence of a CLK signal.

Figure 1

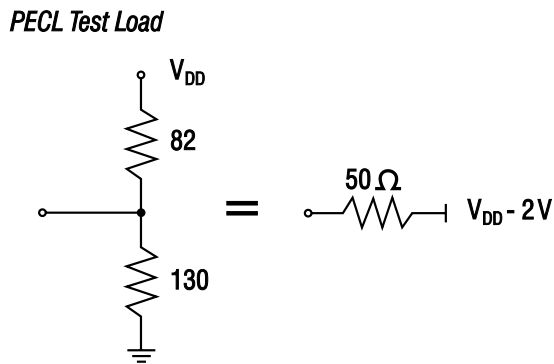
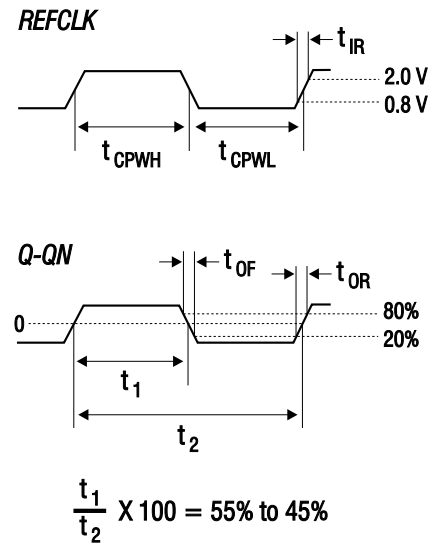
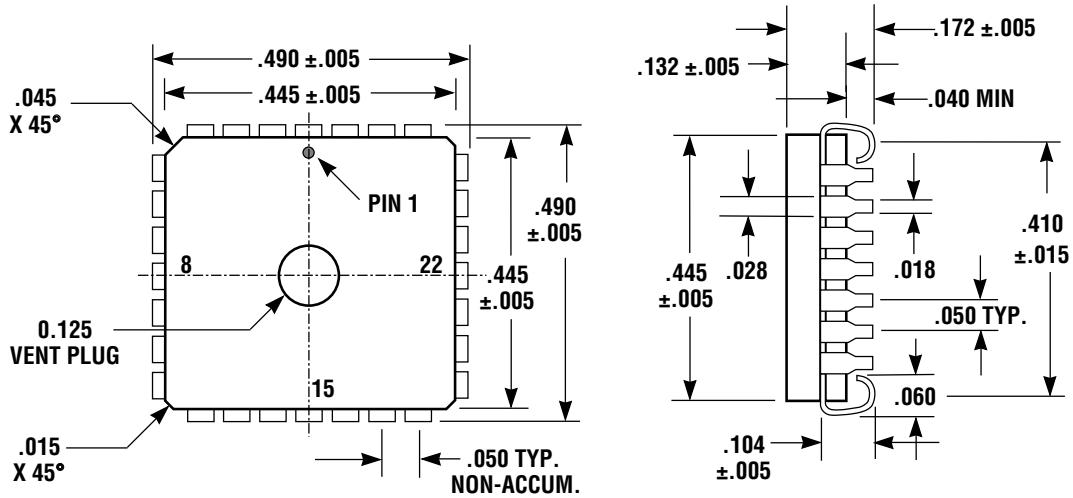


Figure 2



28-Pin MQuad J-Leaded Package Mechanical Specification
 (All dimensions in inches)



28-Pin MQuad Pin Description

Pin #	Pin Name	Description	I/O
1	NC	No Connect	—
2	NC	No Connect	—
3	NC	No Connect	—
4	NC	No Connect	—
5	NC	No Connect	—
6	NC	No Connect	—
7	GND	Ground	—
8	REFCLK	Reference Clock	I
9	TESTIN	Test Input	I
10	NC	No Connect	—
11	GND	Logic Ground	—
12	VDD	Logic VDD (+5 V)	—
13	NC	No Connect	—
14	TEST1	Test Control 1	I

Pin #	Pin Name	Description	I/O
15	TEST2	Test Control 2	I
16	NC	No Connect	—
17	NC	No Connect	0
18	GND	Ground	—
19	EVDD	VDD for ECL Output (+5 V)	—
20	PDR2	Pull-down Resistor 2 (200 Ω)	I
21	QN	Differential PECL Output (-)	0
22	Q	Differential PECL Output (+)	0
23	PDR1	Pull-down Resistor 1 (200 Ω)	I
24	GND	Ground	—
25	AGND	Analog Ground	—
26	AVDD	Analog VDD (+5 V)	—
27	NC	No Connect	—
28	NC	No Connect	—

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