Current-mode PWM controller — UC3842

DESCRIPTION

The UC3842 is available in an 8-Pin mini-DIP the necessary features to implement off-line, fixed-frequency current-mode control schemes with a minimal external parts count. This technique results in improved line regulation, enhanced load response characteristics, and a simpler, easier to design control loop. Topological advantages include inherent pulse-by-pulse current limiting.

Protection circuitry includes built-in undervoltage lock-out and current limiting. Other features include fully-latched operation, a 1% trimmed bandgap reference, and start-up current less than 1mA.

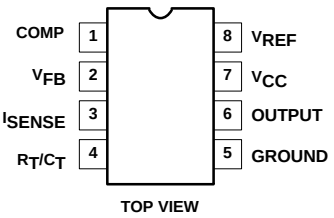
These devices feature a totem-pole output designed to source and sink high peak current from a capacitive load, such as the gate of a power MOSFET. Consistent with N-channel power devices, the output is low in the OFF-state.

FEATURES

- Low start-up current (≤1mA)
- Automatic feed-forward compensation
- Pulse-by-pulse current limiting
- Enhanced load response characteristics
- Undervoltage lock-out with hysteresis
- Double pulse suppression
- High current totem-pole output
- Internally-trimmed bandgap reference
- 400kHz operation, guaranteed min

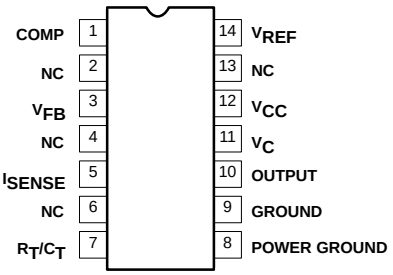
PIN CONFIGURATIONS

N Package



TOP VIEW

D Package

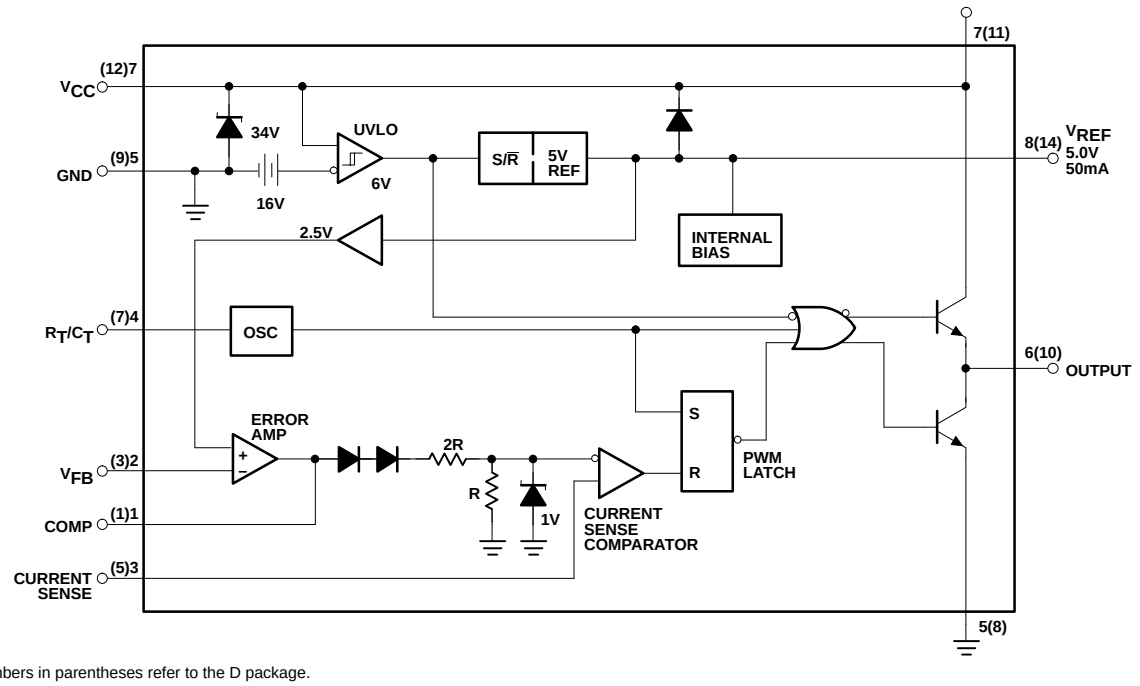


TOP VIEW

APPLICATIONS

- Off-line switched mode power supplies
- DC-to-DC converters UC3842

BLOCK DIAGRAM



NOTE:

Pin numbers in parentheses refer to the D package.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	UC3842N	0404B
14-Pin Plastic Small Outline (SO) Package	0 to +70°C	UC3842D	0405B

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage (I_{CC}<30mA)		Self-Limiting
V_{CC}	Supply voltage (low impedance source)	30	V
I_{OUT}	Output current [2, 3]	±1	A
	Output energy (capacitive load)	5	µJ
	Analog inputs (Pin 2, Pin 3)	-0.3 to 6.3	V
	Error amp output sink current	10	mA
P_D	Power dissipation at T_A≤70°C (derate 12.5mW/°C for T_A>70°C)[2]	1	W
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead temperature (soldering, 10sec max)	300	°C

NOTES:
1. All voltages are with respect to Pin 5; all currents are positive into the specified terminal.
2. See section in application note on “Power Dissipation Calculation”.
3. This parameter is guaranteed, but not 100% tested in production.

DC AND AC ELECTRICAL CHARACTERISTICS

$0 \le T_J \le 70°C$ for UC3842; V_{CC}=15V; R_T=10kW; C_T=3.3nF, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	UC3842			UNIT
			Min	Typ	Max	
Reference section						
V_{OUT}	Output voltage	T_J=25°C, I_O=1mA	4.90	5.00	5.10	V
	Line regulation	$12 \le V_{IN} \le 25V$		6	20	mV
	Load regulation	$1 \le I_O \le 20mA$		6	25	mV
	Temp. stability[1]			0.2	0.4	mV/°C
	Total output variation[1]	Line, load, temp.	4.82		5.18	V
V_{NOISE}	Output noise voltage[1]	$10Hz \le f \le 10kHz$, T_J=25°C		50		µV
	Long-term stability[1]	T_J=125°C, 1000 Hrs.		5	25	mV
	Output short-circuit	T_J=25	-30	-100	-130	mA
	Output short-circuit	$-55 < T_J \le 0°C$	-30	-100	-180	mA
Oscillator section						
	Initial accuracy	T_J=25°C	47	52	57	kHz
	Voltage stability	$12 \le V_{CC} \le 25V$		0.2	1	%
	Temp. stability[1]	$T_{MIN} \le T_J \le T_{MAX}$		5		%
	Amplitude	$V_{PIN\ 4}$ peak-to-peak		1.7		V
Error amp section						
	Input voltage	V Pin 1=2.5V	2.42	2.50	2.58	V
I_{BIAS}	Input bias current			-0.3	-2	µA
A_{VOL}		$2 \le V_O \le 4V$	65	90		dB
	Unity gain bandwidth[1]	T_J=25°C	0.7	1		MHz
	Unity gain bandwidth	$T_{MIN} < T_J < T_{MAX}$	0.5			MHz
PSRR	Power supply rejection ratio	$12 \le V_{CC} \le 25V$	60	70		dB
I_{SINK}	Output sink current	$V_{PIN\ 2}$=2.7V, $V_{PIN\ 1}$=1.1V	2	6		mA
I_{SOURCE}	Output source current	$V_{PIN\ 2}$=2.3V, $V_{PIN\ 1}$=5V	-0.5	-0.8		mA
	V_{OUT} High	$V_{PIN\ 2}$=2.3V, R_L=15k to ground	5	6		V
	V_{OUT} Low	$V_{PIN\ 2}$=2.7V, R_L=15k to Pin 8		0.7	1.1	V
Current sense section						
	Gain [2, 3]		2.85	3	3.15	V/V
	Maximum input signal[2]	$V_{PIN\ 1}$=5V	0.9	1	1.1	V
PSRR	Power supply rejection ratio[2]	$12 \le V_{CC} \le 25V$		70		dB
I_{BIAS}	Input bias current			-2	-10	µA
	Delay to output[1]			150	300	ns

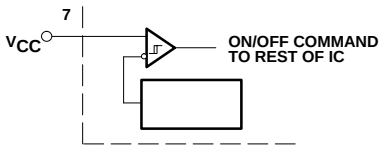
DC AND AC ELECTRICAL CHARACTERISTICS

$0 \le T_J \le 70°C$ for UC3842; V_{CC}=15[4]; R_T=10kΩ; C_T=3.3nF, unless otherwise specified

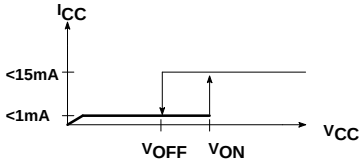
SYMBOL	PARAMETER	TEST CONDITIONS	UC3842			UNIT
			Min	Typ	Max	
Output section						
V_{OL}	Output Low-Level	I_{SINK}=20mA		0.1	0.4	V
		I_{SINK}=200mA		1.5	2.2	
V_{OH}	Output High-Level	I_{SOURCE}=20mA	13	13.5		V
		I_{SOURCE}=200mA	12	13.5		
t_R	Rise time	C_L=1nF		50	150	ns
t_F	Fall time	C_L=1nF		50	150	ns
Undervoltage lockout section						
	Start threshold		14.5	16	17.5	V
	Min. operating voltage after turn on		8.5	10	11.5	V
PWM section						
	Maximum duty cycle		93	97	100	%
	Minimum duty cycle				0	
Total standby current						
	Start-up current			0.5	1	mA
I_{CC}	Operating supply current	$V_{PIN\ 2}$=$V_{PIN\ 3}$=0V		11	17	mA
	V_{CC} zener voltage	I_{CC}=25mA		34		V
Maximum operating frequency section						
	Maximum operating frequency for all functions operating cycle-by-cycle		400			kHz

NOTES:
1. These parameters, although guaranteed, are not 100% tested in production.
2. Parameter measured at trip point of latch with $V_{PIN\ 2}$=0.
3. Gain defined as: $A = \frac{\Delta V_{PIN\ 1}}{\Delta V_{PIN\ 3}}$; $0 \le V_{PIN\ 3} \le 0.8V$

UNDERVOLTAGE LOCKOUT

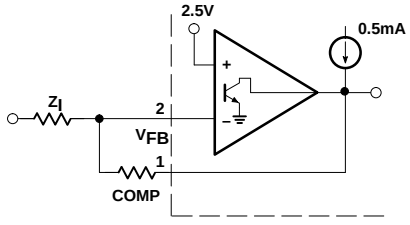


	UC3842
V_{ON}	16V
V_{OFF}	10V



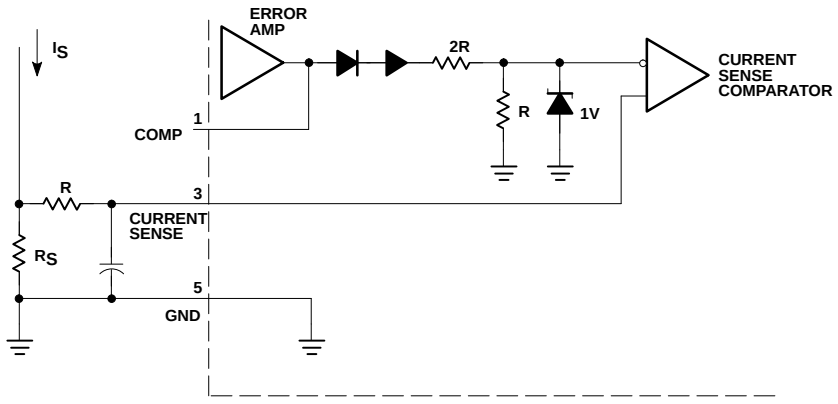
NOTE:
During Undervoltage Lock-Out, the output driver is biased to a high impedance state. Pin 6 should be shunted to ground with a bleeder resistor to prevent activating the power switch with output leakage current.

ERROR AMP CONFIGURATION



NOTE:
Error AMP can source or sink up to 0.5mA.

CURRENT SENSE CIRCUIT



NOTE:

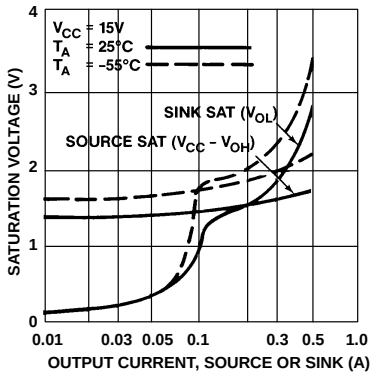
Peak current (I_S) is determined by the formula:

$$I_{S\ MAX} = \frac{1.0V}{R_S}$$

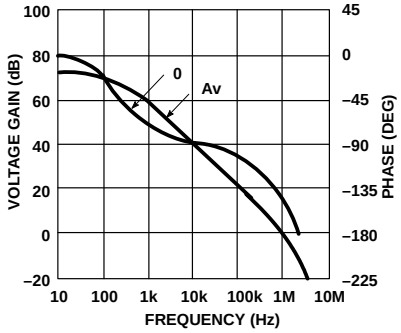
A small RC filter may be required to suppress switch transients.

TYPICAL PERFORMANCE CHARACTERISTICS

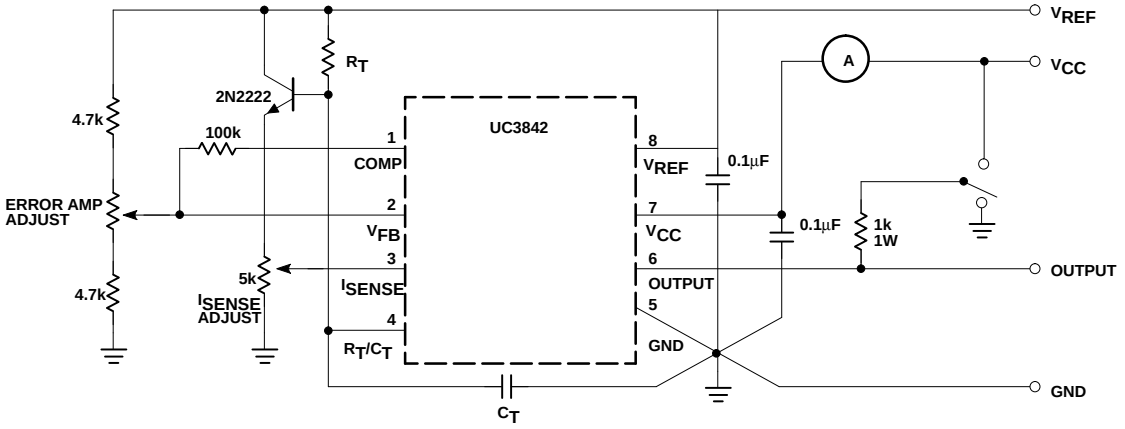
Output Saturation Characteristics



Error Amplifier Open-Loop Frequency Response

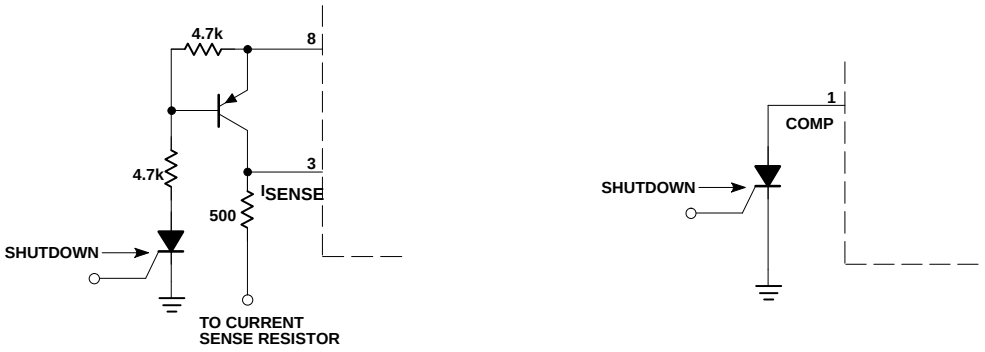


OPEN-LOOP LABORATORY TEST FIXTURE



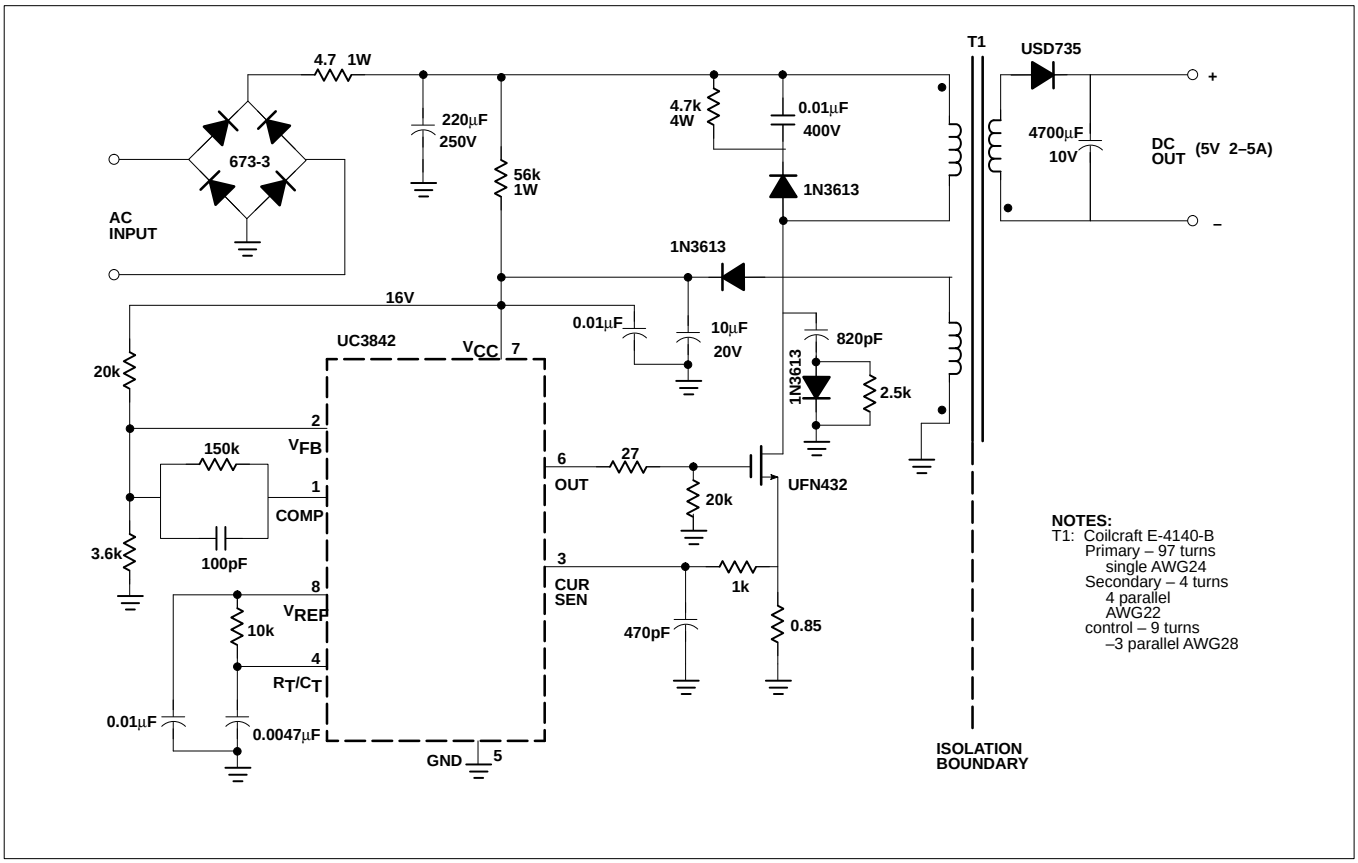
NOTE:
High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to Pin 5 in a single point ground. The transistor and 5k potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to Pin 3.

SHUTDOWN TECHNIQUES



NOTE:
Shutdown of the UC3842 can be accomplished by two methods; either raise Pin 3 above 1V or pull Pin 1 below a voltage two diode drops above ground. Either method causes the output of the PWM comparator to be high (refer to Block Diagram). The PWM latch is reset dominant so that the output will remain low until the next clock cycle after the shutdown condition at Pins 1 and/or 3 is removed. In the examples shown, an externally-latched shutdown may be accomplished by adding an SCR which will be reset by cycling V_{CC} below the lower UVLO threshold (10V). At this point all internal bias is removed, allowing the SCR to reset.

OFF-LINE FLYBACK REGULATOR

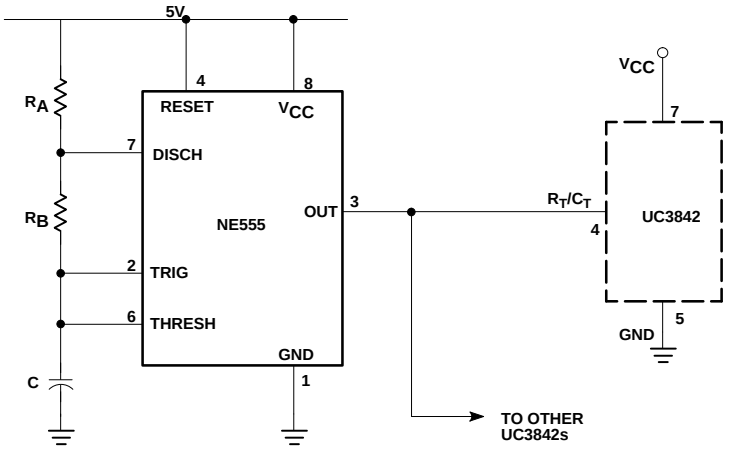


SPECIFICATIONS

Input line voltage:	$90V_{AC}$ to $130V_{AC}$
Input frequency:	50 or 60Hz
Switching frequency:	40kHz±10%
Output power:	25W maximum
Output voltage:	5V±5%
Output current:	2 to 5A
Line regulation:	0.01%/V
Load regulation:	8%/A*
Efficiency @ 25 W,	
V_{IN}=$90V_{AC}$:	70%
V_{IN}=$130V_{AC}$:	65%
Output short-circuit current:	2.5A average

NOTE:
This circuit uses a low-cost feedback scheme in which the DC voltage developed from the primary-side control winding is sensed by the UC3842 error amplifier. Load regulation is therefore dependent on the coupling between secondary and control windings, and on transformer leakage inductance. For applications requiring better load regulation, a UC1901 Isolated Feedback Generator can be used to directly sense the output voltage.

SYNCHRONIZATION AND MAXIMUM DUTY CYCLE CLAMP



NOTES:

$$f = \frac{1.44}{(R_A \quad 2R_B)\ C}$$

$$D_{MAX} = \frac{R_B}{R_A \quad 2R_B}$$