Dual Channel Low Capacitance ESD Protection Array
UM5202EEDF *SOT143*

General Description

UM5202EEDF is surge rated diode arrays designed to protect high speed data interfaces. This series has been specifically designed to protect sensitive components which are connected to data and transmission lines from over-voltage caused by ESD (electrostatic discharge).
The unique design incorporates surge rated, low capacitance steering diodes and a TVS diode in a single package. During transient conditions, the steering diodes direct the transient to either the positive side of the power supply line or to ground. The internal TVS diode prevents over-voltage on the power line, protecting any downstream components.
The low capacitance array configuration allows the user to protect two high-speed data or transmission lines. The low inductance construction minimizes voltage overshoot during high current surges. This device is optimized for ESD protection of portable electronics. They may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (± 15kV air, ± 8kV contact discharge).

Applications

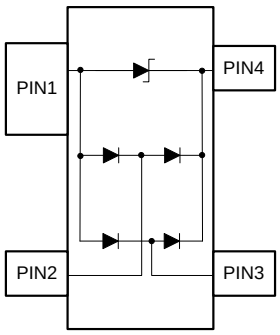
- USB 2.0
- USB OTG
- Monitors and Flat Panel Displays
- Digital Visual Interface (DVI)
- High-Definition Multimedia Interface (HDMI)
- SIM Ports
- IEEE 1394 Firewire Ports

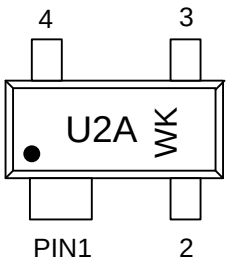
Features

- Transient Protection for High-Speed Data Lines to IEC 61000-4-2 (ESD) ± 15kV (Air), ± 8kV (Contact)
- Array of Surge Rated Diodes with Internal TVS Diode
- Protects Two I/O Lines & Power Line
- Low Capacitance (<2pF) for High-Speed Interfaces
- No Insertion Loss to 2.0GHz
- Low Leakage Current and Clamping Voltage
- Low Operating Voltage: 5.0V
- Solid-State Silicon-Avalanche Technology

Pin Configurations

Top View





WK: Week Code
UM5202EEDF
SOT143

Ordering Information

Part Number	Working Voltage	Packaging Type	Channel	Marking Code	Shipping Qty
UM5202EEDF	5.0V	SOT143	2	U2A	3000pcs /7Inch Tape & Reel

Absolute Maximum Ratings

RATING	SYMBOL	VALUE	UNITS
Peak Pulse Power (tp = 8/20μs)	P_{pk}	150	Watts
Peak Pulse Current (tp = 8/20μs)	I_{PP}	6	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	±15 ±8	kV
Operating Temperature	T_J	-55 to +125	℃
Storage Temperature	T_{STG}	-55 to +150	℃

Electrical Characteristics (Note 1)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Reverse Stand-Off Voltage	V_{RWM}				5.0	V
Reverse Breakdown Voltage	V_{BR}	It = 1mA, Pin 4 to Pin1	6.0			V
Reverse Leakage Current	I_R	V_{RWM} = 5V, T=25℃, Pin4 to Pin1			2	μA
Clamping Voltage	V_C	I_{PP} = 1A, 8/20μs, Any pin to pin1			15	V
Clamping Voltage	V_C	I_{PP} = 6A, 8/20μs, Any pin to pin1			25	V
Junction Capacitance	C_j	V_R = 0V, f = 1MHz, Any I/O pin to pin1			2	pF
		V_R = 0V, f = 1MHz , Between I/O pins			1	pF
		V_R = 0V, f = 1MHz, Pin4 to pin1		60		pF
		V_R = 2.5V, f = 1MHz, Pin4 to pin1		40		pF
Reverse Recovery Time	Trr	Pin1to Pin4		40		ns
		Pin1 to I/O Pin		160		ns
		Pin4 to I/O Pin		45		ns

Note 1: I/O pins are pin 2, 3.

Applications Information

Device Connection Options for Protection of two High-Speed Data Lines

This device is designed to protect data lines by clamping them to a fixed reference. When the voltage on the protected line exceeds the reference voltage the steering diodes are forward biased, conducting the transient current away from the sensitive circuitry. Data lines are connected at pins 2, 3. Pin 1 should be connected directly to a ground plane. The path length is kept as short as possible to minimize parasitic inductance. The positive reference is connected at pin 4. The options for connecting the positive reference are as follows:

1. To protect data lines and the power line, connect pin 4 directly to the positive supply rail (VCC). In this configuration the data lines are referenced to the supply voltage. The internal TVS diode prevents over-voltage on the supply rail.
2. In applications where the supply rail does not exit the system, the internal TVS may be used as the reference. In this case, pin 4 is not connected. The steering diodes will begin to conduct when the voltage on the protected line exceeds the working voltage of the TVS (plus one diode drop).

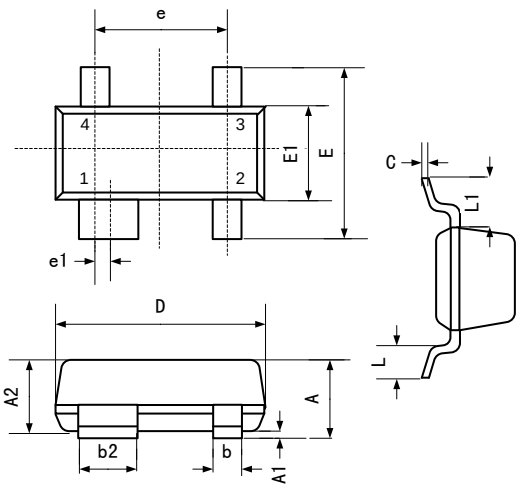
Matte Tin Lead Finish

Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. In addition, unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation of the solder joint.

Package Information

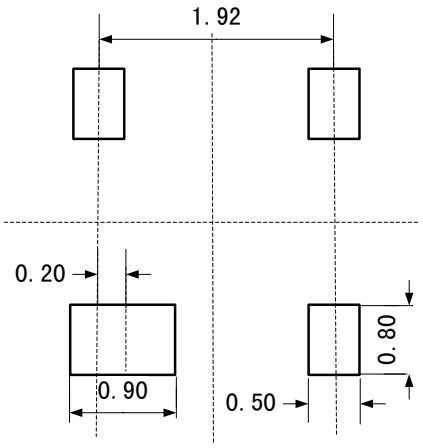
UM5202EEDF SOT143

Outline Drawing



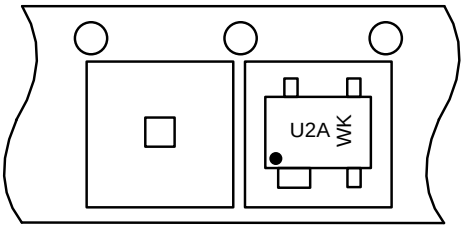
Symbol	DIMENSIONS			
	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	0.763	1.220	0.031	0.049
A1	0.013	0.150	0.001	0.006
A2	0.750	1.070	0.030	0.043
b	0.300	0.510	0.012	0.020
b2	0.760	0.930	0.030	0.037
C	0.080	0.200	0.003	0.008
D	2.800	3.040	0.112	0.122
E	2.200	2.640	0.088	0.211
E1	1.200	1.400	0.048	0.056
e	1.920BSC		0.077BSC	
e1	0.200BSC		0.008BSC	
L1	0.540REF		0.022	
L	0.400	0.600	0.016	0.024

Land Pattern



NOTES:
1. Compound dimension: 2.90×1.30;
2. Unit: mm;
3. General tolerance ±0.05mm unless otherwise specified;
4. The layout is just for reference.

Tape and Reel Orientation



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