

240-OUTPUT TFT-LCD GATE DRIVER**DESCRIPTION**

The μ PD16704 is a TFT-LCD gate driver equipped with 240-output lines. It can output a high-gate scanning voltage in response to CMOS level input because it is provided with a level-shift circuit inside the IC circuit.

FEATURES

- CMOS level input (3.0 to 3.6 V)
- 240 outputs
- High-output voltage (V_{DD2} to V_{EE2} : 40 V MAX.)
- Double scan inversion function
- COG inversion

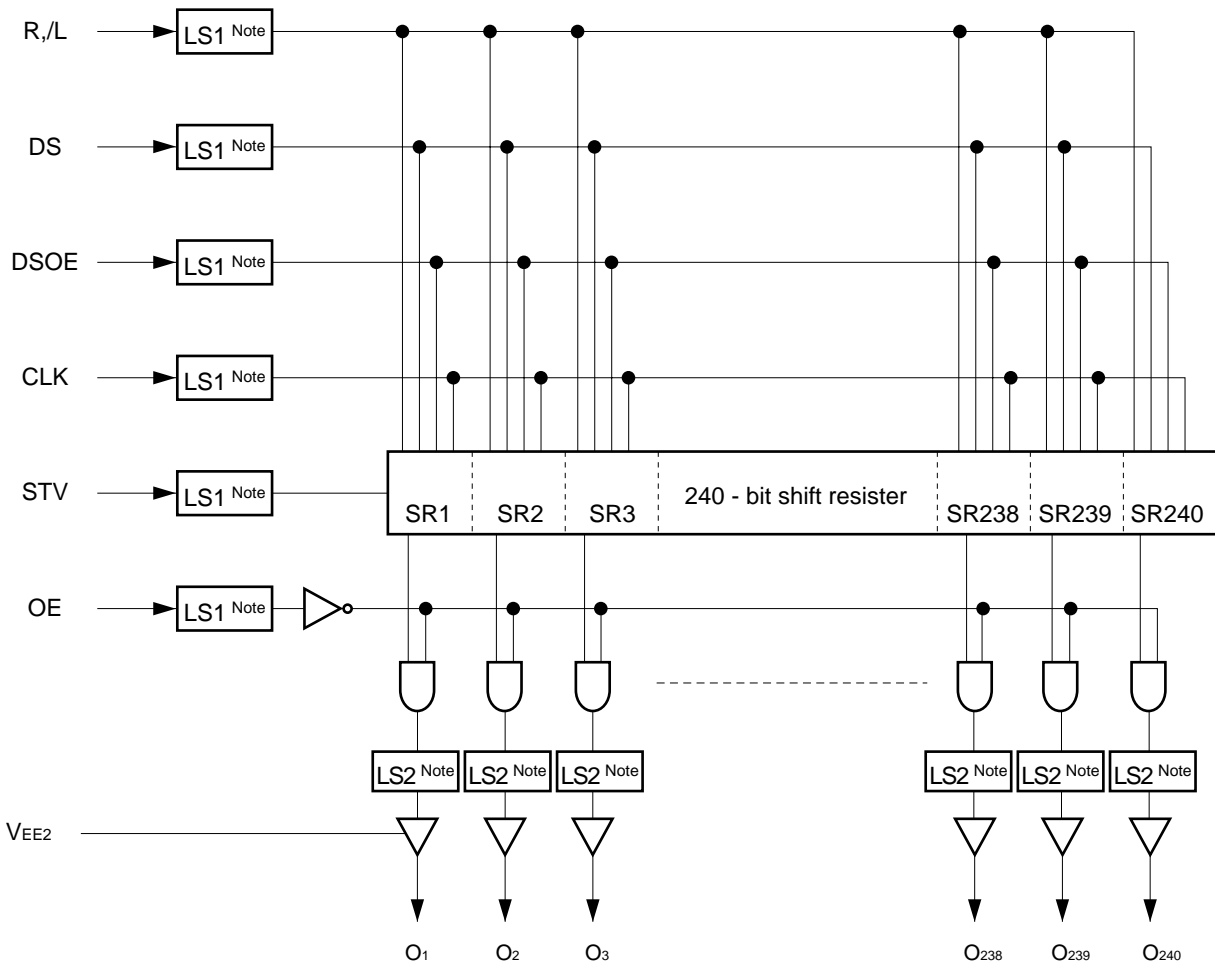
ORDERING INFORMATION

Part Number	Package
μ PD16704P	Chip

Remark Purchasing the above chip entail the exchange of documents such as a separate memorandum or product quality, so please contact one of our sales representatives.

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1. BLOCK DIAGRAM

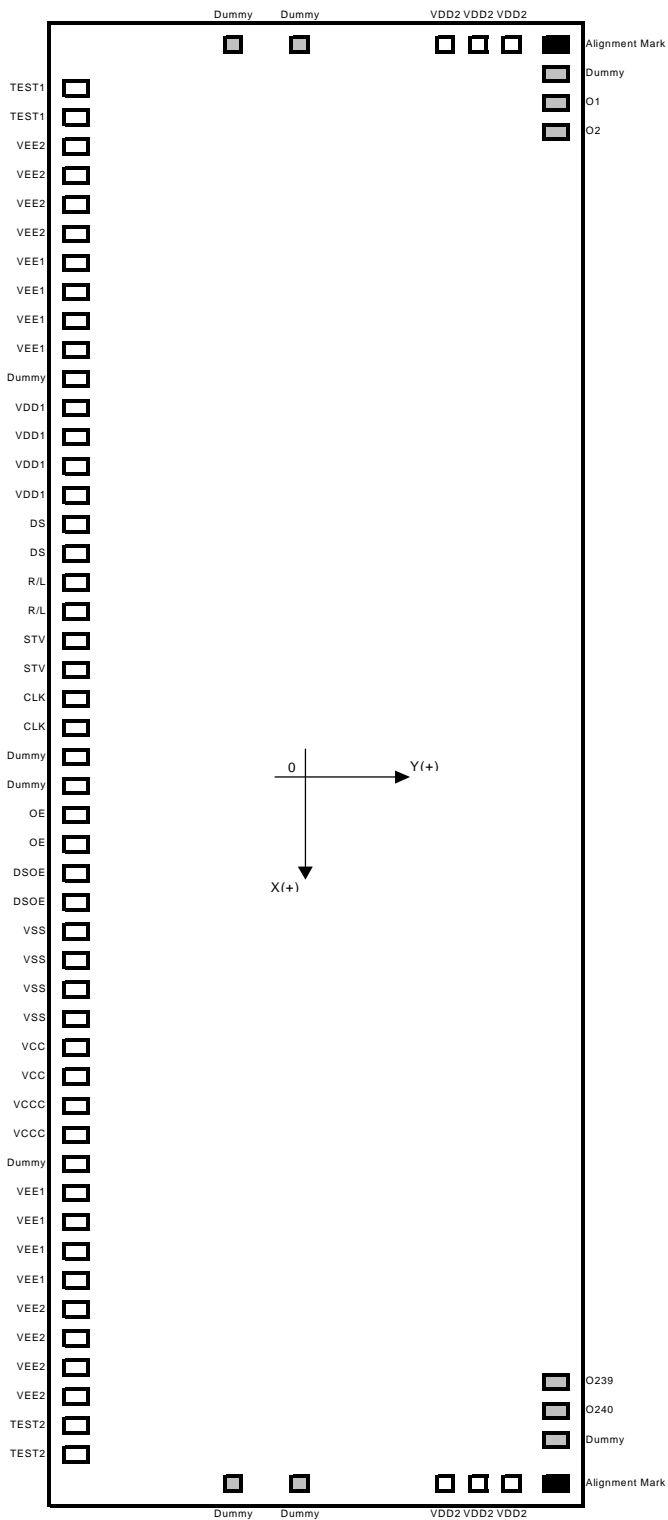


Note LS1: shifts CMOS level and internal level, LS2: shifts internal level and output level (V_{DD2} to V_{EE2}).

Remark /xxx indicates active low signal.

2. PIN CONFIGURATION (IC Pad Surface)

Chip Size: 1.06 x 15.39 mm²



Remark This figure does not specify the TCP package.

Figure 2-1. Pad Coordinate (1/3)

No	PAD Name	X[μm]	Y[μm]	Bump size (X:Y)[μm]
1	TEST1	-7061.8	-375.0	110:60
2	TEST1	-6931.8	-375.0	110:60
3	VEE2	-6801.8	-375.0	110:60
4	VEE2	-6671.8	-375.0	110:60
5	VEE2	-6541.8	-375.0	110:60
6	VEE2	-6411.8	-375.0	110:60
7	VEE1	-6193.8	-375.0	110:60
8	VEE1	-6063.8	-375.0	110:60
9	VEE1	-5933.8	-375.0	110:60
10	VEE1	-5803.8	-375.0	110:60
11	DUMMY	-5673.8	-375.0	110:60
12	VDD1	-5490.8	-375.0	110:60
13	VDD1	-5360.8	-375.0	110:60
14	VDD1	-4999.0	-375.0	110:60
15	VDD1	-4450.2	-375.0	110:60
16	DS	-4120.4	-375.0	110:60
17	DS	-3809.4	-375.0	110:60
18	RL	-3362.4	-375.0	110:60
19	RL	-2924.2	-375.0	110:60
20	STV	-2280.2	-375.0	110:60
21	STV	-1969.2	-375.0	110:60
22	CLK	-1522.2	-375.0	110:60
23	CLK	-1084.0	-375.0	110:60
24	DUMMY	-440.0	-375.0	110:60
25	DUMMY	182.2	-375.0	110:60
26	OE	826.2	-375.0	110:60
27	OE	1264.4	-375.0	110:60
28	DSOE	1711.4	-375.0	110:60
29	DSOE	2022.4	-375.0	110:60
30	VSS	2194.2	-375.0	110:60
31	VSS	2564.8	-375.0	110:60
32	VSS	2926.6	-375.0	110:60
33	VSS	3056.6	-375.0	110:60
34	VCC	3433.4	-375.0	110:60
35	VCC	4073.4	-375.0	110:60
36	VCCC	4450.2	-375.0	110:60
37	VCCC	5090.2	-375.0	110:60
38	DUMMY	5691.8	-375.0	110:60
39	VEE1	5821.8	-375.0	110:60
40	VEE1	5951.8	-375.0	110:60
41	VEE1	6081.8	-375.0	110:60
42	VEE1	6211.8	-375.0	110:60
43	VEE2	6429.8	-375.0	110:60
44	VEE2	6559.8	-375.0	110:60
45	VEE2	6689.8	-375.0	110:60
46	VEE2	6819.8	-375.0	110:60
47	TEST2	6949.8	-375.0	110:60
48	TEST2	7079.8	-375.0	110:60
49	DUMMY	7556.0	-220.0	80:40
50	DUMMY	7556.0	-80.0	80:40

No	PAD Name	X[μm]	Y[μm]	Bump size (X:Y)[μm]
51	VDD2	7556.0	136.0	110:60
52	VDD2	7556.0	216.0	110:60
53	VDD2	7556.0	296.0	110:60
54	DUMMY	7200.0	310.5	40:80
55	O ₂₄₀	7140.0	310.5	40:80
56	O ₂₃₉	7080.0	310.5	40:80
57	O ₂₃₈	7020.0	310.5	40:80
58	O ₂₃₇	6960.0	310.5	40:80
59	O ₂₃₆	6900.0	310.5	40:80
60	O ₂₃₅	6840.0	310.5	40:80
61	O ₂₃₄	6780.0	310.5	40:80
62	O ₂₃₃	6720.0	310.5	40:80
63	O ₂₃₂	6660.0	310.5	40:80
64	O ₂₃₁	6600.0	310.5	40:80
65	O ₂₃₀	6540.0	310.5	40:80
66	O ₂₂₉	6480.0	310.5	40:80
67	O ₂₂₈	6420.0	310.5	40:80
68	O ₂₂₇	6360.0	310.5	40:80
69	O ₂₂₆	6300.0	310.5	40:80
70	O ₂₂₅	6240.0	310.5	40:80
71	O ₂₂₄	6180.0	310.5	40:80
72	O ₂₂₃	6120.0	310.5	40:80
73	O ₂₂₂	6060.0	310.5	40:80
74	O ₂₂₁	6000.0	310.5	40:80
75	O ₂₂₀	5940.0	310.5	40:80
76	O ₂₁₉	5880.0	310.5	40:80
77	O ₂₁₈	5820.0	310.5	40:80
78	O ₂₁₇	5760.0	310.5	40:80
79	O ₂₁₆	5700.0	310.5	40:80
80	O ₂₁₅	5640.0	310.5	40:80
81	O ₂₁₄	5580.0	310.5	40:80
82	O ₂₁₃	5520.0	310.5	40:80
83	O ₂₁₂	5460.0	310.5	40:80
84	O ₂₁₁	5400.0	310.5	40:80
85	O ₂₁₀	5340.0	310.5	40:80
86	O ₂₀₉	5280.0	310.5	40:80
87	O ₂₀₈	5220.0	310.5	40:80
88	O ₂₀₇	5160.0	310.5	40:80
89	O ₂₀₆	5100.0	310.5	40:80
90	O ₂₀₅	5040.0	310.5	40:80
91	O ₂₀₄	4980.0	310.5	40:80
92	O ₂₀₃	4920.0	310.5	40:80
93	O ₂₀₂	4860.0	310.5	40:80
94	O ₂₀₁	4800.0	310.5	40:80
95	O ₂₀₀	4740.0	310.5	40:80
96	O ₁₉₉	4680.0	310.5	40:80
97	O ₁₉₈	4620.0	310.5	40:80
98	O ₁₉₇	4560.0	310.5	40:80
99	O ₁₉₆	4500.0	310.5	40:80
100	O ₁₉₅	4440.0	310.5	40:80

Figure 2-1. Pad Coordinate (2/3)

No	PAD Name	X[μm]	Y[μm]	Bump size (X:Y)[μm]
101	O194	4380.0	310.5	40:80
102	O193	4320.0	310.5	40:80
103	O192	4260.0	310.5	40:80
104	O191	4200.0	310.5	40:80
105	O190	4140.0	310.5	40:80
106	O189	4080.0	310.5	40:80
107	O188	4020.0	310.5	40:80
108	O187	3960.0	310.5	40:80
109	O186	3900.0	310.5	40:80
110	O185	3840.0	310.5	40:80
111	O184	3780.0	310.5	40:80
112	O183	3720.0	310.5	40:80
113	O182	3660.0	310.5	40:80
114	O181	3600.0	310.5	40:80
115	O180	3540.0	310.5	40:80
116	O179	3480.0	310.5	40:80
117	O178	3420.0	310.5	40:80
118	O177	3360.0	310.5	40:80
119	O176	3300.0	310.5	40:80
120	O175	3240.0	310.5	40:80
121	O174	3180.0	310.5	40:80
122	O173	3120.0	310.5	40:80
123	O172	3060.0	310.5	40:80
124	O171	3000.0	310.5	40:80
125	O170	2940.0	310.5	40:80
126	O169	2880.0	310.5	40:80
127	O168	2820.0	310.5	40:80
128	O167	2760.0	310.5	40:80
129	O166	2700.0	310.5	40:80
130	O165	2640.0	310.5	40:80
131	O164	2580.0	310.5	40:80
132	O163	2520.0	310.5	40:80
133	O162	2460.0	310.5	40:80
134	O161	2400.0	310.5	40:80
135	O160	2340.0	310.5	40:80
136	O159	2280.0	310.5	40:80
137	O158	2220.0	310.5	40:80
138	O157	2160.0	310.5	40:80
139	O156	2100.0	310.5	40:80
140	O155	2040.0	310.5	40:80
141	O154	1980.0	310.5	40:80
142	O153	1920.0	310.5	40:80
143	O152	1860.0	310.5	40:80
144	O151	1800.0	310.5	40:80
145	O150	1740.0	310.5	40:80
146	O149	1680.0	310.5	40:80
147	O148	1620.0	310.5	40:80
148	O147	1560.0	310.5	40:80
149	O146	1500.0	310.5	40:80
150	O145	1440.0	310.5	40:80

No	PAD Name	X[μm]	Y[μm]	Bump size (X:Y)[μm]
151	O144	1380.0	310.5	40:80
152	O143	1320.0	310.5	40:80
153	O142	1260.0	310.5	40:80
154	O141	1200.0	310.5	40:80
155	O140	1140.0	310.5	40:80
156	O139	1080.0	310.5	40:80
157	O138	1020.0	310.5	40:80
158	O137	960.0	310.5	40:80
159	O136	900.0	310.5	40:80
160	O135	840.0	310.5	40:80
161	O134	780.0	310.5	40:80
162	O133	720.0	310.5	40:80
163	O132	660.0	310.5	40:80
164	O131	600.0	310.5	40:80
165	O130	540.0	310.5	40:80
166	O129	480.0	310.5	40:80
167	O128	420.0	310.5	40:80
168	O127	360.0	310.5	40:80
169	O126	300.0	310.5	40:80
170	O125	240.0	310.5	40:80
171	O124	180.0	310.5	40:80
172	O123	120.0	310.5	40:80
173	O122	60.0	310.5	40:80
174	O121	0.0	310.5	40:80
175	O120	-60.0	310.5	40:80
176	O119	-120.0	310.5	40:80
177	O118	-180.0	310.5	40:80
178	O117	-240.0	310.5	40:80
179	O116	-300.0	310.5	40:80
180	O115	-360.0	310.5	40:80
181	O114	-420.0	310.5	40:80
182	O113	-480.0	310.5	40:80
183	O112	-540.0	310.5	40:80
184	O111	-600.0	310.5	40:80
185	O110	-660.0	310.5	40:80
186	O109	-720.0	310.5	40:80
187	O108	-780.0	310.5	40:80
188	O107	-840.0	310.5	40:80
189	O106	-900.0	310.5	40:80
190	O105	-960.0	310.5	40:80
191	O104	-1020.0	310.5	40:80
192	O103	-1080.0	310.5	40:80
193	O102	-1140.0	310.5	40:80
194	O101	-1200.0	310.5	40:80
195	O100	-1260.0	310.5	40:80
196	O99	-1320.0	310.5	40:80
197	O98	-1380.0	310.5	40:80
198	O97	-1440.0	310.5	40:80
199	O96	-1500.0	310.5	40:80
200	O95	-1560.0	310.5	40:80

Figure 2-1. Pad Coordinate (3/3)

No	PAD Name	X[μm]	Y[μm]	Bump size (X:Y)[μm]
201	O ₉₄	-1620.0	310.5	40:80
202	O ₉₃	-1680.0	310.5	40:80
203	O ₉₂	-1740.0	310.5	40:80
204	O ₉₁	-1800.0	310.5	40:80
205	O ₉₀	-1860.0	310.5	40:80
206	O ₈₉	-1920.0	310.5	40:80
207	O ₈₈	-1980.0	310.5	40:80
208	O ₈₇	-2040.0	310.5	40:80
209	O ₈₆	-2100.0	310.5	40:80
210	O ₈₅	-2160.0	310.5	40:80
211	O ₈₄	-2220.0	310.5	40:80
212	O ₈₃	-2280.0	310.5	40:80
213	O ₈₂	-2340.0	310.5	40:80
214	O ₈₁	-2400.0	310.5	40:80
215	O ₈₀	-2460.0	310.5	40:80
216	O ₇₉	-2520.0	310.5	40:80
217	O ₇₈	-2580.0	310.5	40:80
218	O ₇₇	-2640.0	310.5	40:80
219	O ₇₆	-2700.0	310.5	40:80
220	O ₇₅	-2760.0	310.5	40:80
221	O ₇₄	-2820.0	310.5	40:80
222	O ₇₃	-2880.0	310.5	40:80
223	O ₇₂	-2940.0	310.5	40:80
224	O ₇₁	-3000.0	310.5	40:80
225	O ₇₀	-3060.0	310.5	40:80
226	O ₆₉	-3120.0	310.5	40:80
227	O ₆₈	-3180.0	310.5	40:80
228	O ₆₇	-3240.0	310.5	40:80
229	O ₆₆	-3300.0	310.5	40:80
230	O ₆₅	-3360.0	310.5	40:80
231	O ₆₄	-3420.0	310.5	40:80
232	O ₆₃	-3480.0	310.5	40:80
233	O ₆₂	-3540.0	310.5	40:80
234	O ₆₁	-3600.0	310.5	40:80
235	O ₆₀	-3660.0	310.5	40:80
236	O ₅₉	-3720.0	310.5	40:80
237	O ₅₈	-3780.0	310.5	40:80
238	O ₅₇	-3840.0	310.5	40:80
239	O ₅₆	-3900.0	310.5	40:80
240	O ₅₅	-3960.0	310.5	40:80
241	O ₅₄	-4020.0	310.5	40:80
242	O ₅₃	-4080.0	310.5	40:80
243	O ₅₂	-4140.0	310.5	40:80
244	O ₅₁	-4200.0	310.5	40:80
245	O ₅₀	-4260.0	310.5	40:80
246	O ₄₉	-4320.0	310.5	40:80
247	O ₄₈	-4380.0	310.5	40:80
248	O ₄₇	-4440.0	310.5	40:80
249	O ₄₆	-4500.0	310.5	40:80
250	O ₄₅	-4560.0	310.5	40:80

No	PAD Name	X[μm]	Y[μm]	Bump size (X:Y)[μm]
251	O ₄₄	-4620.0	310.5	40:80
252	O ₄₃	-4680.0	310.5	40:80
253	O ₄₂	-4740.0	310.5	40:80
254	O ₄₁	-4800.0	310.5	40:80
255	O ₄₀	-4860.0	310.5	40:80
256	O ₃₉	-4920.0	310.5	40:80
257	O ₃₈	-4980.0	310.5	40:80
258	O ₃₇	-5040.0	310.5	40:80
259	O ₃₆	-5100.0	310.5	40:80
260	O ₃₅	-5160.0	310.5	40:80
261	O ₃₄	-5220.0	310.5	40:80
262	O ₃₃	-5280.0	310.5	40:80
263	O ₃₂	-5340.0	310.5	40:80
264	O ₃₁	-5400.0	310.5	40:80
265	O ₃₀	-5460.0	310.5	40:80
266	O ₂₉	-5520.0	310.5	40:80
267	O ₂₈	-5580.0	310.5	40:80
268	O ₂₇	-5640.0	310.5	40:80
269	O ₂₆	-5700.0	310.5	40:80
270	O ₂₅	-5760.0	310.5	40:80
271	O ₂₄	-5820.0	310.5	40:80
272	O ₂₃	-5880.0	310.5	40:80
273	O ₂₂	-5940.0	310.5	40:80
274	O ₂₁	-6000.0	310.5	40:80
275	O ₂₀	-6060.0	310.5	40:80
276	O ₁₉	-6120.0	310.5	40:80
277	O ₁₈	-6180.0	310.5	40:80
278	O ₁₇	-6240.0	310.5	40:80
279	O ₁₆	-6300.0	310.5	40:80
280	O ₁₅	-6360.0	310.5	40:80
281	O ₁₄	-6420.0	310.5	40:80
282	O ₁₃	-6480.0	310.5	40:80
283	O ₁₂	-6540.0	310.5	40:80
284	O ₁₁	-6600.0	310.5	40:80
285	O ₁₀	-6660.0	310.5	40:80
286	O ₉	-6720.0	310.5	40:80
287	O ₈	-6780.0	310.5	40:80
288	O ₇	-6840.0	310.5	40:80
289	O ₆	-6900.0	310.5	40:80
290	O ₅	-6960.0	310.5	40:80
291	O ₄	-7020.0	310.5	40:80
292	O ₃	-7080.0	310.5	40:80
293	O ₂	-7140.0	310.5	40:80
294	O ₁	-7200.0	310.5	40:80
295	DUMMY	-7260.0	310.5	40:80
296	V _{DD2}	-7556.0	296.0	110:60
297	V _{DD2}	-7556.0	216.0	110:60
298	V _{DD2}	-7556.0	136.0	110:60
299	DUMMY	-7556.0	-80.0	80:40
300	DUMMY	-7556.0	-220.0	80:40

3. PIN FUNCTIONS

(1/2)

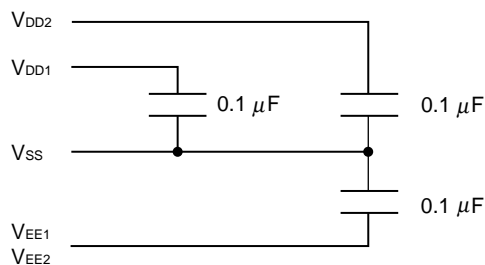
Pin Symbol	Pin Name	Pad No	I/O	Description
O ₁ to O ₂₄₀	Driver output	294 - 55	Output	These pins output scan signals that drive the vertical direction (gate lines) of a TFT-LCD. The output signals change in synchronization with the rising edge of shift clock CLK. The driver output amplitude is V _{DD2} to V _{EE2} .
R,/L	Shift direction select input	18, 19	Input	R,/L = H (right shift) : STV → O ₁ → O ₂₄₀ R,/L = L (left shift) : STV → O ₂₄₀ → O ₁
STV	Start pulse input/output	20, 21	I/O	This is the input of the internal shift register. The start pulse is written at the rising edge of shift clock CLK. The pulse range is less than one cycle of CLK. The input level is a V _{DD1} to V _{SS} (logic level).
CLK	Shift clock input	22, 23	Input	This pin inputs a shift clock to the internal shift register. The shift operation is performed in synchronization with the rising edge of this input.
OE	Output enable input	26, 27	Input	When this pin goes low level, the driver output is fixed to V _{EE2} level. The shift register is not cleared. Refer to 4. TIMING CHART for details.
DS	Double scan control input	16, 17	Input	This pin outputs scan signals simultaneously from two outputs in synchronization with the rise of CLK when DS = H is written. Refer to 4. TIMING CHART for details.
DSOE	Double scan pulse width control input	28, 29	Input	This pin controls the fall timing of one of the scan signals (the output side in normal scan mode) when the DS signal is used to output scan signals simultaneously from two outputs. This signal is input asynchronously to the clock. Refer to 4. TIMING CHART for details.
VCC, VCCC	IC internal reference voltage	34, 35, 36, 37	–	Short the VCC pin to the VCCC pin so that these pins are in a floating state.
TEST1, TEST2	TEST pins	1, 2, 47, 48	–	Short TEST1 and TEST2 separately inside the IC. These pins are not connected to any other pins inside the IC.
Dummy	Dummy pin	11, 24, 25, 38, 49, 50, 54, 295, 299, 300	–	No dummy pins are connected to any other pins inside the IC.
V _{DD1}	Logic power supply	12 - 15	–	3.3 ± 0.3 V
V _{DD2}	Driver positive power supply	51 - 53, 296 - 298	–	15 to 25 V The driver output: high level

(2/2)

Pin Symbol	Pin Name	Pad No	I/O	Description
V _{SS}	Logic ground	30 - 33	–	Connect this pin to the ground of the system.
V _{EE1}	Negative power supply for internal operation	7 - 10, 39 - 42	–	–15 to –5 V
V _{EE2}	Driver negative power supply	3 - 6, 43 - 46	–	The driver output: low level (V _{EE2} to V _{EE1} < 6.0 V)

Cautions 1. To prevent latch-up, turn on power to V_{DD1}, V_{EE1}, V_{EE2}, V_{DD2}, and logic input in this order. Turn off power in the reverse order. These power up/down sequence must be observed also during transition period.

2. Insert a capacitor of about 0.1 μF between each power line, as shown below, to secure noise margin such as V_{IH} and V_{IL}.

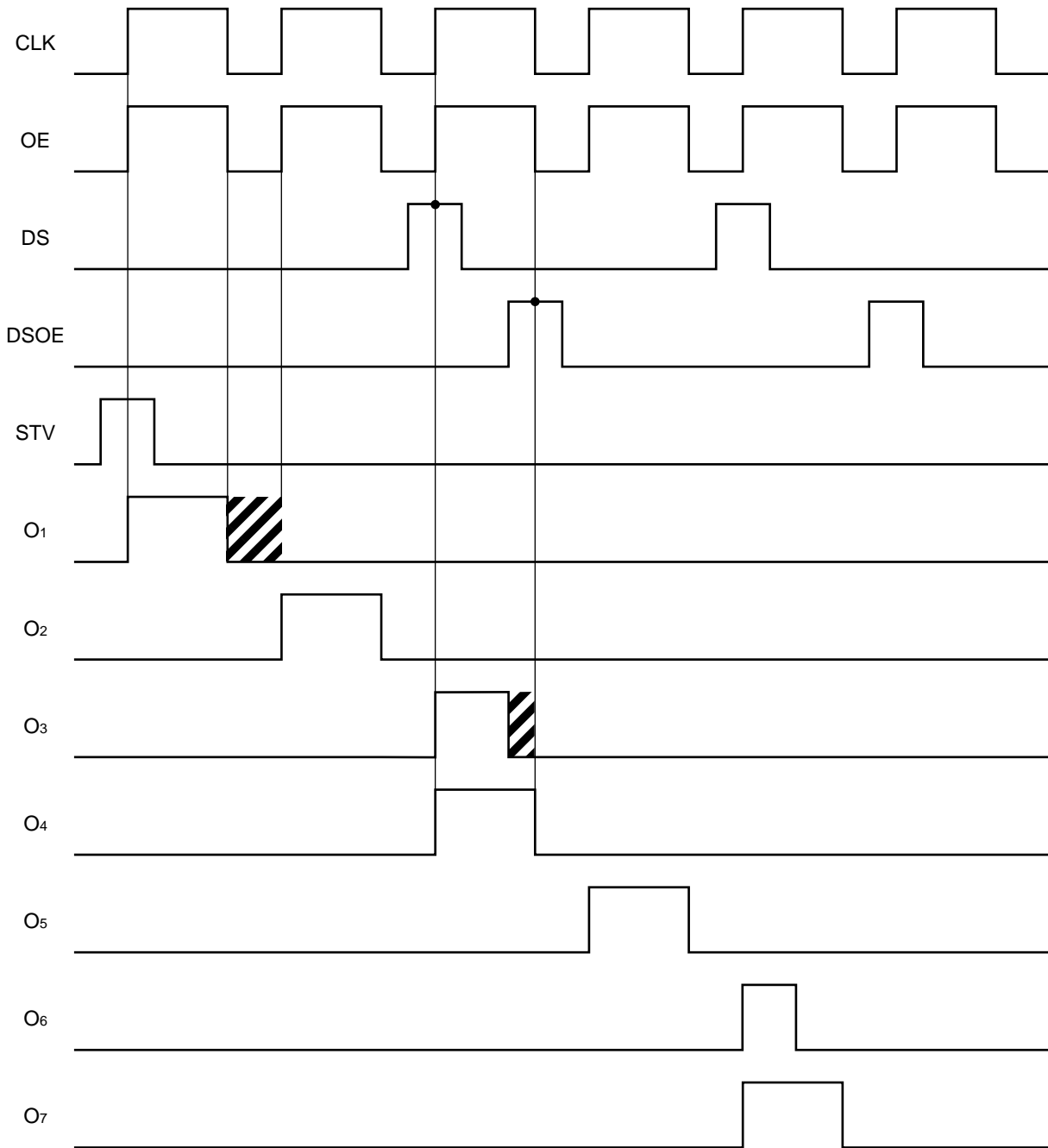


4. TIMING CHART (R,/L = H)

As shown in the figure below, when DS = H, scan signals are output successively from two outputs in synchronization with the rise of CLK (double scan operation).

It is also possible to accelerate the fall timing of one of the scan signals (the output side in normal scan mode) in a double scan operation by using the DSOE signal. DSOE is input asynchronously to the clock, and the output is fixed to V_{EE2} in the period between the rise of DSOE and the rise of CLK.

The DSOE signal is only enabled during a double scan operation.



5. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS} = 0 V)

Parameter	Symbol	Rating	Unit
Logic Supply Voltage	V _{DD1}	-0.5 to +7.0	V
Driver Positive Supply Voltage	V _{DD2}	-0.5 to +28	V
Power Supply Voltage	V _{DD2} to V _{EE1} , V _{EE2}	-0.5 to +42	V
Internal Operation Negative Supply Voltage	V _{EE1}	-16 to +0.5	V
Driver Negative Supply Voltage	V _{EE2}	V _{EE1} - 0.3 to V _{EE1} + 7.0	V
Input Voltage	V _I	-0.5 to V _{DD1} + 0.5	V
Operating Ambient Temperature	T _A	-30 to +85	°C
Storage Temperature	T _{stg}	-55 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Range (T_A = -30 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Logic Supply Voltage	V _{DD1}	3.0	3.3	3.6	V
Driver Positive Supply Voltage	V _{DD2}	15	23	25	V
Internal Operation Negative Supply Voltage	V _{EE1}	-15	-10	-5.0	V
Power Supply Voltage	V _{DD2} to V _{EE1}	20	33	40	V
	V _{EE2} to V _{EE1}	0		6.0	V
Clock Frequency	f _{CLK}			500	kHz

Electrical Characteristics (T_A = -30 to +85°C, V_{DD1} = 3.3 V ±0.3 V, V_{DD2} = 23 V, V_{EE1} = V_{EE2} = -10 V, V_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High-level Input Voltage	V _{IH}	CLK, STV, R _/ L, OE	0.8 V _{DD1}		V _{DD1}	V
Low-level Input Voltage	V _{IL}		V _{SS}		0.2 V _{DD1}	V
LCD Driver Output ON Resistance	R _{ON}	V _{OUT} = V _{EE2} + 1.0 V, or V _{DD2} - 1.0 V			2.0	kΩ
Input Leak Current	I _{IL}	V _I = 0 V or 3.6 V,			±1.0	μA
Dynamic Current Dissipation	I _{DD1}	V _{DD1} , f _{CLK} = 50 kHz, f _{STV} = 60 Hz, No load			1000	μA
	I _{DD2}	V _{DD2} , f _{CLK} = 50 kHz, f _{STV} = 60 Hz, No load			100	μA
	I _{EE}	V _{EE1} , f _{CLK} = 50 kHz, f _{STV} = 60 Hz, No load	-1000			μA

Switching Characteristics (T_A = -30 to +85°C, V_{DD1} = 3.3 V ±0.3 V, V_{DD2} = 23 V, V_{EE1} = V_{EE2} = -10 V, V_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Driver Output Delay Time	t _{PHL2}	C _L = 300 pF, CLK → O _n			800	ns
	t _{PLH2}				800	ns
	t _{PHL3}	C _L = 300 pF, OE → O _n			800	ns
	t _{PLH3}				800	ns
DSOE	t _{PHL4}			800	ns	
Output Rise Time	t _{TLH}	C _L = 300 pF			1500	ns
Output Fall Time	t _{THL}				1500	ns
Input Capacitance	C _I	T _A = 25°C			15	pF

Timing Requirements (T_A = -30 to +85°C, V_{DD1} = 3.3 V ±0.3 V, V_{DD2} = 23 V, V_{EE1} = V_{EE2} = -10 V, V_{SS} = 0 V, t_r = t_f = 20 ns (10 to 90%))

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Pulse High Width	PW _{CLK(H)}		500			ns
Clock Pulse Low Width	PW _{CLK(L)}		500			ns
Enable Pulse Width	PW _{OE}	OE	1000			ns
Start Pulse Setup Time	t _{SETUP1}	STV ↑ → CLK ↑	200			ns
Start Pulse Hold Time	t _{HOLD1}	CLK ↑ → STV ↓	200			ns
Double Scan Setup Time	t _{SETUP2}	DS ↑ → CLK ↑	200			ns
Double Scan Hold Time	t _{HOLD2}	CLK ↑ → DS ↓	200			ns

Remark Unless otherwise specified, the input level is defined to be V_{IH} = 0.8 V_{DD1}, V_{IL} = 0.2 V_{DD1}.

NOTES FOR CMOS DEVICES**① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents**NEC Semiconductor Device Reliability/Quality Control System (C10983E)****Quality Grades On NEC Semiconductor Devices (C11531E)**

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