

**7300 PIXELS  $\times$  3 COLOR CCD LINEAR IMAGE SENSOR**

The  $\mu$ PD3788 is a high-speed and high sensitive color CCD (Charge Coupled Device) linear image sensor which changes optical images to electrical signal and has the function of color separation.

The  $\mu$ PD3788 has 3 rows of 7300 pixels, and it is a 2-output/color type CCD sensor with 2 rows/color of charge transfer register, which transfers the photo signal electrons of 7300 pixels separately in odd and even pixels. Moreover, the spectral response characteristics of the  $\mu$ PD3788 is modified from the previous device  $\mu$ PD3728 to be suitable for Xe-lamp. Therefore, it is suitable for 600 dpi/A3 high-speed color digital copiers and so on.

**FEATURES**

- Valid photocell : 7300 pixels  $\times$  3
- Photocell pitch : 10  $\mu$ m
- Photocell size : 10  $\times$  10  $\mu$ m<sup>2</sup>
- Line spacing : 40  $\mu$ m (4 lines) Red line-Green line, Green line-Blue line
- Color filter : Primary colors (red, green and blue), pigment filter (with light resistance 10<sup>7</sup> lx•hour)
- Resolution : 24 dot/mm (600 dpi) A3 (297  $\times$  420 mm) size (shorter side)
- Drive clock level : CMOS output under 5 V operation
- Data rate : 40 MHz MAX. (20 MHz/1 output)
- Output type : 2 outputs in phase/color
- Power supply : +12 V
- On-chip circuits : Reset feed-through level clamp circuits  
Voltage amplifiers

**ORDERING INFORMATION**

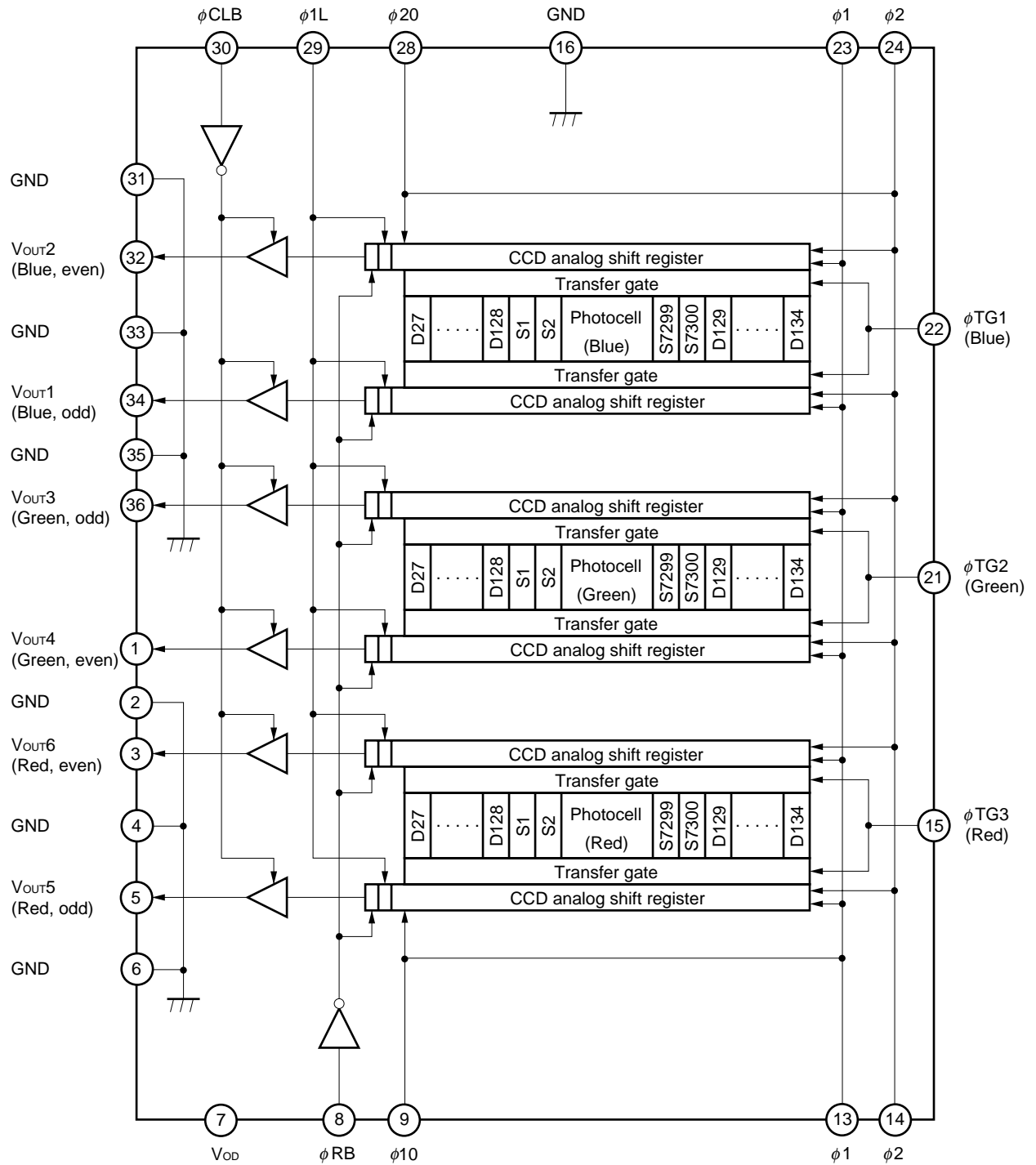
Part Number	Package
$\mu$ PD3788D	CCD linear image sensor 36-pin ceramic DIP (15.24 mm (600))

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.  
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

COMPARISON CHART

Item		μPD3788	μPD3728		
ABSOLUTE MAXIMUM RATINGS	Shift register clock voltage (V)		-0.3 to +8	-0.3 to +15	
	Reset gate clock voltage (V)		-0.3 to +8	-0.3 to +15	
	Reset feed-through level clamp clock voltage (V)		-0.3 to +8	-0.3 to +15	
	Transfer gate clock voltage (V)		-0.3 to +8	-0.3 to +15	
ELECTRICAL CHARACTERISTICS	Saturation exposure (lx·s)	Red	TYP.	0.36	0.35
		Green	TYP.	0.37	0.39
		Blue	TYP.	0.80	0.31
	Response (V/lx·s)	Red	MIN.	3.85	3.9
			TYP.	5.5	5.6
			MAX.	7.15	7.3
		Green	MIN.	3.78	3.6
			TYP.	5.4	5.1
			MAX.	7.02	6.6
		Blue	MIN.	1.75	4.5
			TYP.	2.5	6.4
			MAX.	3.25	8.3
	Response peak (nm)	Red	TYP.	645	630
		Green	TYP.	540	540
		Blue	TYP.	445	460
	Random noise test conditions		t <sub>cp</sub> = 20 ns	t7 = 150 ns	
TIMING CHART	t3 (ns)		MIN.	17	20
	t7 (ns)		MIN.	17	20
	t10 (ns)		MIN.	-20	-10
	t <sub>CP</sub> (ns)		MIN.	5	-
			TYP.	150	-
STANDARD CHARACTERISTIC CURVES	TOTAL SPECTRAL RESPONSE CHARACTERISTICS		modified	-	

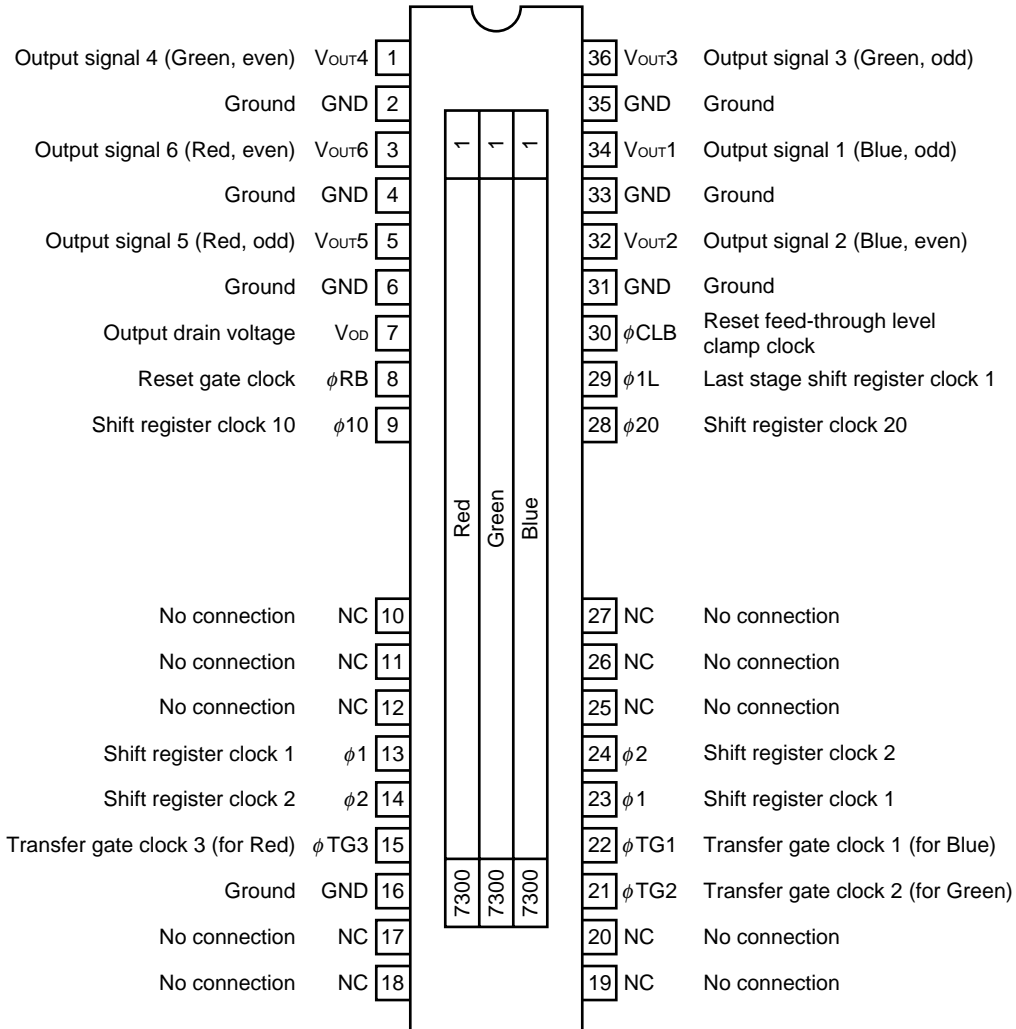
BLOCK DIAGRAM



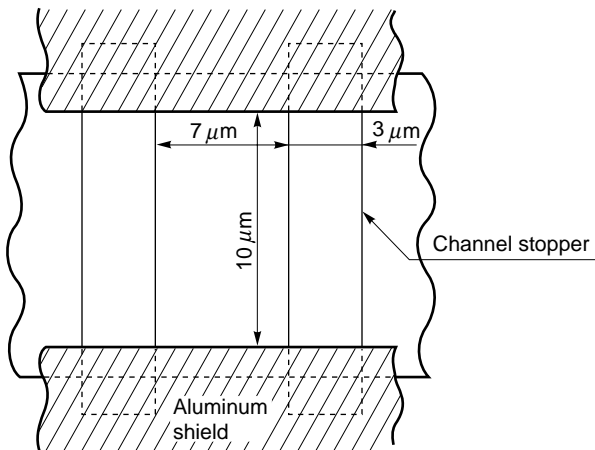
**PIN CONFIGURATION (Top View)**

CCD linear image sensor 36-pin ceramic DIP (15.24 mm (600))

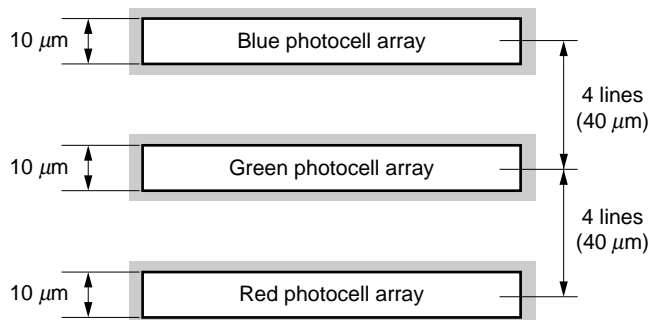
- μPD3788D



**PHOTOCELL STRUCTURE DIAGRAM**



**PHOTOCELL ARRAY STRUCTURE DIAGRAM (Line spacing)**



**ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = +25 °C)**

Parameter	Symbol	Ratings	Unit
Output drain voltage	V <sub>OD</sub>	-0.3 to +15	V
Shift register clock voltage	V <sub>φ1</sub> , V <sub>φ1L</sub> , V <sub>φ10</sub> , V <sub>φ2</sub> , V <sub>φ20</sub>	-0.3 to +8	V
Reset gate clock voltage	V <sub>φRB</sub>	-0.3 to +8	V
Reset feed-through level clamp clock voltage	V <sub>φCLB</sub>	-0.3 to +8	V
Transfer gate clock voltage	V <sub>φTG1</sub> to V <sub>φTG3</sub>	-0.3 to +8	V
Operating ambient temperature	T <sub>A</sub>	-25 to +60	°C
Storage temperature	T <sub>stg</sub>	-40 to +100	°C

**Caution** Exposure to **ABSOLUTE MAXIMUM RATINGS** for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The parameters apply independently.

**RECOMMENDED OPERATING CONDITIONS (T<sub>A</sub> = +25 °C)**

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Output drain voltage	V <sub>OD</sub>	11.4	12.0	12.6	V
Shift register clock high level	V <sub>φ1H</sub> , V <sub>φ1LH</sub> , V <sub>φ10H</sub> , V <sub>φ2H</sub> , V <sub>φ20H</sub>	4.5	5.0	5.5	V
Shift register clock low level	V <sub>φ1L</sub> , V <sub>φ1LL</sub> , V <sub>φ10L</sub> , V <sub>φ2L</sub> , V <sub>φ20L</sub>	-0.3	0	+0.5	V
Reset gate clock high level	V <sub>φRBH</sub>	4.5	5.0	5.5	V
Reset gate clock low level	V <sub>φRBL</sub>	-0.3	0	+0.5	V
Reset feed-through level clamp clock high level	V <sub>φCLBH</sub>	4.5	5.0	5.5	V
Reset feed-through level clamp clock low level	V <sub>φCLBL</sub>	-0.3	0	+0.5	V
Transfer gate clock high level <sup>Note</sup>	V <sub>φTG1H</sub> to V <sub>φTG3H</sub>	4.5	V <sub>φ1H</sub> (V <sub>φ10H</sub> )	V <sub>φ1H</sub> (V <sub>φ10H</sub> )	V
Transfer gate clock low level	V <sub>φTG1L</sub> to V <sub>φTG3L</sub>	-0.3	0	+0.5	V
Data rate	2f <sub>φRB</sub>	-	2	40	MHz

**Note** When Transfer gate clock high level (V<sub>φTG1H</sub> to V<sub>φTG3H</sub>) is higher than Shift register clock high level (V<sub>φ1H</sub> (V<sub>φ10H</sub>)), Image lag can increase.

**Remark** Pin 9 (φ10) and pin 28 (φ20) should be open to decrease the influence of input clock noise to output signal waveform, in case of operating at low or middle speed range; data rate under 24 MHz or so.

**ELECTRICAL CHARACTERISTICS**

(  $T_A = +25\text{ }^\circ\text{C}$ ,  $V_{OD} = 12\text{ V}$ ,  $f_{\phi RB} = 1\text{ MHz}$ , data rate = 2 MHz, storage time = 10 ms, input signal clock = 5 V<sub>p-p</sub>,  
light source: 3200 K halogen lamp +C-500S (infrared cut filter, t = 1mm) +HA-50 (heat absorbing filter, t = 3mm) )

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Saturation voltage	$V_{sat}$		1.5	2.0	–	V
Saturation exposure	Red	SER		0.36		lx·s
	Green	SEG		0.37		lx·s
	Blue	SEB		0.80		lx·s
Photo response non-uniformity	PRNU	$V_{OUT} = 1\text{ V}$		6	18	%
Average dark signal <b>Note 1</b>	ADS1	Light shielding		1.0	5.0	mV
	ADS2			0.5	5.0	mV
Dark signal non-uniformity <b>Note 1</b>	DSNU1	Light shielding		2.0	5.0	mV
	DSNU2			1.0	5.0	mV
Power consumption	$P_W$			600	800	mW
Output impedance	$Z_o$			0.3	0.5	kΩ
Response	Red	$R_R$	3.85	5.5	7.15	V/lx·s
	Green	$R_G$	3.78	5.4	7.02	V/lx·s
	Blue	$R_B$	1.75	2.5	3.25	V/lx·s
Image lag <b>Note 1</b>	IL1	$V_{OUT} = 1\text{ V}$		2.0	5.0	%
	IL2			1.0	5.0	%
Offset level <b>Note 2</b>	$V_{os}$		4.0	5.0	6.0	V
Output fall delay time <b>Note 3</b>	$t_d$	$V_{OUT} = 1\text{ V}$		20		ns
Register imbalance	RI	$V_{OUT} = 1\text{ V}$	0		4.0	%
Total transfer efficiency	TTE	$V_{OUT} = 1\text{ V}$ , data rate = 40 MHz	95	98		%
Response peak	Red			645		nm
	Green			540		nm
	Blue			445		nm
Dynamic range <b>Note 1</b>	DR11	$V_{sat}/DSNU1$		1000		times
	DR12	$V_{sat}/DSNU2$		2000		times
	DR21	$V_{sat}/\sigma_{bit1}$		2000		times
	DR22	$V_{sat}/\sigma_{bit2}$		4000		times
Reset feed-through noise <b>Note 2</b>	RFTN	Light shielding	–500	+200	+500	mV
Random noise <b>Note 1</b>	$\sigma_{bit1}$	Light shielding, bit clamp	–	1.0	–	mV
	$\sigma_{bit2}$	mode ( $t_{cp} = 20\text{ ns}$ )	–	0.5	–	mV
	$\sigma_{line1}$	Light shielding, line	–	4.0	–	mV
	$\sigma_{line2}$	clamp mode ( $t_{19} = 3\text{ }\mu\text{s}$ )	–	2.0	–	mV

**Notes 1.** ADS1, DSNU1, IL1, DR11, DR21,  $\sigma_{bit1}$  and  $\sigma_{line1}$  show the specification of  $V_{OUT1}$  and  $V_{OUT2}$ .  
ADS2, DSNU2, IL2, DR12, DR22,  $\sigma_{bit2}$  and  $\sigma_{line2}$  show the specification of  $V_{OUT3}$  to  $V_{OUT6}$ .

**2.** Refer to **TIMING CHART 2, 5**.

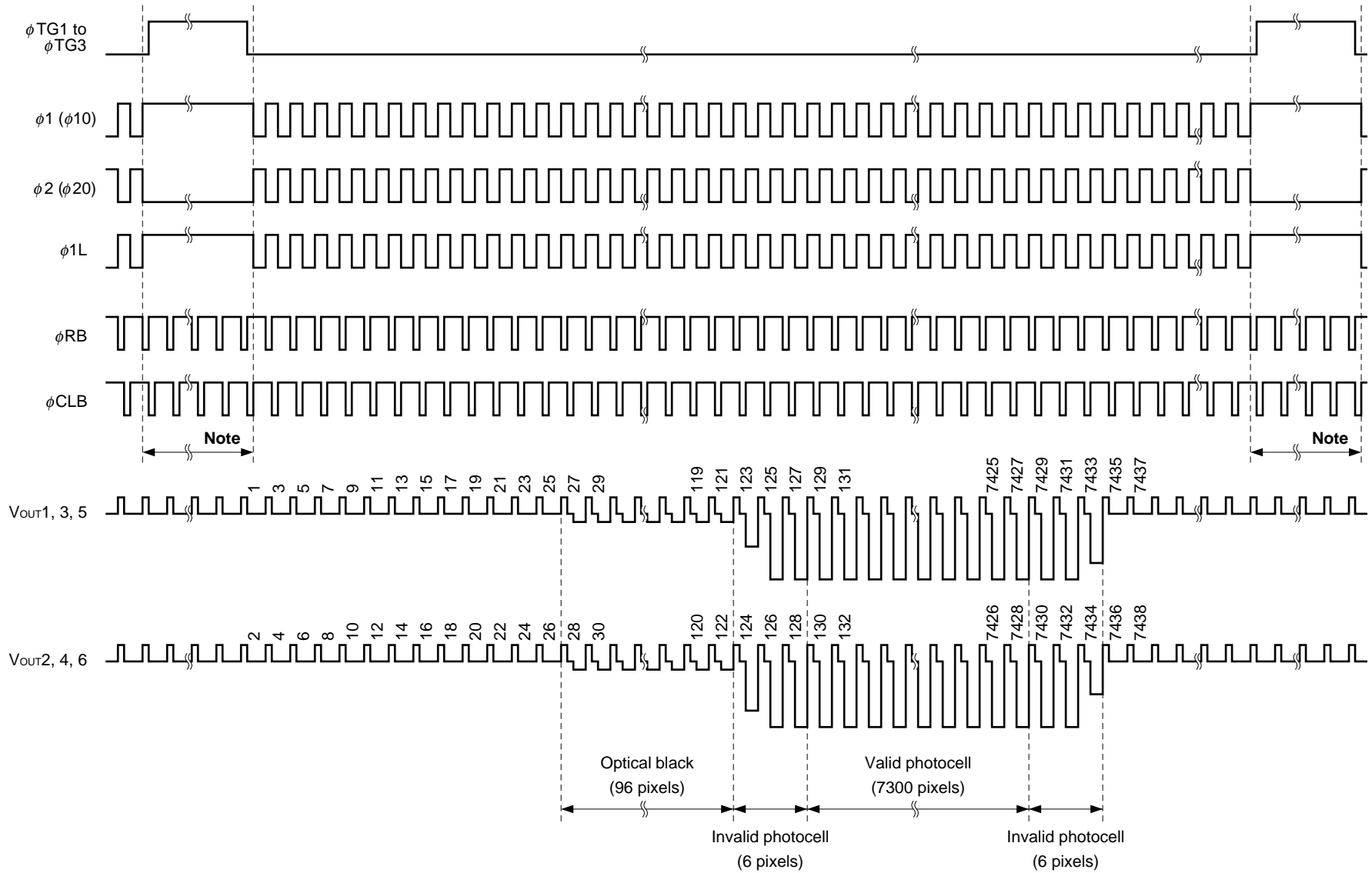
**3.** When the fall time of  $\phi 1L$  ( $t_2'$ ) is the TYP. value (refer to **TIMING CHART 2, 5**).

INPUT PIN CAPACITANCE ( $T_A = +25\text{ }^\circ\text{C}$ ,  $V_{OD} = 12\text{ V}$ )

Parameter	Symbol	Pin name	Pin No.	MIN.	TYP.	MAX.	Unit
Shift register clock pin capacitance 1	$C_{\phi 1}$	$\phi 1$	13		350	500	pF
			23		350	500	pF
		$\phi 10$	9		350	500	pF
Shift register clock pin capacitance 2	$C_{\phi 2}$	$\phi 2$	14		350	500	pF
			24		350	500	pF
		$\phi 20$	28		350	500	pF
Last stage shift register clock pin capacitance	$C_{\phi L}$	$\phi 1L$	29		10		pF
Reset gate clock pin capacitance	$C_{\phi RB}$	$\phi RB$	8		10		pF
Reset feed-through level clamp clock pin capacitance	$C_{\phi CLB}$	$\phi CLB$	30		10		pF
Transfer gate clock pin capacitance	$C_{\phi TG}$	$\phi TG1$	22		100		pF
		$\phi TG2$	21		100		pF
		$\phi TG3$	15		100		pF

**Remark** Pins 13, 23 ( $\phi 1$ ) and pin 9 ( $\phi 10$ ) are connected each other inside of the device.  
Pins 14, 24 ( $\phi 2$ ) and pin 28 ( $\phi 20$ ) are connected each other inside of the device.

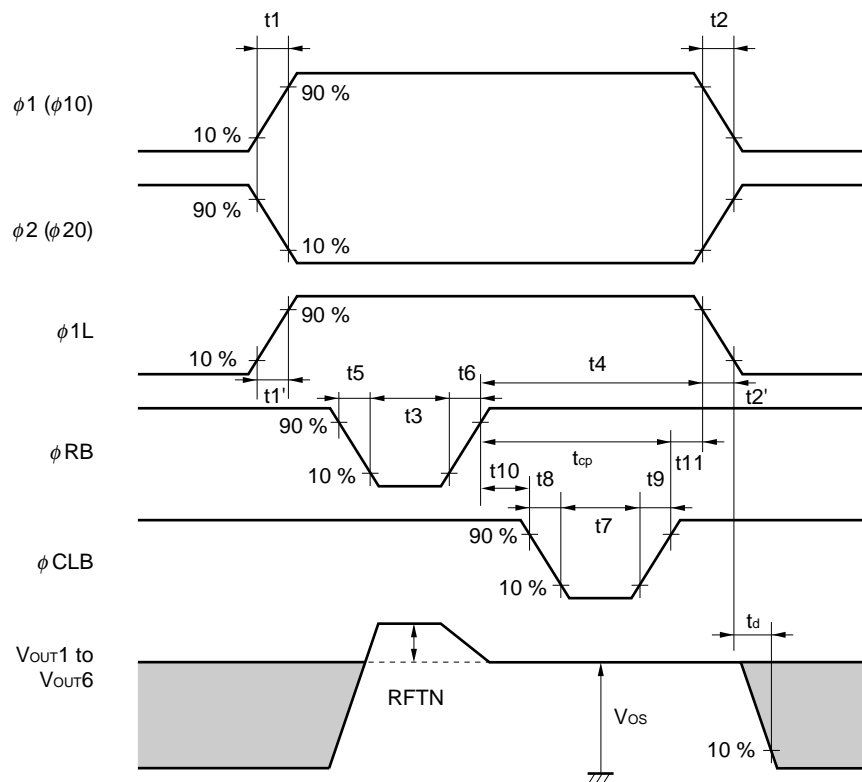
**TIMING CHART 1 (Bit clamp mode, for each color)**



**Note** Input the  $\phi$ RB and  $\phi$ CLB pulses continuously during this period, too.

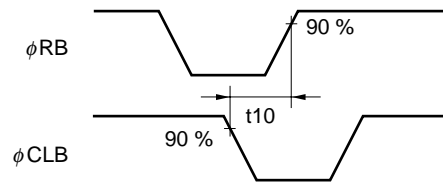


TIMING CHART 2 (Bit clamp mode, for each color)

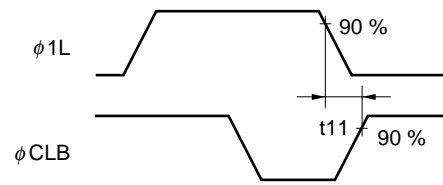


Symbol	MIN.	TYP.	MAX.	Unit
$t_1, t_2$	0	50		ns
$t_1', t_2'$	0	5		ns
$t_3$	17	50		ns
$t_4$	5	200	—	ns
$t_5, t_6$	0	20		ns
$t_7$	17	150		ns
$t_8, t_9$	0	20		ns
$t_{10}$	-20 <sup>Note 1</sup>	+50	—	ns
$t_{11}$	-5 <sup>Note 2</sup>	+50		ns
$t_{cp}$	5	150		ns

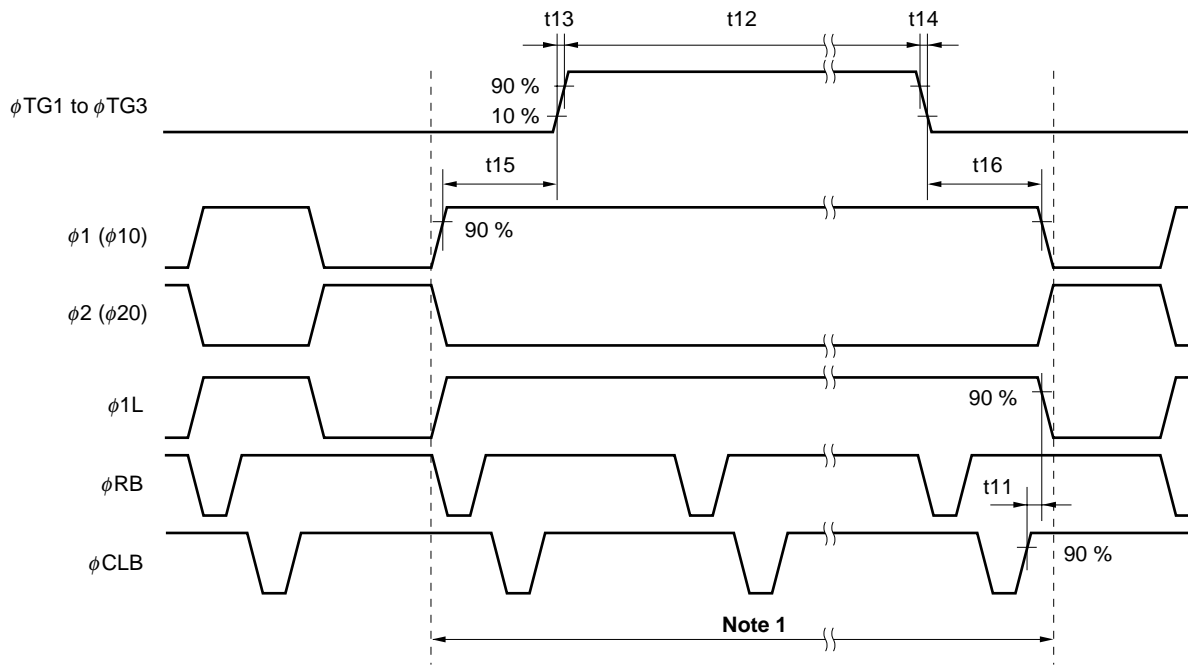
Notes 1. MIN. of t10 shows that the  $\phi$ RB and  $\phi$ CLB overlap each other.



2. MIN. of t11 shows that the  $\phi$ 1L and  $\phi$ CLB overlap each other.

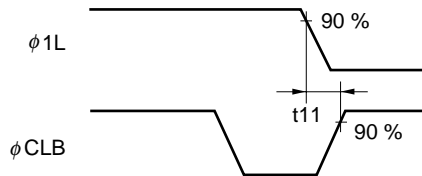


TIMING CHART 3 (Bit clamp mode, for each color)

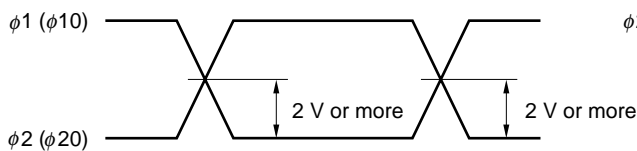


Symbol	MIN.	TYP.	MAX.	Unit
t11	-5Note 2	+50		ns
t12	3000	10000		ns
t13, t14	0	50		ns
t15, t16	900	1000		ns

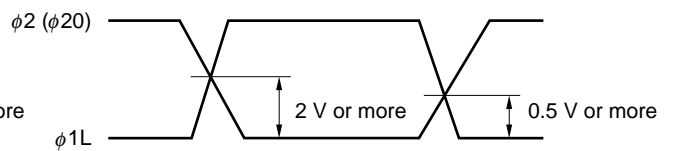
- Notes** 1. Input the  $\phi RB$  and  $\phi CLB$  pulses continuously during this period, too.  
 2. MIN. of t11 shows that the  $\phi 1L$  and  $\phi CLB$  overlap each other.



$\phi 1$  ( $\phi 10$ ),  $\phi 2$  ( $\phi 20$ ) cross points

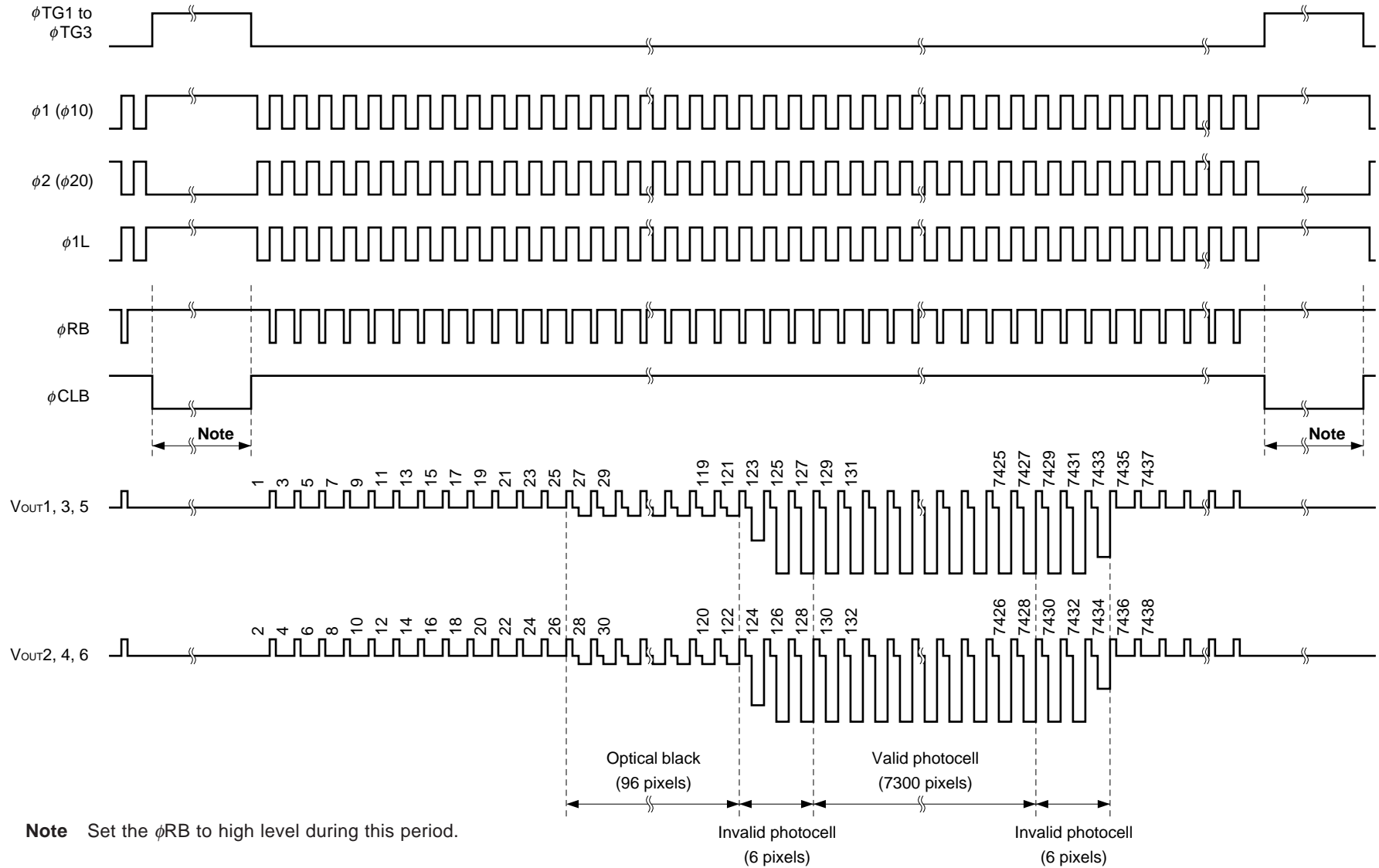


$\phi 1L$ ,  $\phi 2$  ( $\phi 20$ ) cross points



**Remark** Adjust cross points ( $\phi 1$  ( $\phi 10$ ),  $\phi 2$  ( $\phi 20$ )) and ( $\phi 1L$ ,  $\phi 2$  ( $\phi 20$ )) with input resistance of each pin.

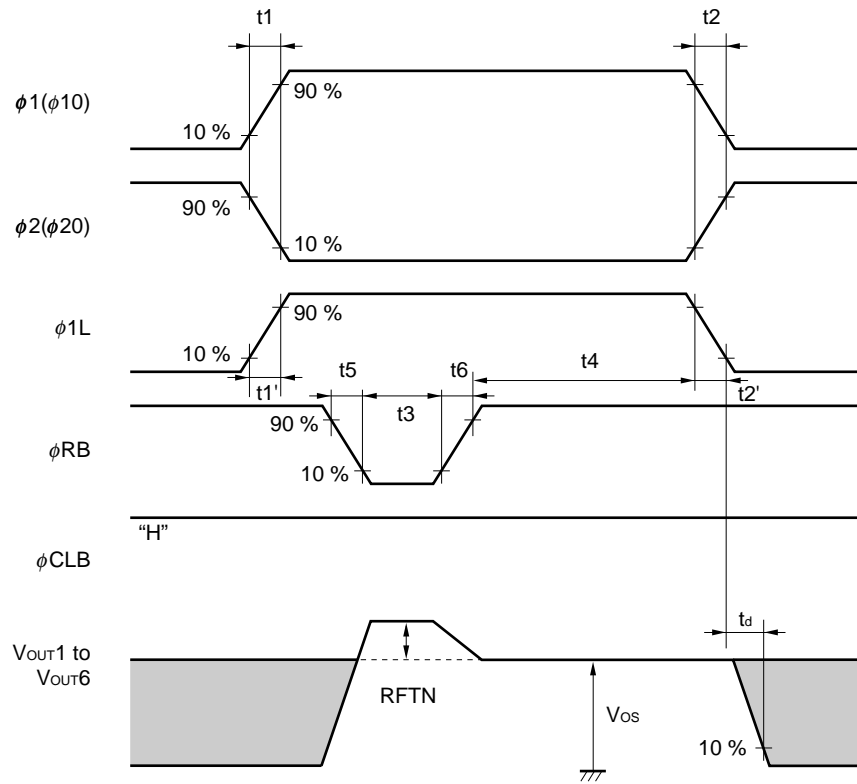
**TIMING CHART 4 (Line clamp mode, for each color)**



**Note** Set the  $\phi RB$  to high level during this period.

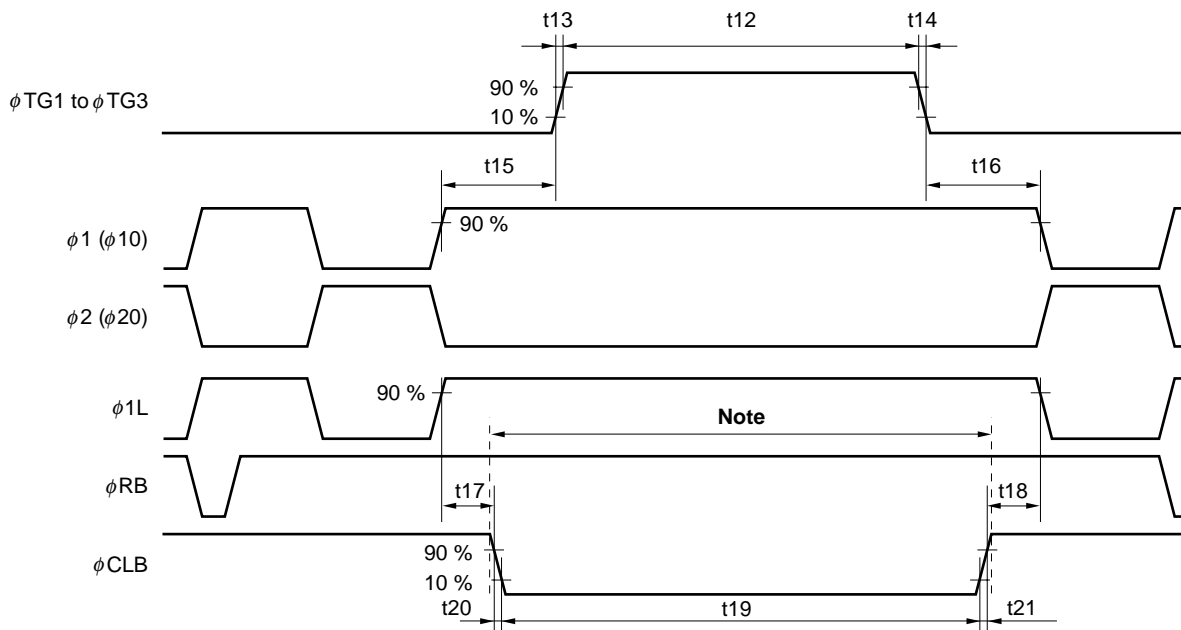
**Remark** Inverse pulse of the  $\phi TG1$  to  $\phi TG3$  can be used as  $\phi CLB$ .

TIMING CHART 5 (Line clamp mode, for each color)



Symbol	MIN.	TYP.	MAX.	Unit
$t_1, t_2$	0	50		ns
$t_1', t_2'$	0	5		ns
$t_3$	17	50		ns
$t_4$	5	200	—	ns
$t_5, t_6$	0	20		ns

**TIMING CHART 6 (Line clamp mode, for each color)**



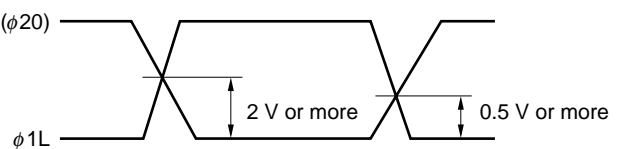
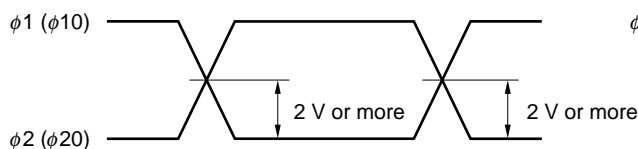
Symbol	MIN.	TYP.	MAX.	Unit
t12	3000	10000		ns
t13, t14	0	50		ns
t15, t16	900	1000		ns
t17, t18	100	1000		ns
t19	200	t12		ns
t20, t21	0	20		ns

**Note** Set the  $\phi$ RB to high level during this period.

**Remark** Inverse pulse of the  $\phi$ TG1 to  $\phi$ TG3 can be used as  $\phi$ CLB.

**$\phi$ 1 ( $\phi$ 10),  $\phi$ 2 ( $\phi$ 20) cross points**

**$\phi$ 1L,  $\phi$ 2 ( $\phi$ 20) cross points**



**Remark** Adjust cross points ( $\phi$ 1 ( $\phi$ 10),  $\phi$ 2 ( $\phi$ 20)) and ( $\phi$ 1L,  $\phi$ 2 ( $\phi$ 20)) with input resistance of each pin.

**DEFINITIONS OF CHARACTERISTIC ITEMS**

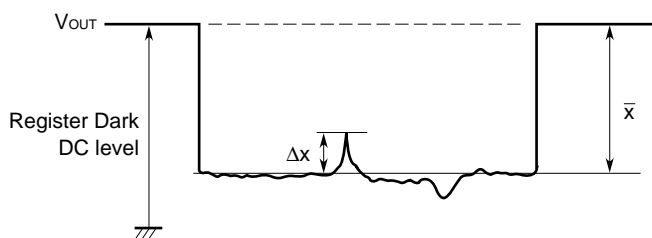
1. Saturation voltage:  $V_{sat}$   
Output signal voltage at which the response linearity is lost.
2. Saturation exposure: SE  
Product of intensity of illumination (lx) and storage time (s) when saturation of output voltage occurs.
3. Photo response non-uniformity: PRNU  
The output signal non-uniformity of all the valid pixels when the photosensitive surface is applied with the light of uniform illumination. This is calculated by the following formula.

$$PRNU (\%) = \frac{\Delta x}{\bar{x}} \times 100$$

$\Delta x$  : maximum of  $|x_j - \bar{x}|$

$$\bar{x} = \frac{\sum_{j=1}^{7300} x_j}{7300}$$

$x_j$  : Output voltage of valid pixel number j



4. Average dark signal: ADS  
Average output signal voltage of all the valid pixels at light shielding. This is calculated by the following formula.

$$ADS (mV) = \frac{\sum_{j=1}^{7300} d_j}{7300}$$

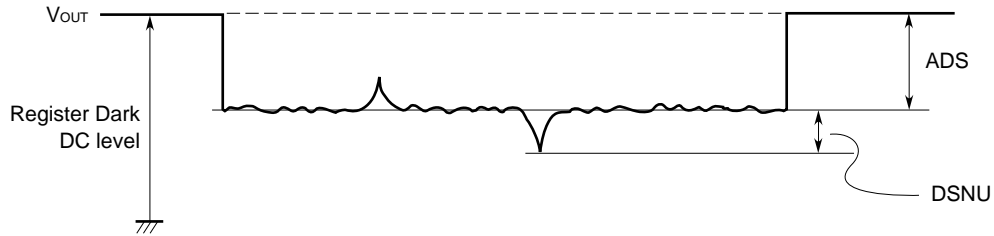
$d_j$  : Dark signal of valid pixel number j

5. Dark signal non-uniformity: DSNU

Absolute maximum of the difference between ADS and voltage of the highest or lowest output pixel of all the valid pixels at light shielding. This is calculated by the following formula.

$$\text{DSNU (mV)} : \text{maximum of } |d_j - \text{ADS}|_{j=1 \text{ to } 7300}$$

$d_j$  : Dark signal of valid pixel number  $j$



6. Output impedance:  $Z_o$

Impedance of the output pins viewed from outside.

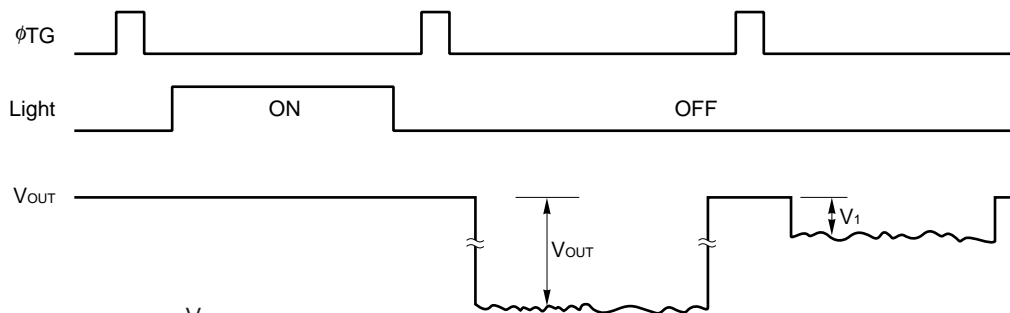
7. Response: R

Output voltage divided by exposure (Ix.s).

Note that the response varies with a light source (spectral characteristic).

8. Image lag: IL

The rate between the last output voltage and the next one after read out the data of a line.



$$\text{IL (\%)} = \frac{V_1}{V_{\text{OUT}}} \times 100$$



9. Register imbalance: RI

The rate of the difference between the averages of the output voltage of Odd and Even pixels, against the average output voltage of all the valid pixels.

$$RI (\%) = \frac{\frac{2}{n} \left| \sum_{j=1}^{\frac{n}{2}} (V_{2j-1} - V_{2j}) \right|}{\frac{1}{n} \sum_{j=1}^n V_j} \times 100$$

n : Number of valid pixels

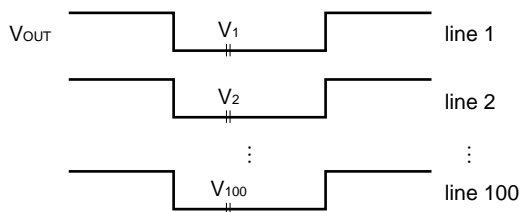
V<sub>j</sub> : Output voltage of each pixel

10. Random noise: σ

Random noise σ is defined as the standard deviation of a valid pixel output signal with 100 times (=100 lines) data sampling at dark (light shielding).

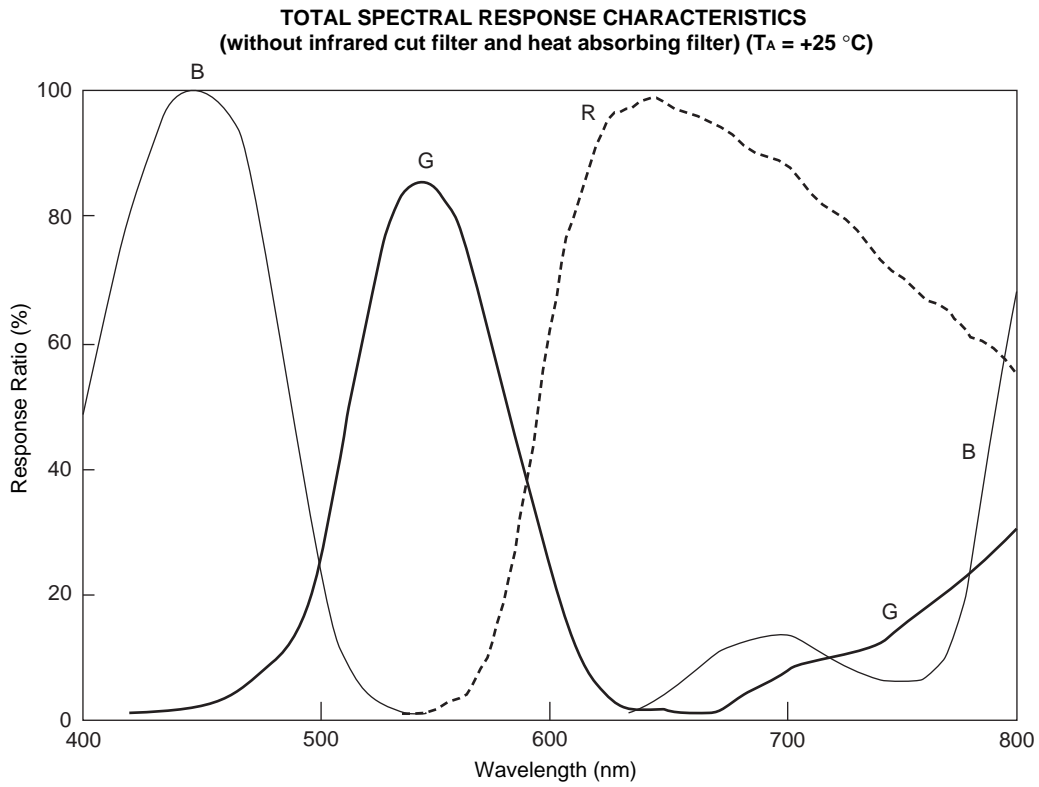
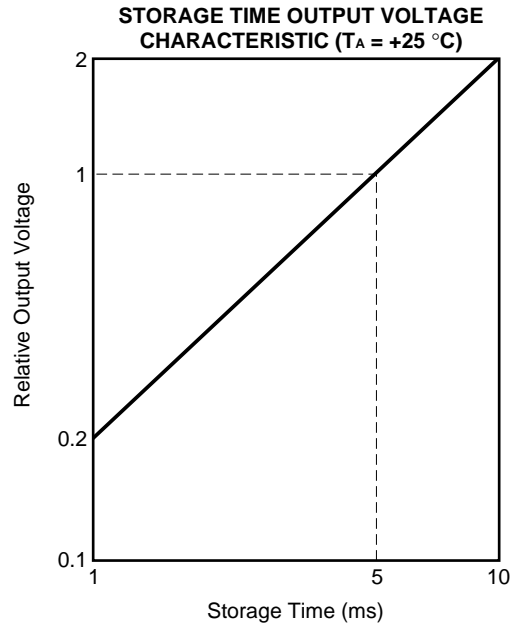
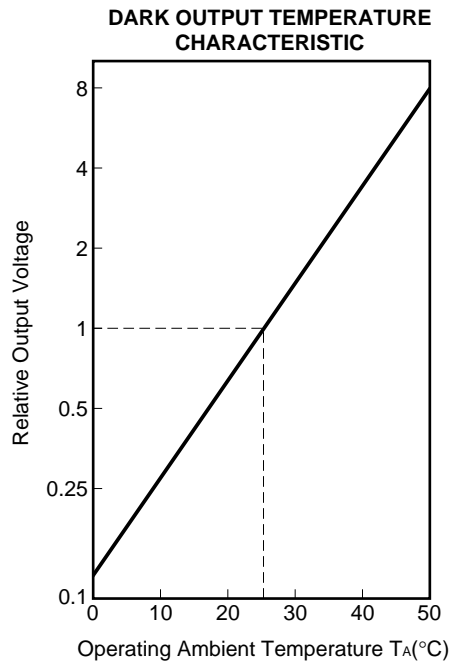
$$\sigma \text{ (mV)} = \sqrt{\frac{\sum_{i=1}^{100} (V_i - \bar{V})^2}{100}}, \quad \bar{V} = \frac{1}{100} \sum_{i=1}^{100} V_i$$

V<sub>i</sub>: A valid pixel output signal among all of the valid pixels for each color

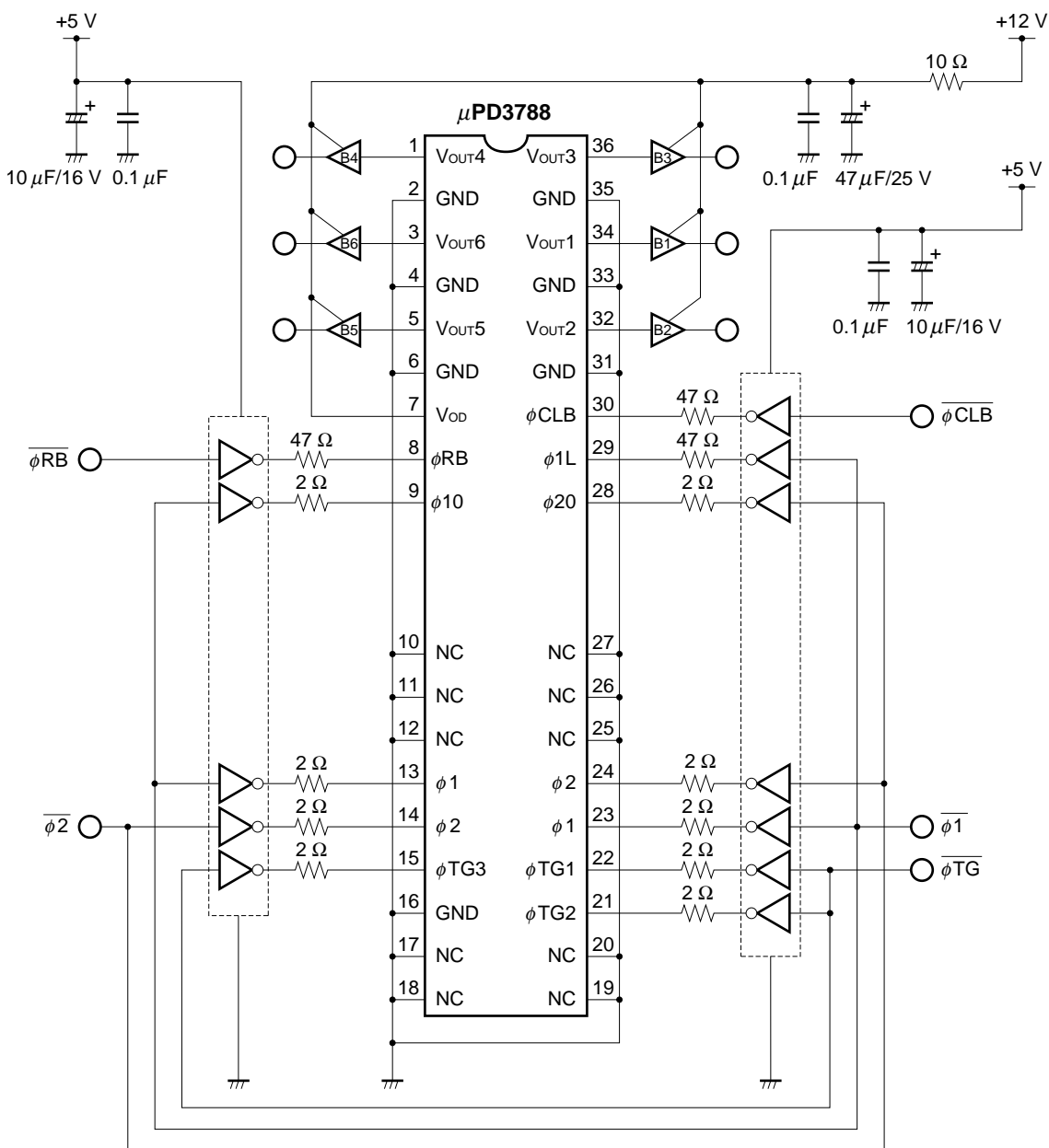


This is measured by the DC level sampling of only the signal level, not by CDS (Correlated Double Sampling).

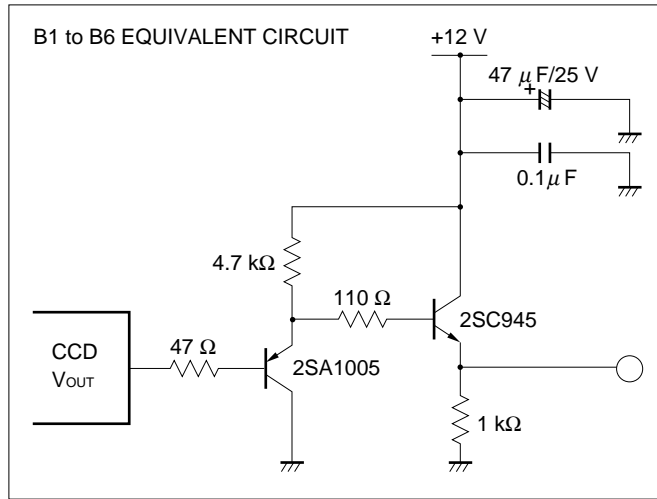
STANDARD CHARACTERISTIC CURVES (Nominal)



APPLICATION CIRCUIT EXAMPLE



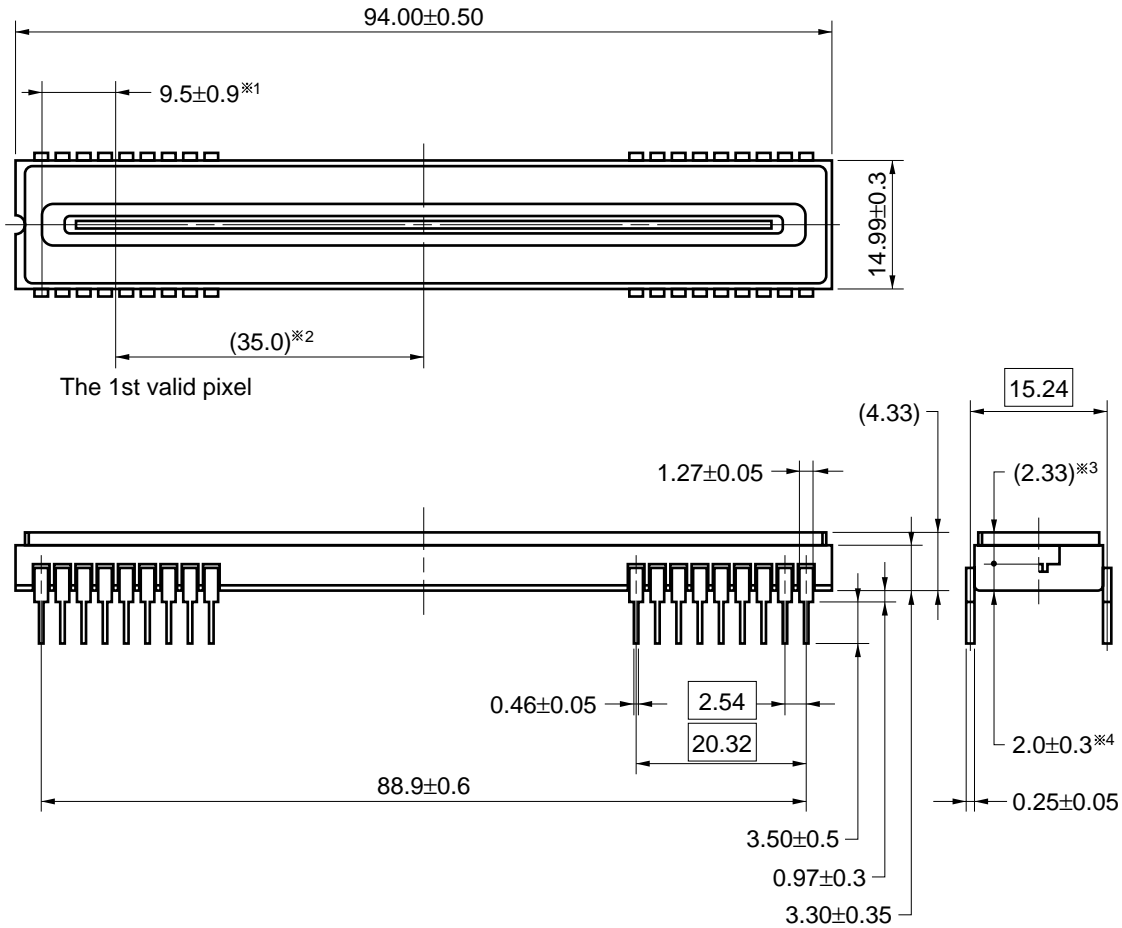
- Remarks**
1. Pin 9 ( $\phi_{10}$ ) and pin 28 ( $\phi_{20}$ ) should be open to decrease the influence of input clock noise to output signal waveform, in case of operating at low or middle speed range; data rate under 24 MHz or so.
  2. The inverters shown in the above application circuit example are the 74AC04.



PACKAGE DRAWING

CCD LINEAR IMAGE SENSOR 36-PIN CERAMIC DIP (15.24mm (600))

(Unit : mm)



Name	Dimensions	Refractive index
Glass cap	$93.0 \times 13.6 \times 1.0$	1.5

- ※1 The 1st valid pixel  $\longleftrightarrow$  The center of the pin1
- ※2 The 1st valid pixel  $\longleftrightarrow$  The center of the package (Reference)
- ※3 The surface of the chip  $\longleftrightarrow$  The top of the glass cap (Reference)
- ※4 The bottom of the package  $\longleftrightarrow$  The surface of the chip

36D-1CCD-PKG1-2

**NOTES ON THE USE OF THE PACKAGE**

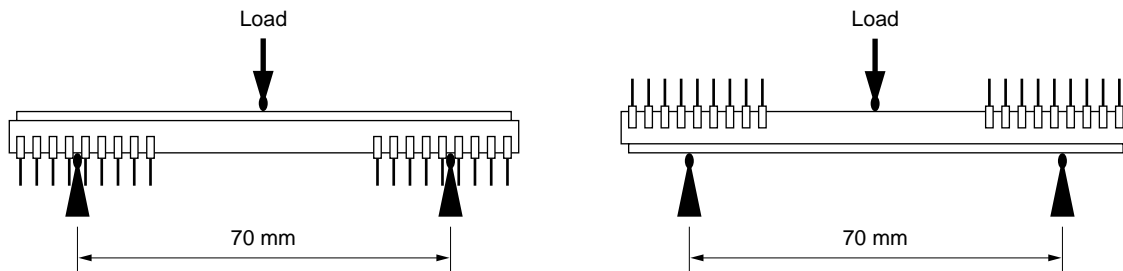
The application of an excessive load to the package may cause the package to warp or break, or cause chips to come off internally. Particular care should be taken when mounting the package on the circuit board.

When mounting the package, use a circuit board which will not subject the package to bending stress, or use a socket.

For this product, the reference value for the three-point bending strength<sup>Note</sup> is 300 [N]. Avoid imposing a load, however, on the inside portion as viewed from the face on which the window (glass) is bonded to the package body (ceramic).

**Note** Three-point bending strength test

Distance between supports: 70 mm, Support R: R 2 mm, Loading rate: 0.5 mm / min.



## NOTES FOR CMOS DEVICES

**① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

**② HANDLING OF UNUSED INPUT PINS FOR CMOS**

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

**③ STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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